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Improved Design of Binary Full Adder

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ABSTRACT

Presented in this paper are a comparison of a conventional full adder circuit and an improved design of binary full adder. The improved full adder circuit consists of 10 transistors reducing the area utilization of about 76.18% from the total standard area of binary full adder design. The overall design has an average power consumption of 2.94uW while achieving the full swing comparing to the 13.2mW power dissipation of conventional 28 CMOS Full Adder transistors architecture. The operating voltage used in this design is 1.2V and the modified binary full adder is designed and implemented in TSMC 65nm CMOS Technology.

Key words: Binary Full Adder, Conventional 26T CMOS Full Adder, Adder

1. INTRODUCTION

Full adder circuit is the core of many digital and analog circuits. It is a critical module for the operation of complex arithmetic operation such as addition [1]. Improving the performance of adder is essential. The main aim of designing the arithmetic circuit is to reduce power consumption and increase speed [2].
Several papers have investigated different approaches in realizing full adders using CMOS technology. At the same time, most tend to use the conventional structure [3].

Table 1. Truth Table for a 1-bit adder

A	B	C_{in}	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The objective of this work is to improve the conventional full adder. Performance criteria considered for design comparison include the area, delay, and power consumption as it is regarded as the main aim in designing arithmetic circuits [5]. The goal of a full binary adder is to implement the following truth table for each bit. In a binary adder circuit, A B and Cin act as input bits with SUM and CARRY that act as outputs

$$SUM = (A \oplus B) \oplus Cin \quad (1)$$
$$Cout = (A.B) + (Cin.(A \oplus B)) \quad (2)$$

2. RESEARCH METHODOLOGY

A basic architecture design was the basis of standard binary full adder design based on conventional CMOS full adder

2.1 Conventional Full Adder Architecture

The conventional full adder design consists of 28 transistors. The structure poses several disadvantages – the presence of a series of transistors causes the adder to have the poor driving capability, and it occupies more area due to several transistors [6].

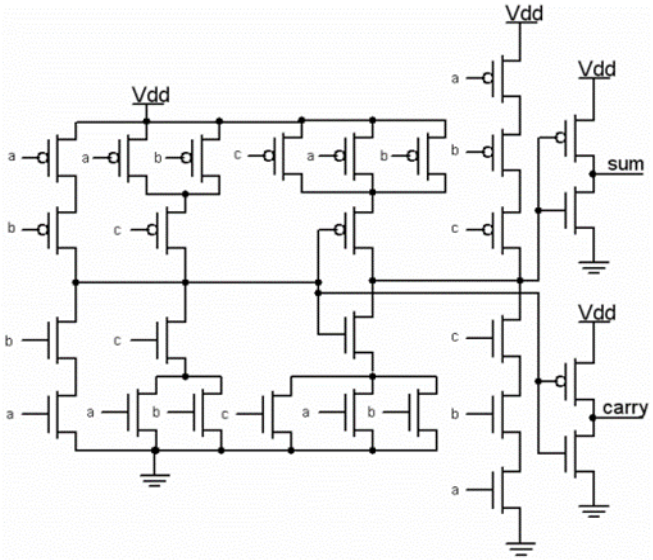


Figure 1: Conventional CMOS Full Adder

2.2 Improved Full Adder

The improved adder consists of 10 transistors. The structure is designed for low power combinational circuits [7]. This approach diminishes power utilization, delay of the circuit and while keeping up a logic circuit with less complexity

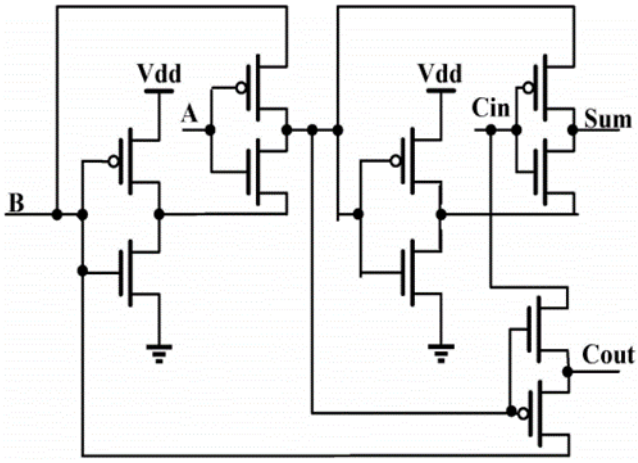
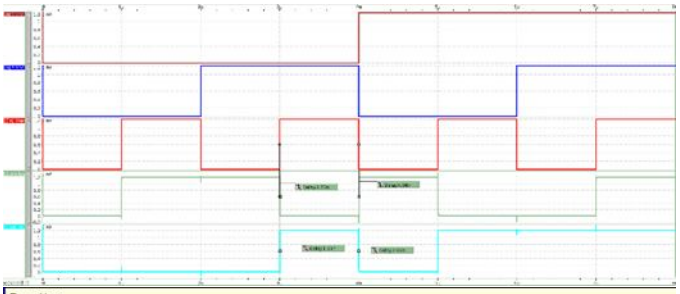


Figure 2: Improved Full Adder Circuit

3. RESULTS AND DISCUSSION

The basic conventional full adder and improved full adder pre-sim propagation and power consumption are simulated.

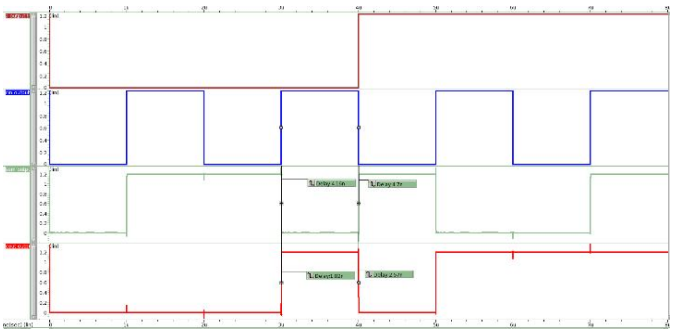
3.1 Conventional Full Adder



Equation

File	Equation	Specification		Result		Pass/Fail
		Min	Max	Value	Mean	
D0:tran:tran	rmsval(p(v2),0,8u)			46u		

Figure 3: Pre-sim propagation delay and power consumption of conventional full adder



Equation

File	Equation	Specification		Result		Pass/Fail
		Min	Max	Value	Mean	
D0:output:tr0	rmsval(p(v2),0,8u)			30.7u		

Figure 4: Post-sim propagation delay and power consumption of conventional full adder

Figure 3 and Figure 4 shows the simulation output of the conventional adder. The results are summarized in Table 2. The propagation delay of signal Sum with respect to Cin, t_{PHL} is 3.733 ns and t_{PLH} is 4.06 ns while for the signal Cout, t_{PHL} is 1.43 ns and t_{PLH} is 2.09 ns.

Table 2: Propagation delay for Conventional

	PRE-SIM		POST-SIM	
	t_{PHL}	t_{PLH}	t_{PHL}	t_{PLH}
Sum	3.733 ns	4.06 ns	4.16ns	4.7ns
Cout	1.43 ns	2.09 ns	1.82ns	2.57n

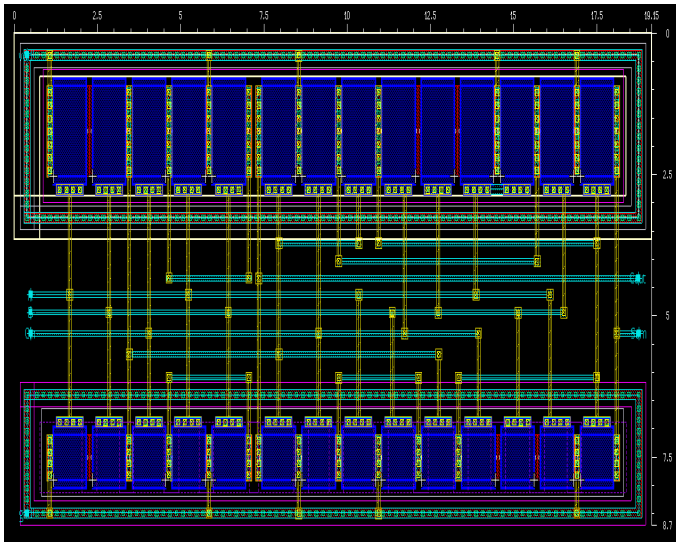
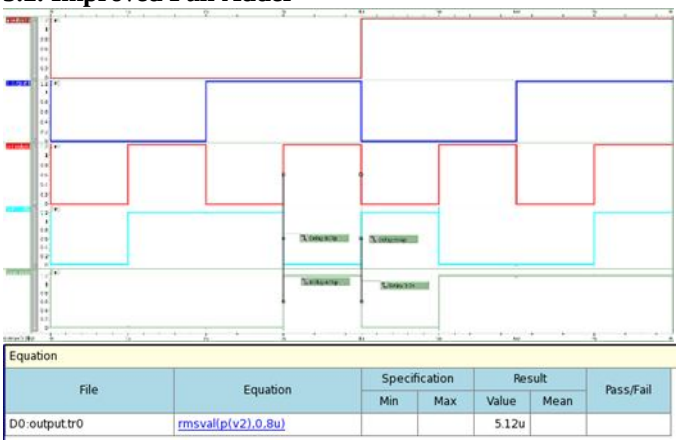


Figure 5: Conventional Adder Lay-out

Figure 5 shows the conventional adder layout. The dimension for the layout is 19.15µm x 8.70µm.

3.2. Improved Full Adder

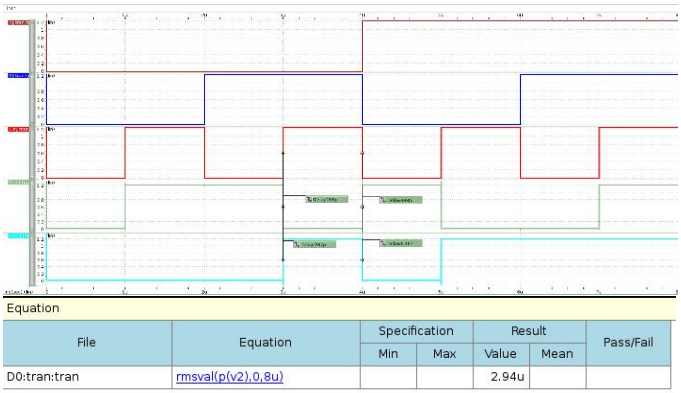


Equation

File	Equation	Specification		Result		Pass/Fail
		Min	Max	Value	Mean	
D0:output:tr0	rmsval(p(v2),0,8u)			5.12u		

Figure 6: Pre-sim propagation delay and power consumption of Improved Full Adder

Figure 6 and Figure 7 shows the simulation output of the improved adder. Although the adder itself consists of 10T transistor, a buffer was used in the Sum and Carry output to restore the signal to its original level – vdd for logic high and gnd for a logic low. The propagation delay from Low to High t_{PLH} and High to low logic t_{PHL} as well as the power consumption, was measured.



Equation

File	Equation	Specification		Result		Pass/Fail
		Min	Max	Value	Mean	
D0:tran:tran	rmsval(p(v2),0,8u)			2.94u		

Figure 7: Post-sim propagation delay and power consumption of Improved Full Adder

The simulation results are summarized in Table 3. The propagation delay of signal Sum with respect to Cin, t_{PHL} is 268 ps and t_{PLH} is 388 ps while for the signal Cout, t_{PHL} is 267 ps and t_{PLH} is 1.46 ns

Table 3: Propagation Delay for Improved

	PRE-SIM		POST-SIM	
	t_{PHL}	t_{PLH}	t_{PHL}	t_{PLH}
Sum	467ps	664ps	268 ps	388 ps
Cout	476ps	3.2n	267 ps	1.46 ns

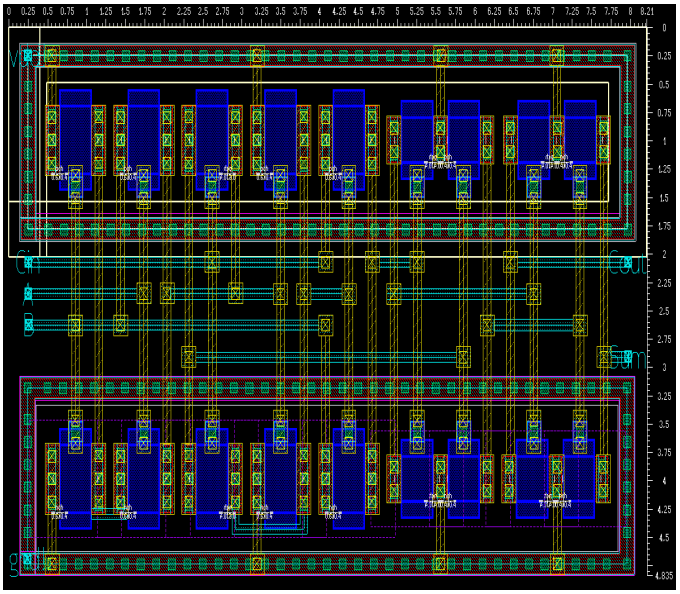


Figure 8: The improved 10T Binary Adder design

Figure 8 shows the improved adder layout. The dimension for the layout of the 10T adder is 8.21 µm x 4.835 µm. The design is much compact compared to the conventional full adder design.

3.3. Comparison

Table 4: Table of Comparison

	PRE-SIM	POST-SIM		
Adder Type	**Average Power Consumption**		**No. of Transistors**	**Layout Dimension**
Conventional	46u	30.7u	28	19.15u x 8.70u
Improved	5.12u	2.94u	10	8.21u x 4.835u

Table 4 shows the comparison of the two adders in terms of power consumption and the number of transistors. The consumption of conventional adder is higher than the improved adder. This is due to the structure of each adder. The number of transistors influences the driving capability of the circuit and power consumption.

Table 5: Other work in terms of binary full adder design

Work	Technology	No of Transistors	Power Consumption
[1]	45nm	16T	1.91.mW
[2]	65nm	-	17.92mW
[3]	-	10T	5.60mW
[4]	CMOS	28T	13.2mW
This work	65nm	10T	2.94uW

From the result shown in Table 2 and Table 3, the 10T adder implemented with buffer at the output has a lesser propagation delay compared to the conventional adder. For the area utilization, the 10T adder uses lesser space compared to the conventional adder.

4. CONCLUSION

The aim of this work was the power reduction in the full adder circuit. A 10T Adder is used. Techniques like transistor size optimization and addition of buffer at the output stage, reduce the power consumption, and achieve full swing. The average power consumption of the 10T adder is 2.94uW with a layout area dimension of 8.21 µm x 4.835 µm. The results are obtained with spice simulation tools.

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