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SEPIC Re-Lift Converter with Reduced Ripple and Improved Time Domain Response

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ABSTRACT

Single ended primary inductor converter (SEPIC) is a good interface between photo voltaic (PV) source and dc load. This work deals with simulation of SEPIC re-lift converter system (SRLCS) in closed loop. A T-filter is suggested at output side to reduce the voltage ripple. Ripples present in output reduce the performance of load. The objective of the proposed SRLCS system is to provide a well regulated dc output voltage. The output of hysteresis controller (HC), proportional integral derivative (PID), fractional order proportional integral derivative (FOPID) and fuzzy controlled (FC) closed loop SRLCS are compared. Comparative results illustrate that fuzzy controlled system outperforms the other methods and therefore it is a viable alternative for the existing dc-dc converters.

Key words: Single ended primary inductor converter (SEPIC), Re-lift converter system (RLCS), Voltage lifting (VL) techniques, Matlab Simulink

1. INTRODUCTION

Design of high efficiency dc-dc converters with compact control structure is essential for applications which require very high voltage [1]. Typical examples include: non-conventional energy sources, power factor correction, portable electronic equipments, and battery powered sources [2]. The well-celebrated SEPIC converter which is a variant of buck-boost converter finds extensive use in high step-up applications due to its low input current ripple, flexibility in output voltage gain and non-inverted output [3]. Step-less voltage gain is possible with the SEPIC converter when it is operated at a very high duty cycle value, but at the cost of severe stress imposed on power semiconductor devices. Moreover, classical converters experience reverse recovery effect and interference due to electromagnetic induction because parasitic resistances gets excited at high operating duty. As a result, the converter efficiency gets reduced [4]-[7]. To preclude the aforesaid problems, many variations in dc-dc converter topology have been proposed in the literature. Converters developed by using the voltage transferring capability of a transformer and by means of n-cell cascade connection, it is possible to obtain a large voltage gain but at the cost of an increase in control circuit complexity, high cost and switching losses [5]. Transformer-less converters such as switched capacitor (SC), switched inductor (SI) and voltage multiplier (VM) cells in combination with a conventional converter topology can also provide large dc output voltage [6]-[8]. In a recent extensive survey, the relative merits and demerits of various state-of-the-art new boost converter topologies have been reviewed for a large number of applications that need a high dc output voltage [9].

A new approach to obtain high step-up ratio is to use voltage lift (VL) technique, which can lead to an improvement in the performance and characteristics of dc-dc converters. F. L. Luo has created a new series of positive output voltage dc-dc converters which can be used to extend the operating voltage range without taking too high value of conduction duty. Luo converter and its derivatives give enhanced voltage transfer gain with advantages: reduced EMI, high power density, small size and simple control structure. The well-established Luo converter finds extensive use in design of electronic circuits and in particular radio engineering [10]-[13]. Several voltage lift circuits have been derived from the SEPIC prototype in [7], for use in applications which require high output voltage gain. VL technique is applied to the basic split inductor type boost converter in [10] and re-lift, triple- lift, n^{th}-lift circuits have been constructed from it with an objective of achieving high voltage in dc level. Zero voltage switching (ZVS) and zero current switching (ZCS) methods have been introduced in order to minimize conduction losses which deteriorate the converter efficiency at high frequency operation. The performance of the converter gets affected by ripple content present in input and output. Hyun-Lark Do has proposed a novel soft-switched SEPIC circuit arrangement without ripple content at the input [4]. For getting a good regulated output dc voltage across the load, it is imperative to operate the converters in closed loop. For controlling issues, the conventional controller used is proportional integral (PI) but it fails miserably under large variation in parameters of the system and also under varying load conditions. Sliding mode control (SMC) strategies have been greatly explored in the literature to get good dynamic response [14], [15]. However, intelligent controllers are preferred over SMC in the sense that it does not need a precise mathematical model and also it can be easily integrated with the system [3], [16]-[18]. In [3], a real time implementation of fuzzy controlled SEPIC to track the maximum power point of a solar system is presented. A genetic fuzzy PID controlled system is presented for controlling the wind turbine generator system [16]. Fuzzy controlled scheme is proposed for reducing total harmonic distortion in three phase grid connected inverter [17]. Open and closed loop performance of various voltage lifted cascaded SEPIC converter systems have been compared to identify a better cascaded converter which can provide high dc power output [18].

Motivated by the encouraging results shown in [3], [4], [7], [10]-[13] the aim of this work is to compare the performance of HC, PID, FOPID and FC controlled SEPIC re-lift system in closed loop. Simulation studies have been extensively done and comparative results indicate that the performance of fuzzy controller is superior to other controllers in terms of settling time and steady state error.

The paper is organized as follows: After a brief introduction in section 1, operation of ZVS resonant converter is presented in section 2. Simulation results in closed loop are reported in section 3. The conclusions are stated in section 4.

2. ZVS RESONANT SEPIC CONVERTER [4]

(Adapted from Hyun-Lark Do IEEE Trans. on Power Electronics, vol. 27, no. 6, June 2012)

Different versions of classical SEPIC converter are highlighted in the literature. Soft switching ripple free SEPIC converter proposed by Hyun-Lark Do [4] is given in Figure 1(b). In the converter, L_r resonant inductor, clamp circuit with auxiliary switch S_a and clamp capacitor are added to the classical SEPIC converter which is shown in Figure 1(a). The equivalent circuit of SEPIC is given in Figure 1(c), in which L_c is modeled as magnetic inductor L_m and an ideal transformer with turns ratio 1: n. Freewheeling diodes D_a and D_m are coupled across the auxiliary switch S_a and the main switch S_m. C_a and C_m represents the internal capacitances and the switches S_a and S_m are operated asymmetrically. Voltage ripple can be ignored by assuming larger values of the capacitors C_1, C_o and C_c. Inductor L_1 is the smoothing inductor in SEPIC converter which decreases input current ripple.

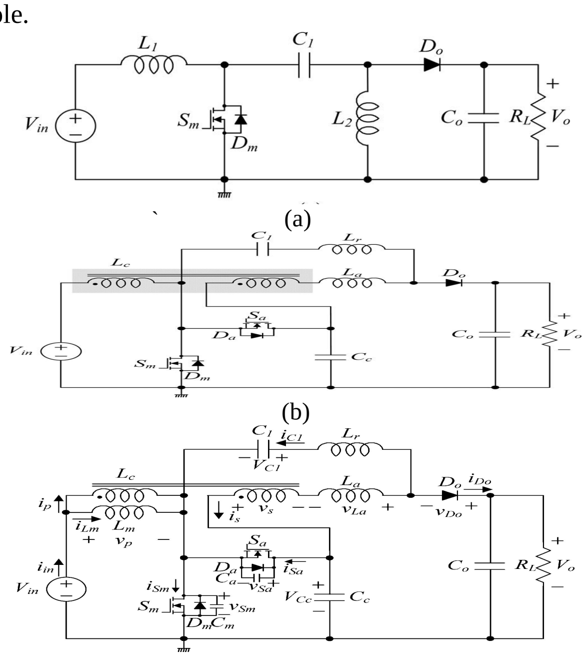


Figure 1: (a) classical SEPIC converter (b) soft-switching ripple-free SEPIC converter (c) equivalent circuit of SEPIC converter

3. SIMULATION RESULTS

This research paper is aimed in comparing the dynamic characteristics of various closed loop SEPIC-RLCS. The block diagram of closed loop system is given in Figure 2.

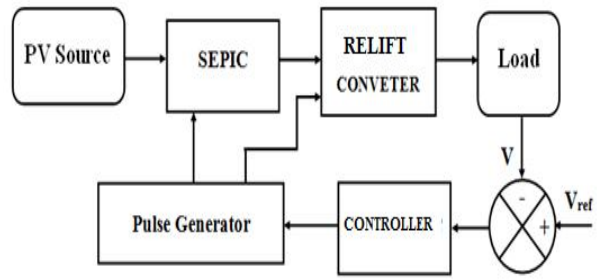
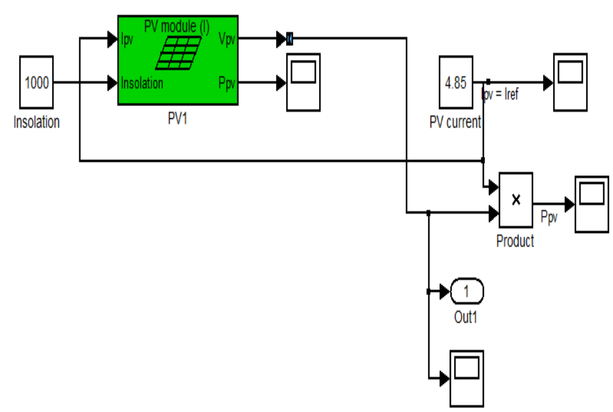


Figure 2: Block diagram of closed loop re-lift converter

3.1 Closed Loop Hysteretic Controlled SEPIC Converter with Re-Lift System

The Matlab simulink model of HC-SRLCS is given in Figure 3(a). The measurement of power from solar panel is illustrated in Figure 3(b). Figure 3(d) represents the voltage across PV of HC-SRLCS and its value is in between 15 and 18 V. The circuit of re-lift system is depicted in Figure 3(c). When switch M_1 is closed, four current loops are established: (i) V_{in} gets coupled to inductor L and charges L to V_{in}. (ii) V_{in} gets coupled through M-D-C_2 thereby charging C_2 to V_{in}. (iii) V_{in} gets coupled through D-L_1-M_1 and charges L_1 to V_{in}, as L, C_2 and L_1 are connected in parallel. (iv) V_{in} gets coupled through D-D_1-C_3-M_1 to ground and therefore C_3 gets charged to V_{in}. If M, M_1 is opened, C_2 and C_3 are connected in series through L_1. The voltage of both capacitors gets added up and thus charging the output capacitor to $2V_c$. Voltage error is applied to the sample and hold block and it is compared with actual current signal. The current error is applied to hysteresis block. The output of HC is given to a comparator which produces updated pulses for re-lift converter. The output voltage, current and power waveforms across R-load of HC-SRLCS are provided in Figure 3(e), 3(f) and 3(g) respectively. Their values are found to be 80V, 0.75A and 60W. The parameters used for simulation is given in Table 1.



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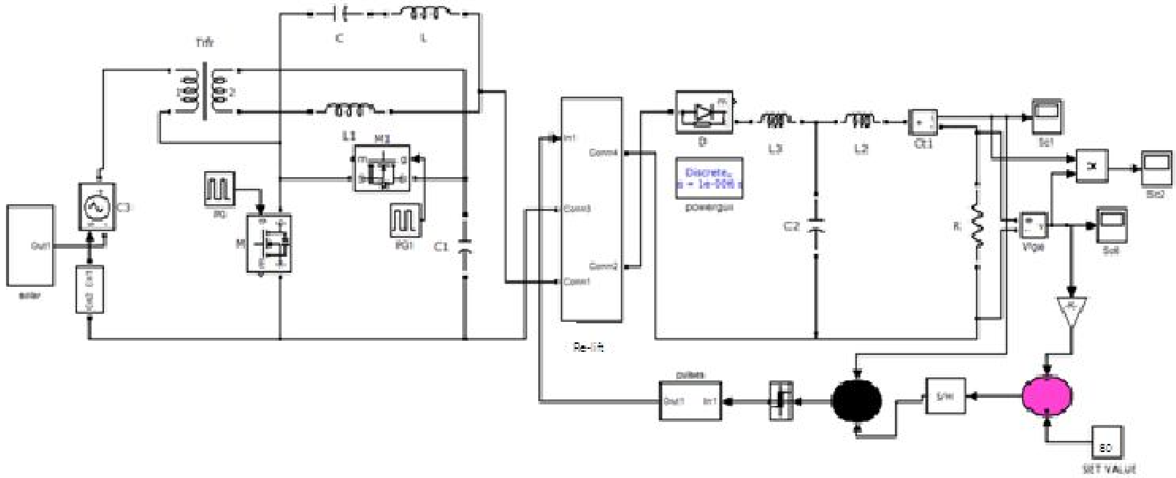

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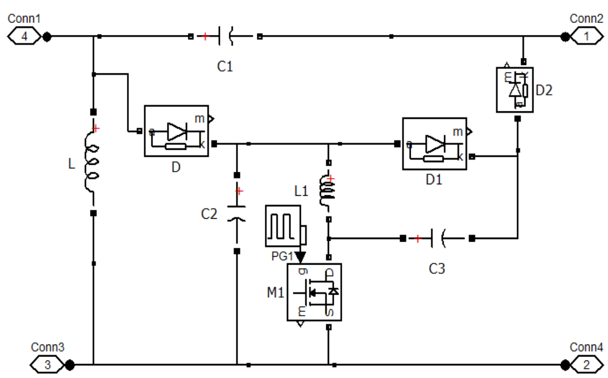

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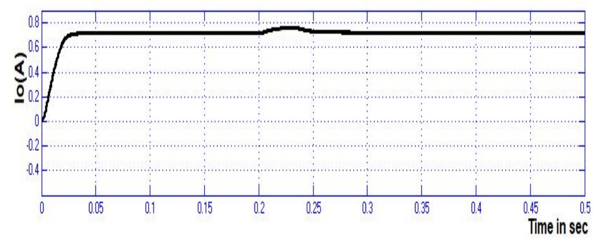

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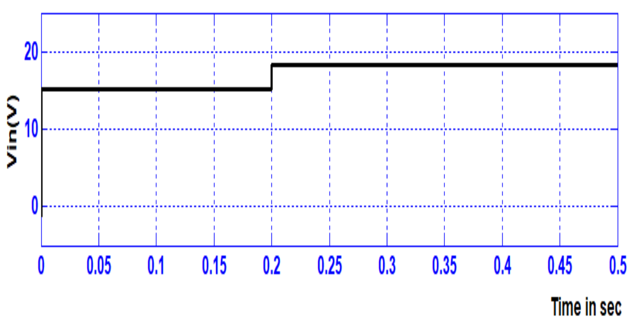

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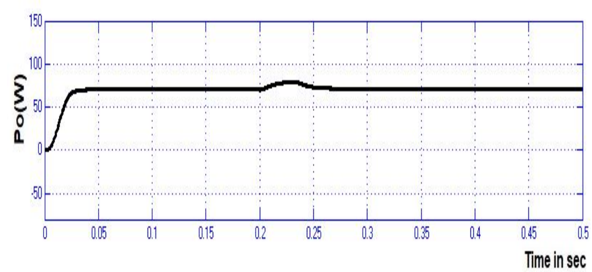

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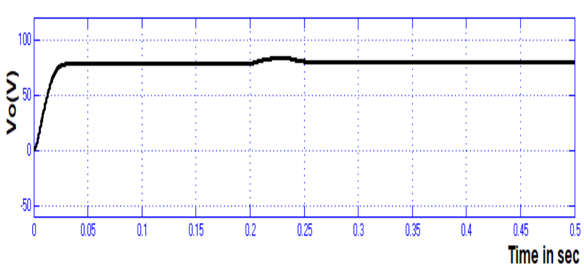


(e)

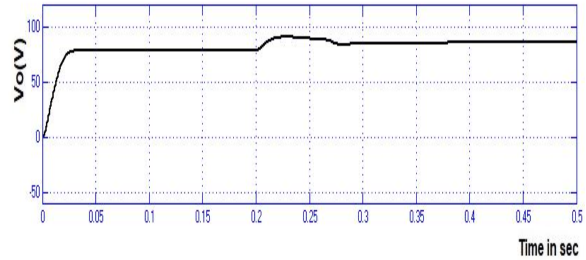
Figure 3: HC-SRLCS: (a) Simulink model (b) measurement of power in solar system (c) circuit of re-lift converter (d) output voltage across PV (e) output voltage (f) output current (g) output power

Table 1: Parameters used for simulation

Parameters	Simulation
L_1	35µH
C_1	6.6µF
C_2	100µF
R_L	100 Ohm
V_{in}	15-18V

3.2 PID and FOPID Controlled SEPIC Re-lift System

The Matlab Simulink model shown in Figure 3(a) is replaced with PID and FOPID controller. The sensed output of converter is compared with reference voltage and from which it is applied to PID/FOPID controllers. The comparator compares time based voltage with error and generates proper pulses to regulate output voltage. The closed loop simulation results with PID controller are provided in Figure 4(a), 4(b) and 4(c). FOPID controller results are shown in Figure 5(a), 5(b), and 5(c) respectively. Time domain parameters are compared with the results of fuzzy controlled RLCS system presented in [18] and it is given in Table 2. From Table 2, it is clearly evident that the time domain response is very much enhanced by using fuzzy scheme. The superiority of fuzzy controlled system is illustrated in bar chart which is given in Figure 5(d).



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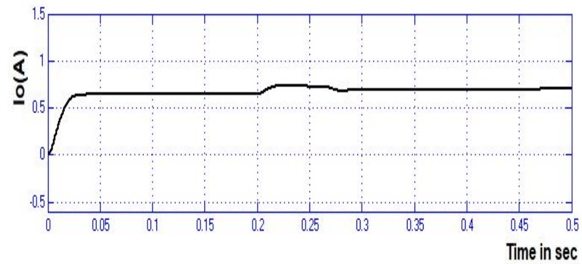

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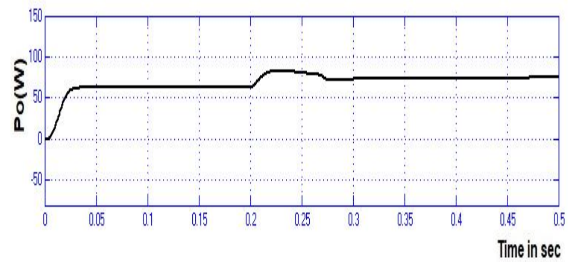
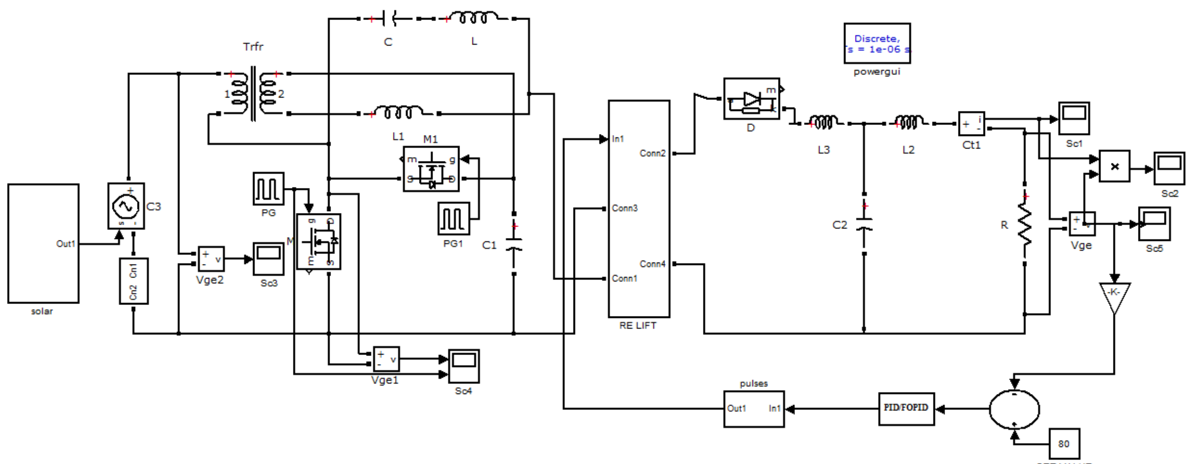
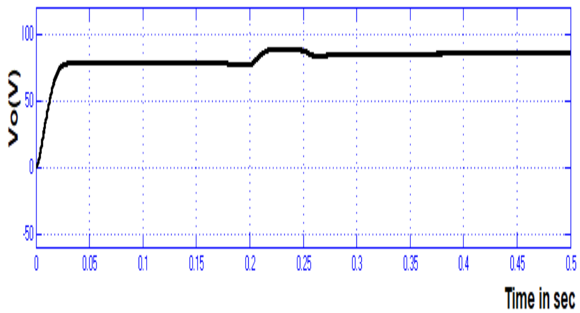


(d)

Figure 4: PID-SRLCS: (a) circuit diagram (b) output voltage (c) output current (d) output power



(a)



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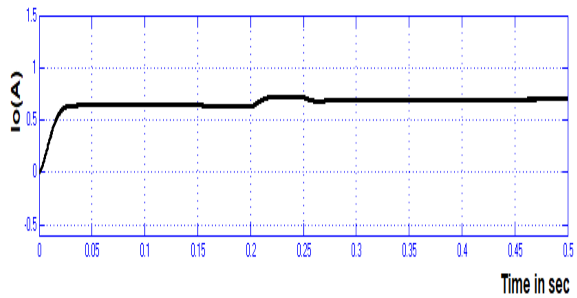

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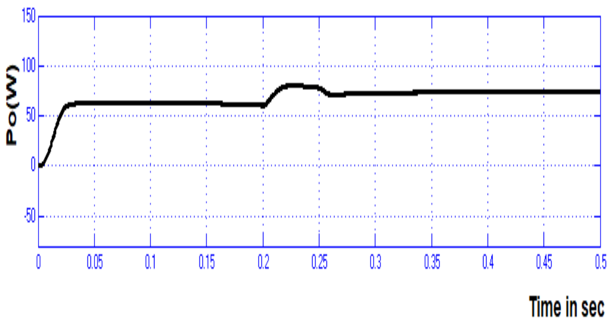

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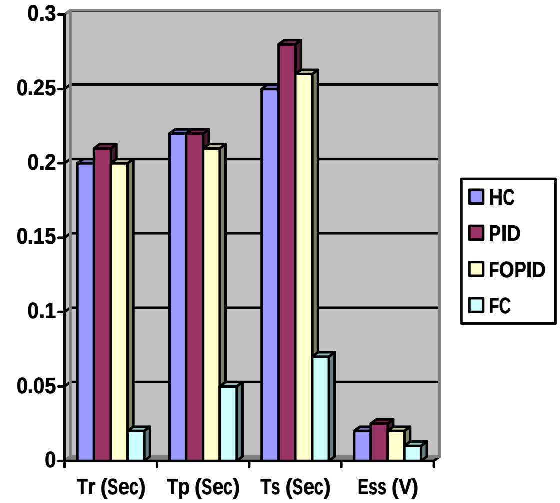

(d)

Figure 5: FOPID-SRLCS: (a) output voltage (b) output current (c) output power (d) bar chart

Table 2: Comparison of time domain parameters

Controller	T_r(Sec)	T_p(Sec)	T_s(Sec)	E_{ss}(Volts)
HC	0.20	0.22	0.25	0.02
PID	0.21	0.22	0.28	0.025
FOPID	0.20	0.21	0.26	0.020
FC [18]	0.02	0.05	0.07	0.01

4. CONCLUSION

Hysteretic, PID and FOPID controlled SEPIC re-lift converter system in closed loop are successfully designed and simulated. The results obtained are analyzed with the fuzzy scheme reported in the literature. Results confirm the superiority of fuzzy re-lift system. Hence, fuzzy controlled re-lift system is a viable alternative to the existing step-up converters. The only drawback of fuzzy system is its low power rating.

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