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A Novel Sensitive Rectifier with Increased Output Load Tolerance for Ambient RF Energy Harvesting

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ABSTRACT

This paper proposes a novel rectifier configuration with reduced output load sensitivity at the frequency of 2.45 GHz. The Harmonic Balanced (HB) and Source/Load pull analysis are utilized to find the optimum matching network under two different load values of 4.3 and 10 kΩ. All the simulations are performed using the commercially available software package Advanced Design System (ADS). A comparison between diffirent rectifier topologies, namely, half-wave, full-wave and a two stage voltage doubler is initially presented. A harmonic rejection filter (HRF) in the form of low pass filter is designed and placed at the input of the signal source to ensure the rejection of all the harmonics generated from the diodes. By providing such a condition, the generated harmonics are terminated and forced to participate on another cycle of rectification leading to increased efficiency of the overall system. The increased performance of proposed rectifier has been justified through the measurements validating the effectiveness of our approach. The efficiency of the rectifier is also evaluated over large output load from 1 to 12 kΩ.The measured results indicate an efficiency better than 40% over a large load range of 3 to 9 kΩ under both low and high incident power levels of -10 and 5 dBm, respectively. The maximum efficiency achieved is 61.9% occurring at 3 dBm. Moreover, even at the low power level of -20 an efficiency better than 13% has been achieved.

Key words: Energy harvesting, Rectifier, Output load tolerance, Harmonic termination, RF-DC efficiency

1. INTRODUCTION

This Wireless power transfer (WPT) and energy harvesting technology has recently attracted significant attention. Microwave rectifiers as of key component in WPT has extensively been used and studied.

Wireless power transmission (WPT) is generally done through four major techniques of inductive coupling, magnetically coupled resonance, microwave wireless power r transfer and distributed laser techniques [1]. Microwave wireless power transmission (MWPT) is the most popular method amongst all other aforementioned techniques as it allows for long-range power transmission. Rectifying antenna, also known as rectenna, is the most important module for MWPTand RF energy harvesting applications.

Microwave rectifiers has been designed with different configurations such as single series [2], single shunt [3], full-wave rectifier [4, 5] and even bridge rectifier [6]. Moreover, harmonic termination has been effectively used in both power amplifier and rectifier designs to improve the efficiency [5, 7, 8].

The resultant conversion efficiencies can be significantly affected when the load presented to the energy harvester varies, which is the case in real applications. Previous works are predominantly focussing on fixed output load value [5, 7, 8]. In this work we present a novel sensitive rectifier with increased output load tolerance using harmonic balanced analysis.

2. MATERIAL AND METHODS

The design of an efficient rectifier follows by determination of complex input impedance of the diodes which is a function of several variables such as power, frequency, harmonic termination and output load. Since, the values of junction capacitance and diodes inherent resistance is extremely non-linear, the analysis of the diodes must be performed under the large signal and HB conditions. In order

to have a better understanding about the performance of different rectifier topologies, a comparison is made between power conversion efficiency and DC output voltage of half-wave rectifier, full-wave and two stage voltage doubler for different output loads of 1 kΩ, 5 kΩ and 10 kΩ presented inFigure 1.

As is observed, the half-wave rectifier achieves its best performance under the low load condition (1 kΩ) with an efficiency better than 40% from -10 to 7.5 dBm. As the value of load increases to 5 kΩ, the efficiency drops at the high power levels while the efficiency at the low power levels increases. Under this condition the peak efficiency of 42.4% at -11 dBm is obtained. However, the efficiency is noticeably reduced for the output load of 10 kΩ in which the achieved efficiency becomes lower or equal to that of the voltage doubler all over the power levels. In oppose to a half-wave rectifier, both single and two-stage voltage doubler exhibit better efficiency performance for the high output loads, nonetheless, due to the lower loss caused by the increasing of the diodes, the voltage doubler outperforms the two-stage rectifier particularly at the low power levels. A summary of different rectifier topologies and their performance is given inTable I.

A. Rectifier Topologies

There are various topologies for the design of rectifiers based on the number of rectifying element used. Some of the common rectifier topologies employed for energy harvesting applications are shown in Figure 2 . A half-wave rectifier has a simple structure consisting of a single diode, a DC pass capacitor and a load resistor. Figure 2(a) and Figure 2(b) demonstrate the two possible configurations of half-wave rectifiers. Owing to the employment of only a single diode, half-wave rectifiers possess the lowest possible loss during the rectification process. Although, theoretically, half-wave rectifiers are limited to a maximum efficiency of 50% (as it passes only a half cycle of the input voltage), at the high frequencies such as microwave range of frequency, the efficiency is significantly increased and it can be treated as a resonant structure. However, despite the fact that RF signal in a half-wave rectifier experiences less losses, there is a large amount of harmonics generated on the circuit. These harmonics have to be terminated for achieving high conversion efficiency which can lead to a significantly large footprint of the overall circuit. On the other hand, considering the typical DC voltage requirement of available low power ICs in the market (typically 0.35-3.5V), the limited supplied voltage by a single diode may not be sufficient. In another words, the issue is not only how efficient a wireless energy harvester is in converting RF-to-DC power, but also what the output DC voltage and current of the energy harvester are at the RF input power level. As a consequence, voltage multipliers in the form of a full-wave voltage doubler (Figure 2 (c)) or a cascade of several stages as well as bridge rectifiers (Figure 2(d)) are used to provide sufficient output power determined by the intended application. Moreover, rectifiers with bridge topologies have also been used for energy harvesting applications. However, when compared to the bridge rectifier, multi-staged voltage doubler may provide additional degree of freedom for the low power operation.

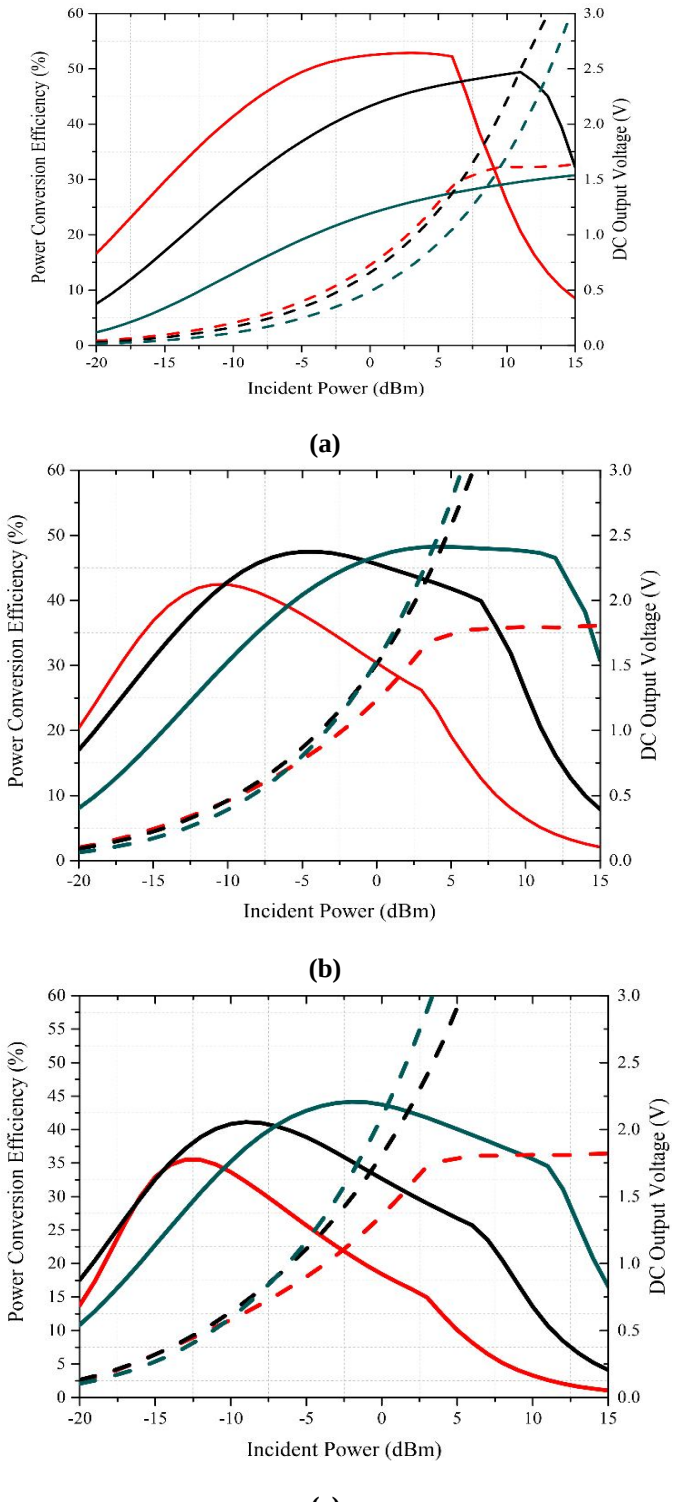


Figure 1: Power conversion efficiency (solid line) and DC output voltage (dashed line) for the output loads of: (a) 1 kΩ, (b) 5 kΩ, (c) 10 kΩ. Half-wave rectifier (red), full-wave rectifier (black) and two-stage voltage doubler (green).

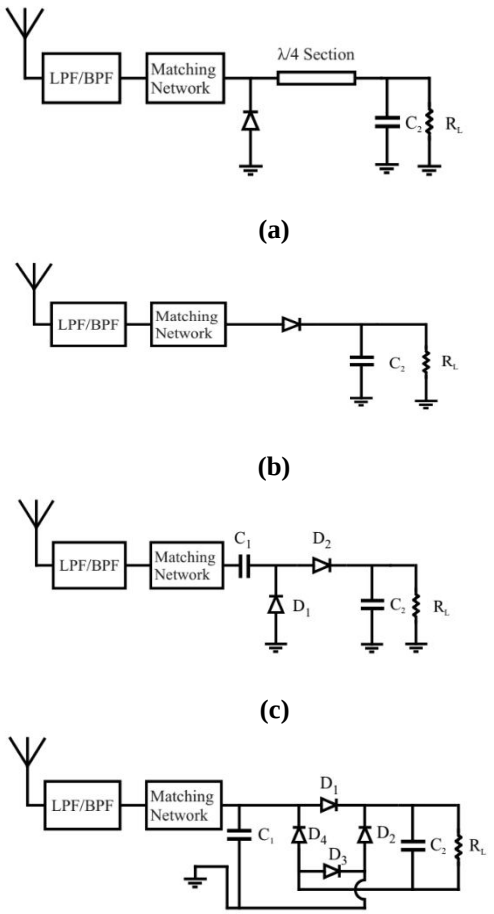


Figure 2: Common rectifier topologies, single shunt (a), single serial (b), voltage doubler (c) and bridge rectifier (d)

Table I: A summary of the performance of rectifier with different topologies. All rectifiers are matched to -15 dBm

Rectifier Topology	R_L (kΩ)	Maximum Efficiency @ dBm	DC Voltage (mV) @ -20 dBm	DC Voltage (mV) @ -10 dBm	DC Voltage (mV) @ 0 dBm
Half-wave rectifier	1	52.85 @ 3	40	203	724
	5	42.4@ -11	100	460	1232
	10	35.5@ -13	117	580	1358
Full-wave rectifier	1	49.4@ 11	27	166	657
	5	47.4@ -5	92	462	1509
	10	41.1@ -9	132	640	1807
Two-stage Voltage doubler	1	30.7@ 15	15	114	488
	5	48.2@ 4	63	390	1529
	10	44.1@ -2	104	593	2091

B. Rectifier Design

Figure 3 provides a depiction of a simple RF energy harvesting receiving end. As is observed, it composed of a receiving antenna that captures the power from the ambience. The collected power passes through a matching network to a rectifier circuit where the power is converted into usable DC form. The provided DC power is then used to drive a device or conserved into a storage element for a later usage.

An important factor for the design of microwave rectifiers at the low power levels is diode in which a diode with low built-in voltage is more preferred.

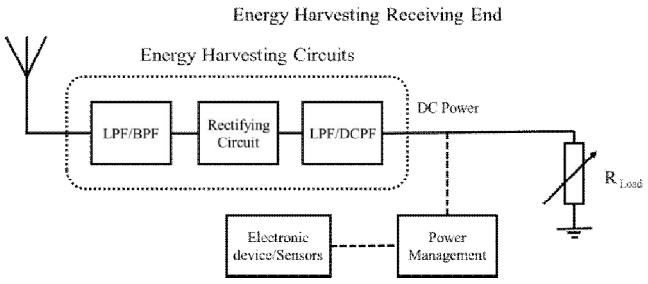


Figure 3: General block diagram of energy harvesting receiving end

On the other hand, Source/Load pull simulation provides rich information for the designers in which the simulator iteratively sweeps the magnitude and phase of the port at the given power and frequency, where the values of current and voltages at each node is iteratively calculated. The resultant DC output voltage is then determined for the corresponding DC output power and the efficiency contours are plotted on the Smith chart where the region of maximum efficiency can be determined.

In order to initiate the Source/Load pull simulation, a DC pass filter from quarter-wavelength resonating stubs are designed to provide short up to 6th order harmonics as can be seen in
Figure **4**. The DC filter used here exhibits good harmonic termination characteristic in which the first quarter-wavelength stub achieves short circuit at the fundamental, and all odd harmonic frequencies where the second resonating stub (λ / 4@2 f_0) provides short at any frequency that is the odd multiple of the second harmonic. The DC filter used here, is capable of providing continues termination up to 7^{th} harmonic. The simulated harmonic terminating characteristic of the designed DC pass filter for the first five harmonics is illustrated in
Figure **5**. The advantage of employing the DC pass filter is to prevent the generated harmonics while protecting the output device.

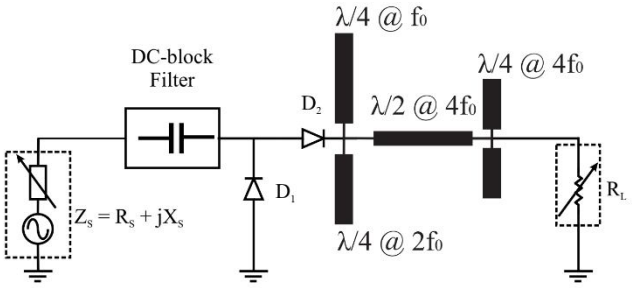


Figure 4: The basic test setup used for the source/load pull simulation in ADS software

It can be seen that, the first four harmonic frequencies present decent shorting termination to the incoming signal while the fifth termination is slightly inductive (0.018 + j0.06 Ω). However, this value of termination is adequate as the harmonic power generated at fifth harmonic is fairly small.

Figure **6** demonstrates the efficiency contours obtained for the efficiency higher than 40% at different power levels. It is observed that the efficiency contours under the medium load condition (4.3 kΩ) presents a much larger efficiency region when compared with that of higher load (10 kΩ) which can greatly simplify the design of matching network. Moreover, for a high load value it can be noticed that, the efficiency contours are not harmonized that reduces the possibility of achieving high RF-to-DC conversion efficiency over large power dynamic range. This effect can be better shown by plotting the two graphs on the same Smith chart as shown in Figure 7.

As is seen, there are several possible scenarios where some important matching regions are highlighted. It can be noticed that, if a matching network is properly designed within the region (A), it can provide power conversion efficiency better than 40% for the power range of -10 to 5dBm under the output load value of 4.3 kΩ.

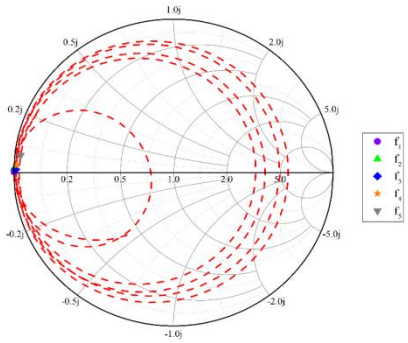
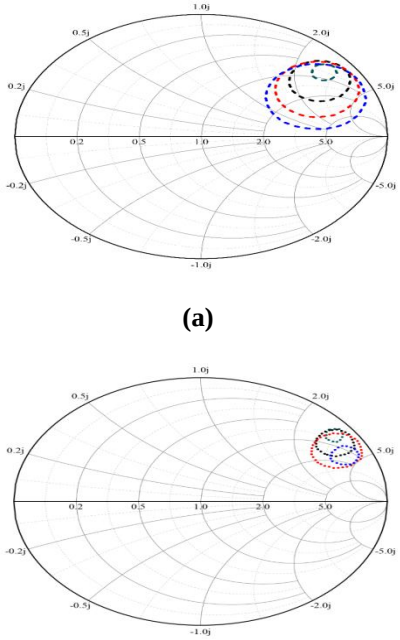


Figure 5: Simulated harmonic terminating characteristic of the DC-pass filter

Same condition applies for region (B) and (C) where the power conversion efficiency better than 40% can be obtained from -5 to 5 dBm and -10 to 0 dBm, respectively. There are also, two important regions that encompass wide dynamic range for both output load cases denoted as region (E) and region (D) that can provide matching for the high and low power levels, respectively. Notice that the region (D) is the overlap of region (C) and (A).

The simulated power conversion efficiency by providing the matching condition at region (E), (D) and (F) are plotted in Figure **8**. As is observed, for the rectifier matched at region (E), the highest efficiency of 73.6% has been obtained for the power level of 5 dBm. However, while the efficiency remains high for the power levels above. -5 dBm, it significantly reduces as the power level drops to -10 dBm. On the other hand, the rectifier matched to region (F) shows the worst performance, since the rectifier can only provide acceptable efficiency within a very limited output load for all power levels. Lastly, the rectifier matched at region (D) exhibits the best performance for the operation at low power levels for various output load values which is very suitable for energy harvesting applications. However, the efficiency obtained is not entirely satisfactory.

A further investigation into the rectifier performance reveals the high value of harmonics generated by diodes at the input terminal. Hence, a harmonic rejection filter (HRF) in the form of low pass filter is designed and placed at the input of the signal source to ensure the rejection of all the harmonics generated from the diodes. By providing such a condition, the generated harmonics are terminated and forced to participate on another cycle of rectification leading to increased efficiency of the overall system.



(a)

(b)

Figure 6: The efficiency contours obtained from source/load pull analysis to realize efficiency higher than 40% for the load values of: (a) 4.3 kΩ and (b) 10 kΩ. The dark cyan, black, red and blue colour lines indicate the power levels of -10, -5, 0 and 5 dBm, respectively.

The configuration of the designed rectifier is shown in Figure 9. A co-simulation is then performed to make sure that all the circuit component performance including the substrate and metal losses of the overall circuit have been taken into account. The simulated performance of proposed rectifier and the rectifier without HRF are shown in Figure **10**.

Table II: The Optimal Dimensions of the Designed Rectifier

Parameter	Length (mm)	Parameter	Length (mm)
L_1	3.06	L_8	7.8
L_2	2.85	L_9	19.09
L_3	4.46	W_f	1.18
L_4	4.68	W_1	0.49
L_5	7.7	W_2	0.3
L_6	6.05	W_3	1.18
L_7	6.04		

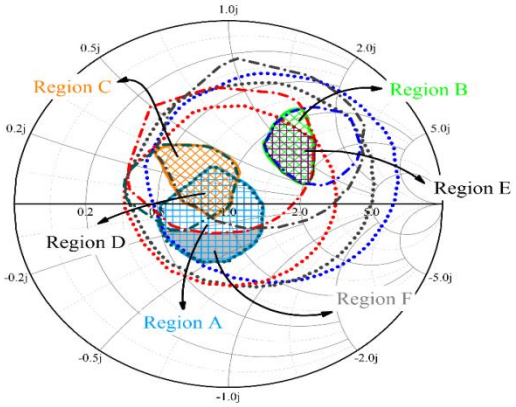


Figure 7: Simulated 40% efficiency contours for the output values of 4.3 kΩ (dotted lines) and 10 kΩ (dash-dotted lines). For the better demonstration, the values are normalized to Z0 × (0.8 – j2.81) on the Smith chart. The dark cyan, dark gray, red and blue colour lines indicate the power levels of -10, -5, 0 and 5 dBm, respectively

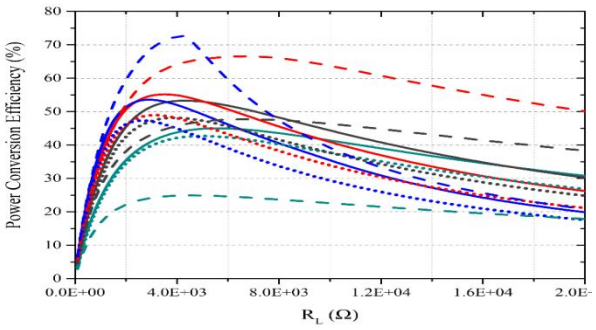


Figure 8: Simulated power conversion efficiency as a function of output load value . Dashed lines (Matched at Region (E)), Solid line (Matched at Region (D)), Dotted lines (Matched at Region (F)), The dark cyan, dark gray, red and blue colour lines indicate the power levels of -10, 5, 0 and 5 dBm, respectively

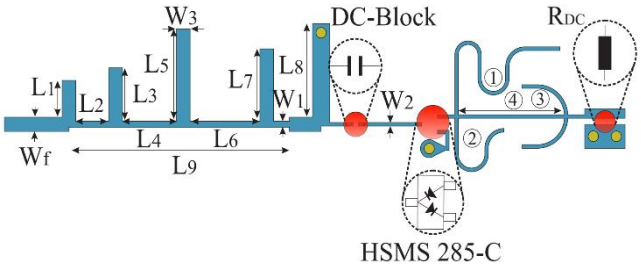


Figure 9 : The rectifier design

The conversion efficiency is calculated following expression

$$\eta_{rec}(\%) = \frac{P_{DC}}{P_{inc}} \times 100 = \frac{V_{DC}^{\ 2}}{R_L \times P_{inc}} \qquad (1)$$

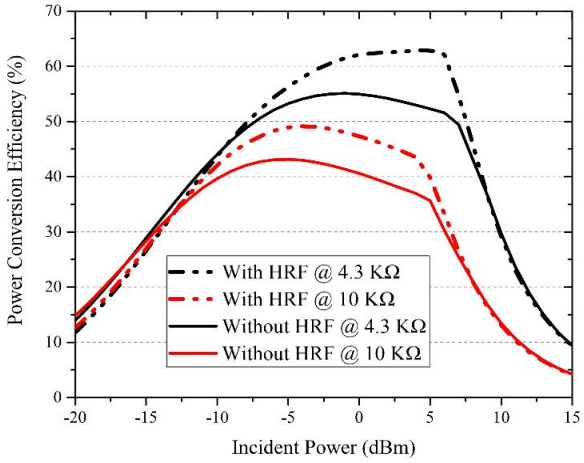


Figure 10 : Comparison between the simulated results of modified rectifier and the rectifier without HRF

where P_{inc} is the incident RF power and V_{DC} is the rectified output voltage measured across the output DC load (R_L). It can be seen that, the efficiency of the proposed rectifier is significantly improved particularly at the power levels above -10 dBm and reaches to 62.9% at the 5 dBm which is almost 10% higher than that of rectifier without HRF.

3. RESULTS AND DISCUSSION

The proposed modified rectifier is fabricated on a 20-mil-thick RO4003C substrate with a relative permittivity of 3.38 and loss tangent of 0.0029. The photograph of fabricated modified rectifier is depicted in Figure 11.

The simulated and measurement S_{11} of the modified rectifier are demonstrated in Figure 12. It can be seen that, the measured resonant frequency is about 2.44 GHz with an impedance bandwidth of nearly 255 MHz from 2.3 to 2.55 GHz. Good agreement between the simulation and measurement has been achieved validating the effectiveness of the method used. The simulated and measured RF-to-DC

power conversion efficiency and achieved output voltage are presented in Figure 13.

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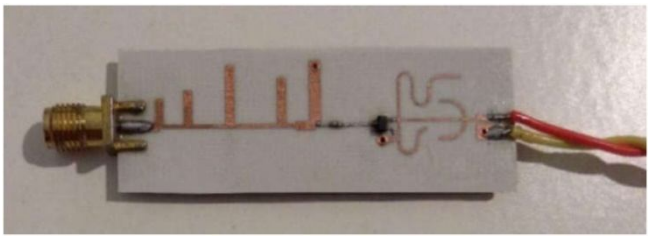

Figure 11: The fabricated rectifier

As is seen, the achieved efficiency of the proposed design is significantly improved with the maximum efficiency of 61.9% occurring at the 3 dBm. It is worth noting that, even at the low power level of -20 dBm, the efficiency remains above 13% where the output voltage is 76 and 120 mV for the load values of 4.3 and 10 kΩ, respectively.

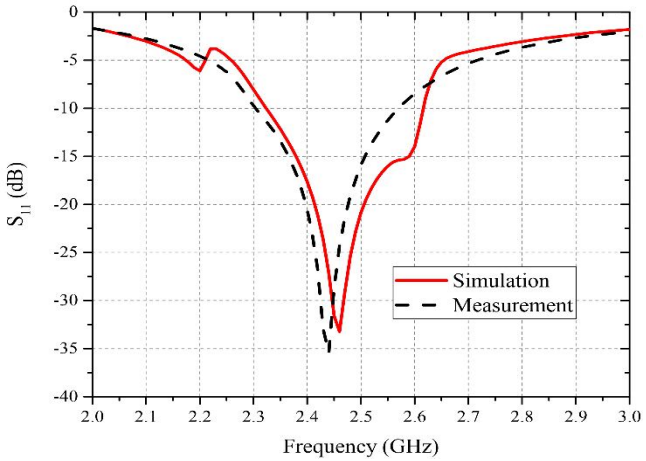

Figure 12: S_{11} of the rectifier for input power -10 dBm and load of 4.3kΩ

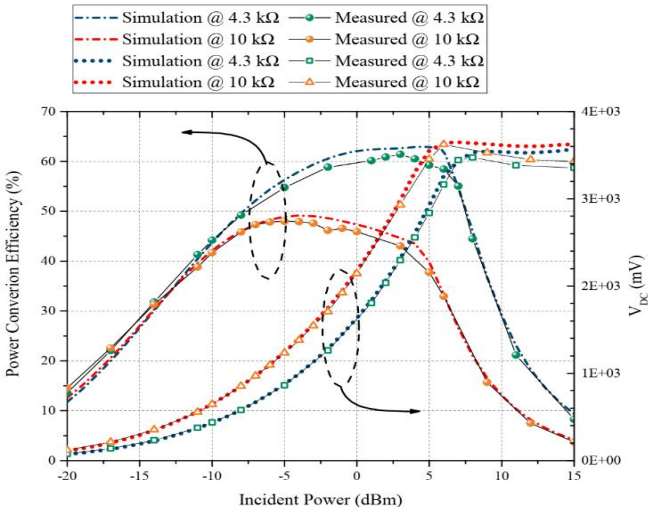

Figure 13: Power conversion efficiency of the rectifier

Moreover, the efficiency of the rectifier is also evaluated by varying the value of output load from 1 to 12 kΩ as demonstrated in Figure 14. It can be observed that, the measured values follow well the simulation at the lower power level (-10 dBm) where diode behaviour is relatively linear. The measured efficiency remains better than 40% over a large load range of 3 to 9 kΩ under both high and low incident power levels of -10 and 5 dBm, respectively. The efficiency better than 40% for the 10kΩ case is ranging from 3 kΩ to 11 kΩ while the same condition occurs from 1 to 9 kΩ when the load condition is altered to 4.3 kΩ. However, it can also be noted that, as the power level increased to 5 dBm, the diode is pushed more into non-linear state and the matching condition is reduced.

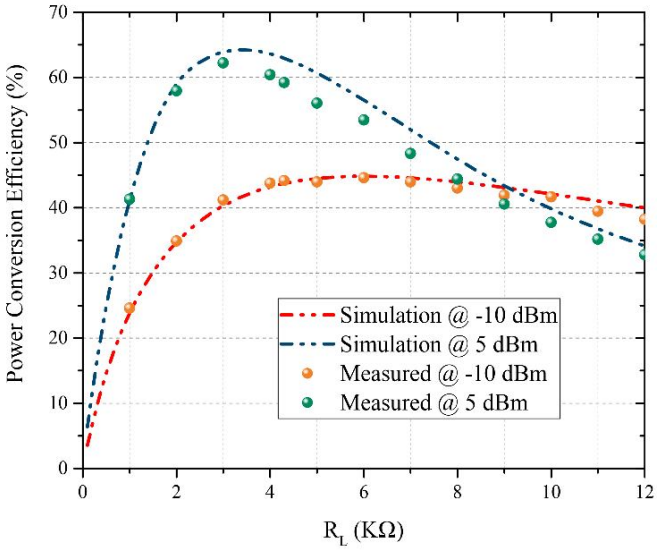

Figure 14: RF-to-DC power conversion efficiency of the modified rectifier as a function of output load R_L

4. CONCLUSIONS

A novel and sensitive rectifier with increased output load tolerance is presented in this work. The harmonic analysis is performed to determine the optimum matching region. In order to further improve the efficiency, an HRF has been employed. The increased performance of proposed rectifier has been justified through the measurements validating the effectiveness of our approach. The results obtained from the fabricated rectifier showed that for a load range of 3 to 9 kΩ the efficiency are observed to be 40% or better both for high and low incident power levels of -10 and 5 dBm, respectively. The maximum efficiency achieved is 61.9% occurring at 3 dBm. Moreover, at -20 dBm, the efficiency remains above 13% where the output voltage is 76 and 120 mV for the load values of 4.3 and 10 kΩ, respectively.

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