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Design of High Speed Single Ended 6T and 8T SRAM Cells

O.Mohanachandrika[1]*, Dr.M.Siva kumar[2]
[1] PhD scholar dept of ECE, KL University,Green Fields, Vaddeswaram, Guntur DT, A.P INDIA
[2] Associate Professor Dept of ECE KL University,Green Fields, Vaddeswaram, Guntur DT, A.P INDIA
mohana.chandrika@gmail.com, siva4580@kluniversity.in

ABSTRACT

In this brief, the new architectures of Single ended 6T SRAM and Single ended 8T SRAM with virtual ground are presented, that are used to avoid the reliability and stability issues of SRAM cells. In the proposed 8T SRAM design, the virtual ground technique is used to weaken the positive feedback mechanism thus improving the writeability of SRAM cell. Moreover a single ended 6T SRAM has been proposed which works faster when compared with conventional one. Also the proposed circuits don't require any circuits related to the pre-charging of read operation. The proposed architectures isolates the storage nodes from the read bit lines which inturn increases the read stability and eliminate read upset. In this work we have investigated the power dissipation and delay parameters in conventional and proposed methods and compared them. From the comparison, it is evident that there is significant increase in the performance of proposed methods in terms of power and delay.

Key words: Single ended SRAM, 6T SRAM, 8T SRAM, 10T SRAM, Virtual ground, power dissipation, and delay.

1. INTRODUCTION

Across the board utilization of mobile phones and hand-held devices, combined with the accessibility of fast communication systems, has brought about an exponential interest for sight and sound administrations on the system. Structuring vitality productive frameworks for longer battery life is one of the vital targets in such gadgets. High goals imaging in these hand-held gadgets has additionally exacerbated the issue of intensity utilization because of expanded handling and capacity prerequisites. Truth be told about 30% power utilization is accounted for to be in implanted static random access memory (SRAM) alone [1]. The dynamic power utilization has a quadratic reliance on voltage, and recollections are intended to work at ultra-low voltages to acquire critical power decreases in memory activities. Decrease in supply voltage, be that as it may, hinders the memory tasks and builds the bit error rate (BER) essentially [2]. While this is one of the real bottlenecks in utilizing such recollections in mainline processors, it is worthy in processors worked for interactive media applications as these are known to be tolerant to errors [3].

High density and Low-power designs have turned out to be progressively basic for different applications because of the developing requests for greater usefulness at higher energy efficiency, especially in cell phones and wireless devices. With the expanding requests for higher memory limit and speed, it has turned out to be basic to guarantee lower control utilization and higher dependability at a quicker speed for the individual memory cells and in general memory framework. Recollections structure an expansive piece of any framework, and the general framework execution is intensely subject to the memory. Different procedures are utilized to diminish power consumption and improve noise margin in the design of memory, which incorporate circuit partitioning, double threshold voltage scheme, expanding the thickness of the gate oxide for noncritical circuits, and a lot more [1]-[4]. In addition, the virtual ground scheme is utilized to upgrade the writeability of cell. The proposed circuit is a lot more straightforward and vitality proficient with respect to plan, execution, and task. Installed recollections are unavoidable in modern VLSI system and system on-chip (SoC) designs. Current embedded memories are overwhelmed by the 6-transistor (6T) SRAMs on account of their ideal installed characteristics: logic CMOS compatibility, rapid and low power activity. They are utilized in various sizes running from a couple of kilobits to a couple of hundred megabits, and possess a substantial territory in present day SoCs. Nonetheless, with scaling of CMOS innovation, the SRAM soundness at ultra-low supply voltage has turned into a vital issue for wearable framework applications.

Section II gives a short overview of the current SRAM designs. Section III shows the proposed SRAM cell circuits, which can possibly defeat numerous constraints of the conventional SRAM designs. Section IV examines the simulation results of the proposed 6T and 8T SRAM At long last, Section V finishes up the paper with a concise review of our continuous and future work.

2. REVIEW OF EXISTING SRAM DESIGNS

In this section various existing architectures of SRAM are discussed.

2.1. Conventional 6T SRAM

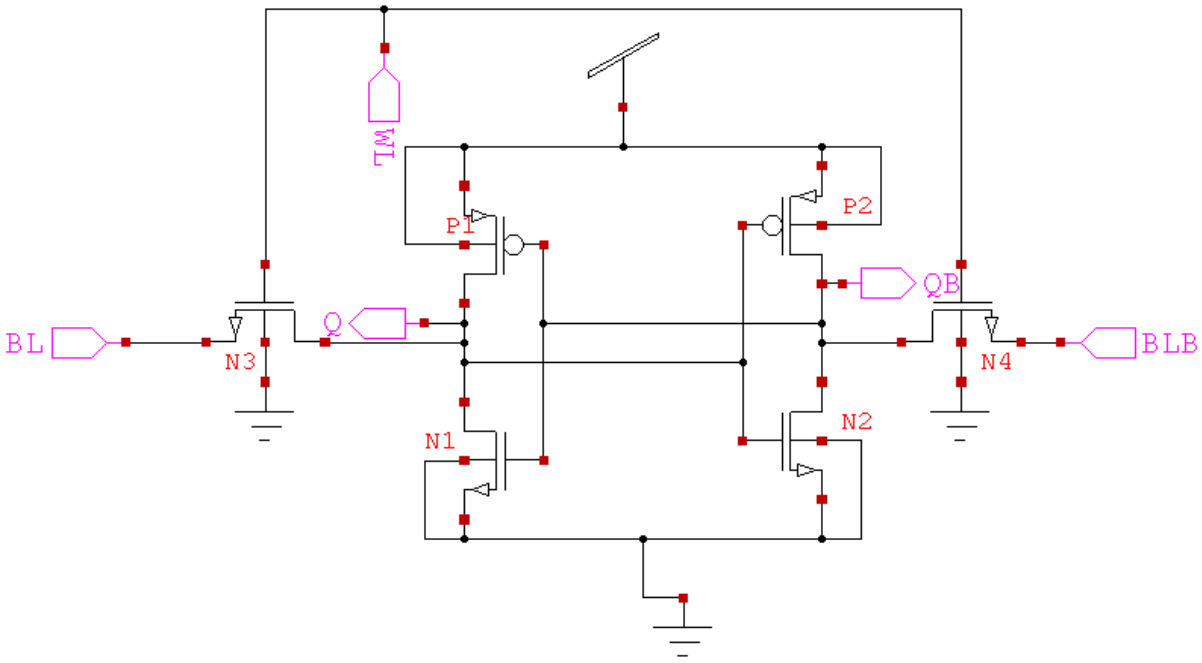

Figure 1: Schematic circuit of Conventional 6T SRAM

The conventional 6T SRAM cell is depicted in Figure 1 has been the industry standard from the introduction of the SRAM [5, 6]. Dependable read and write activities are the key consideration in SRAM design. Because of the simplicity and symmetry of the 6T SRAM cell circuit, it is very effective. In any case, double bit line scheme of 6T cell, the bit lines are not electrically isolated from the output storage nodes during read and write activities. The SRAM cell is exceptionally helpless against the noise during the read operation. The voltage at the storage node with "0" ascends to a higher voltage than ground because of voltage division along access (N3, N4) and pull down (N1, N2) transistors, amidst pre-charged bit lines (BL and BLB) and the ground terminal of the SRAM cell. This circumstance may finish up with perusing a wrong value, generally known as read upset. The regular 8T SRAM is acquainted with defeat this confinement.

2.2. Conventional 8T RAM

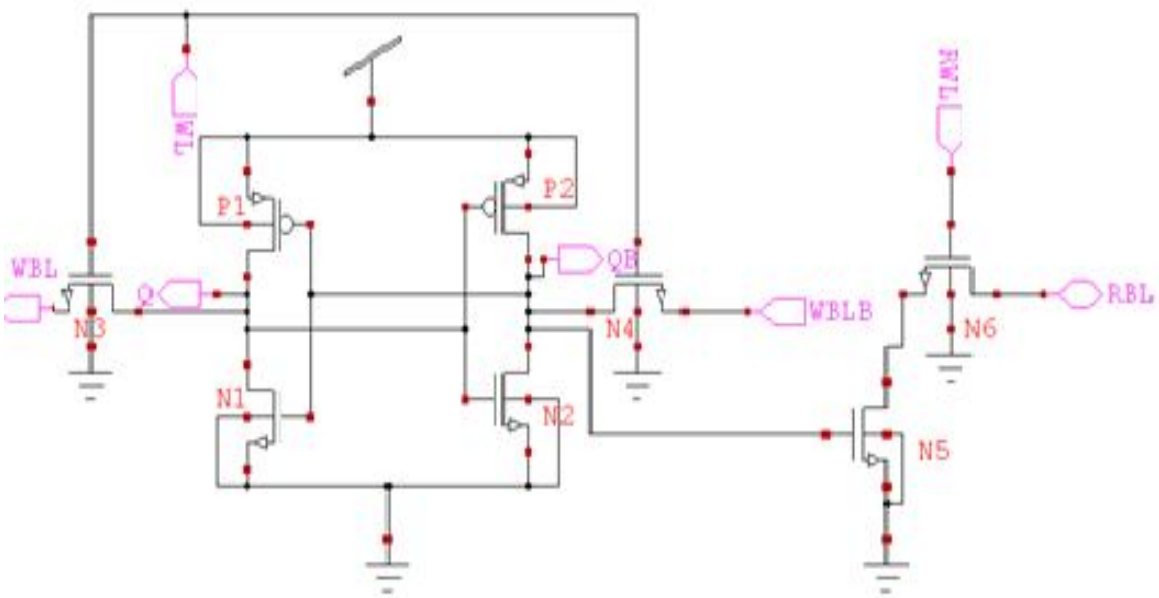

Figure 2: Schematic circuit of Conventional 8T SRAM with Dual Port

In 8T SRAM, two extra stack transistors (N5, N6) give access to the cell through the extra Read bit-line (RBL) as appeared in Figure 2. It has two dedicated word-lines (WL and RWL). Everything else is like the standard 6T SRAM. The reading task of 8T SRAM is isolated from the remainder of the cell, which expands the read static noise margin (RSNM). Higher noise margin edge guarantees better perused steadiness and strength. The read task of 8T SRAM does not irritate the capacity information of cell. The execution of the 8T SRAM amid the read task is dictated by the quality of the read stack transistors [6, 7].

2.3. Conventional 10T SRAM

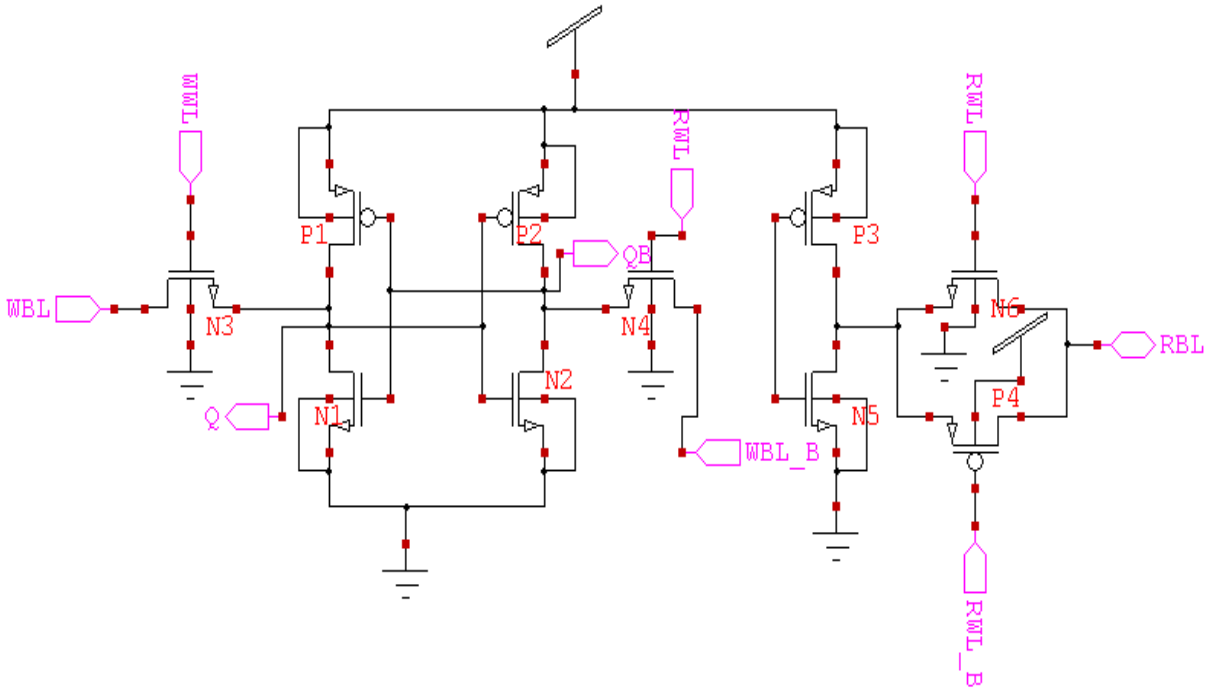

Figure 3: Schematic Circuit of Conventional 10T SRAM cell

The conventional 6T and 8T SRAM structures require pre-charging of the bit-lines amid the read task. This pre-charging forces serious vitality and timing imperatives on the structure and activity of high-thickness and high-limit SRAM applications. Figure 3 demonstrates the circuit of a non-pre-charge 10T SRAM with a read bit-line BL. It is a mix of the traditional 6T SRAM cell, an inverter, and a transmission gate. Read word line (RWL) controls the NMOS transistor (N4) at the transmission gate and RWL_B controls the PMOS transistor (P4) at the transmission gate. Once RWL and RWL_B are activated, the transmission gate is triggered, and the storage node is to RBL through the inverter. In 10T SRAM structure, the pre-charge hardware is dispensed with, in light of the fact that the inverter completely charges/releases the RBL. The RBL expends no power if recently arrived information is like the past state. Along these lines, 10T single-finished SRAM cell devours no extra power if sequential "0"s or "1"s are perused out. The charge and release powers are possibly devoured if the readout information is unique in relation to the past state. The transient likelihood on RBL is half for 10T single-ended SRAM in a grouping of irregular information, along these lines decreasing force utilization altogether amid the read task [5]. Notwithstanding, extra gadgets and required wirings force higher region overheads contrasted with 8T SRAMs [7, 8].

3. PROPOSED SRAM

In this paper, we have, designed a single ended 6-T SRAM cell and a single ended 8T RAM cell with a virtual ground. In SRAM memory, the majority of the power is consumed by charging and releasing of the bit-lines [10]. Since, our proposed SRAM cell utilizes just single bit line for read and single bit line for write it expends just half of the power when contrasted with traditional 6-T SRAM cell. In this work, we discuss about the proposed 6T SRAM cell and 8T SRAM Cell, investigate its write and read failures and contrast with traditional architectures of SRAM cell discussed so far.

3.1. Proposed 8T SRAM cell with Virtual ground:

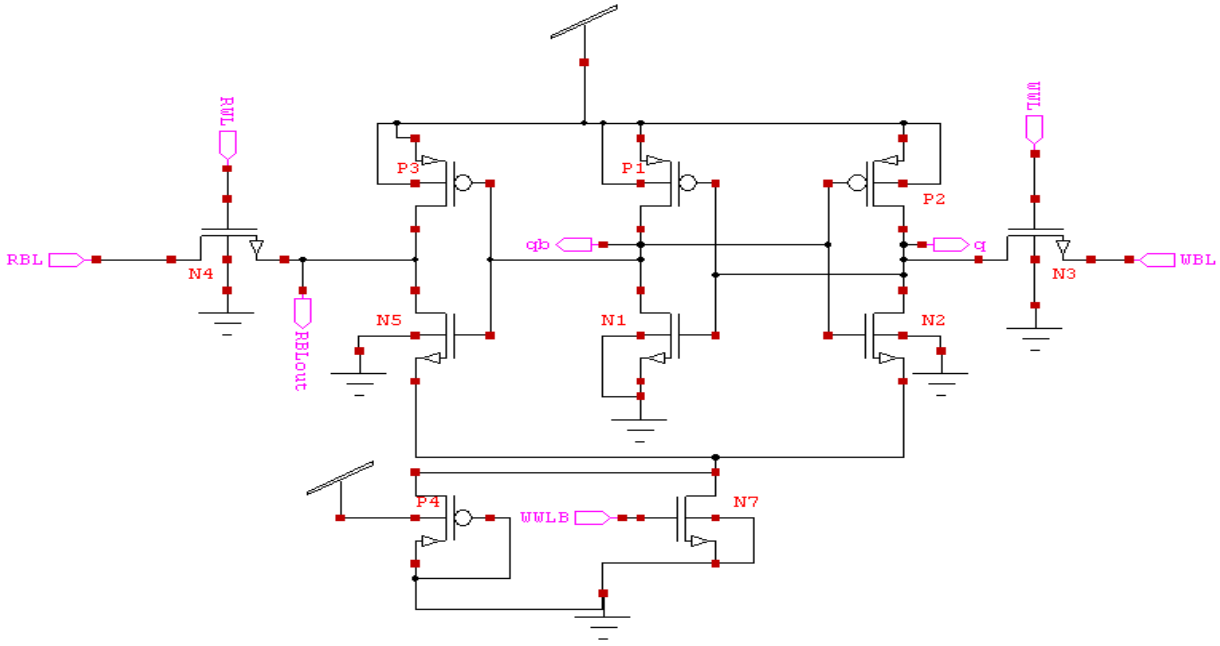

Figure 4: Proposed Circuit architecture of 8T SRAM with Virtual ground

The proposed 8T SRAM utilizes single-ended write and read operations. The proposed 8T SRAM cell offers resistance against the read upset about utilizing the inverter (P3-N5), which confines the storage node (QB) from the RBL in the proposed circuit, as appeared in Figure 4. Hence, the readout of the storage node QB can be performed without exasperating the stored data. In the ordinary 6T SRAM cell two bitlines (BL) and single word line (WL) are utilized during the write and read operations. In the proposed 8T SRAM structure as it were one BL and one WL are utilized prompting lower power consumption during the write and read tasks. The proposed configuration offers higher read strength and writeability. The architecture takes out pre-charging circuit, as the inverter completely charges/releases the read bit-line (RBL). As a result, a critical decrease can be accomplished in power utilization. The ordinary 6T and 8T SRAM cells require pre-charging of the bit lines during the read task that further expands the power utilization of the memory cell.

a. Write Operation of Proposed SRAM

Rather than the 6T cell, the proposed method is single ended architecture with virtual ground. During the write operation, write bit line (WBL) and write word line (WWL) are activated while read word line (RWL) is deactivated. The access transistor N3 is on while N4 is OFF of the fact that RWL is deactivated. Subsequently, the write task is isolated from the read activity. Also, a virtual ground is utilized to improve the writeability of cell by debilitating the positive feedback connection of inverters (P1-N1, P2-N2). During hold and read activity, the virtual ground(P4-N7) node is associated with the ground to hold the stored information in positive feedback. The hold condition of the proposed designed is like 6T SRAM cell. Be that as it may, during the write task, the virtual ground node is associated with the source of PMOS transistor (P4) as appeared in Figure 4. Since PMOS is a bad pull down device, this debilitates the positive feedback mechanism and writes activity is done effectively. Let us consider Q is at first at "1" and we need to compose a "0" into the cell. The write task starts once WWL is active. At that point WBL is set to zero to state "0". When Q falls low, QB gets high as a nature of positive input.

b. Read Operation of Proposed SRAM

During the read operation, just RWL is initiated, while WWL and WBL are deactivated. The read activity is isolated from the writing part, as WWL and WBL are deactivated, and transistor N3 is off, while N4 is activated. The storage node QB is confined from the RBL. Along these lines, the value stored at QB isn't aggravated, which builds the read static noise margin (RSNM).

3.2. Proposed 6T Single Ended SRAM cell

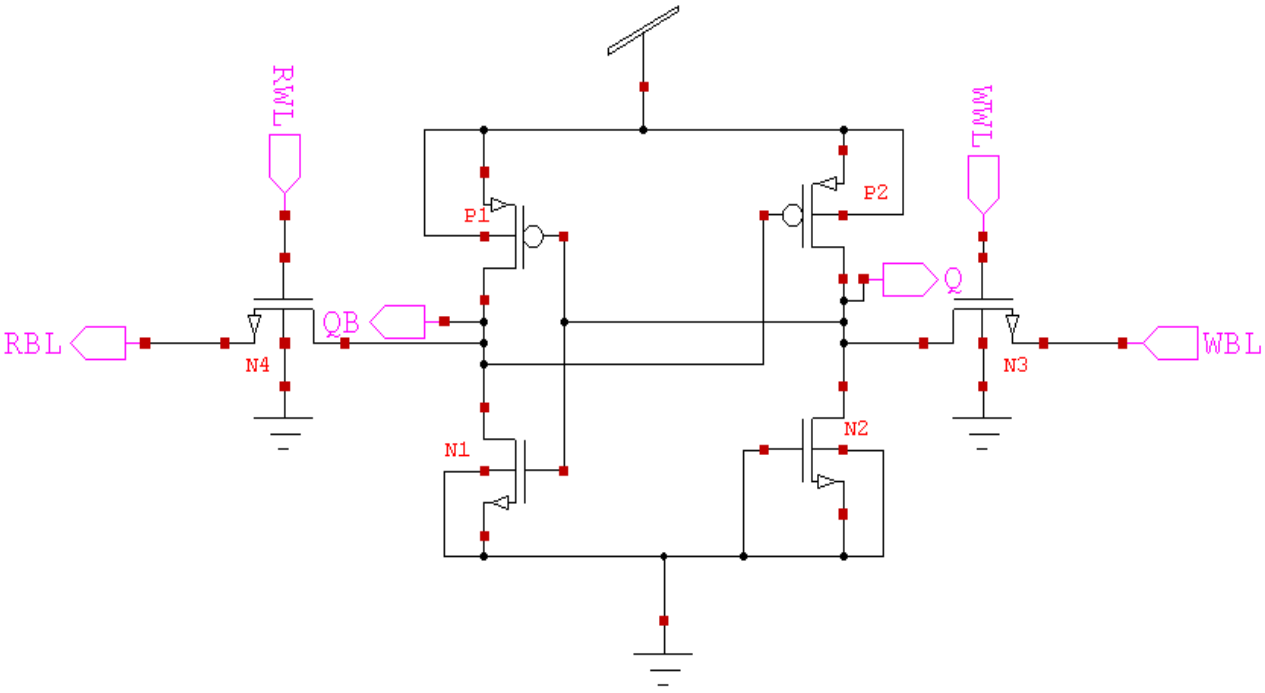

Figure 5: Proposed architecture of Single Ended 6T SRAM Cell

Here the architecture of Single ended 6T SRAM cell is depicted which is shown in figure 5. The proposed SRAM cells have improvement in one or more aspects of read and write stability when compared with existing or conventional architectures. The proposed circuit is an extension work of 7T SRAM cell. In this circuit, Transistor N2 will be always in the cut-off region because gate is connected to ground. This helps in reducing the contention between N2 and P2, thus increases write margin.

3.2.1. Write Operation of Proposed SRAM

During the write operation, write bit line (WBL) and write word line (WWL) are activated while read word line (RWL) is deactivated. The access transistor N3 is on while N4 is OFF of the fact that RWL is deactivated. Subsequently, the write task is isolated from the read activity. The data input at the Write Bit Line (WBL) will be stored at the storage node. Due to the feedback mechanism the output at the storage node QB is reverse to the data at Q. Let us consider Q is at first at "1" and we need to compose a "0" into the cell. The write task starts once WWL is active. At that point WBL is set to zero to state "0". When Q falls low, QB gets high as a nature of positive input.

3.2.2. Read Operation of Proposed SRAM

During the read operation, just RWL is initiated, while WWL and WBL are deactivated. The read activity is isolated from the writing part, as WWL and WBL are deactivated, and transistor N3 is off, while N4 is activated. The storage node QB is confined from the RBL.

4. SIMULATION RESULTS

The transient Simulation results of proposed 8T SRAM cell are depicted in the figure 6 and the transient Simulation results of proposed 6T SRAM cell are depicted in the figure 7.

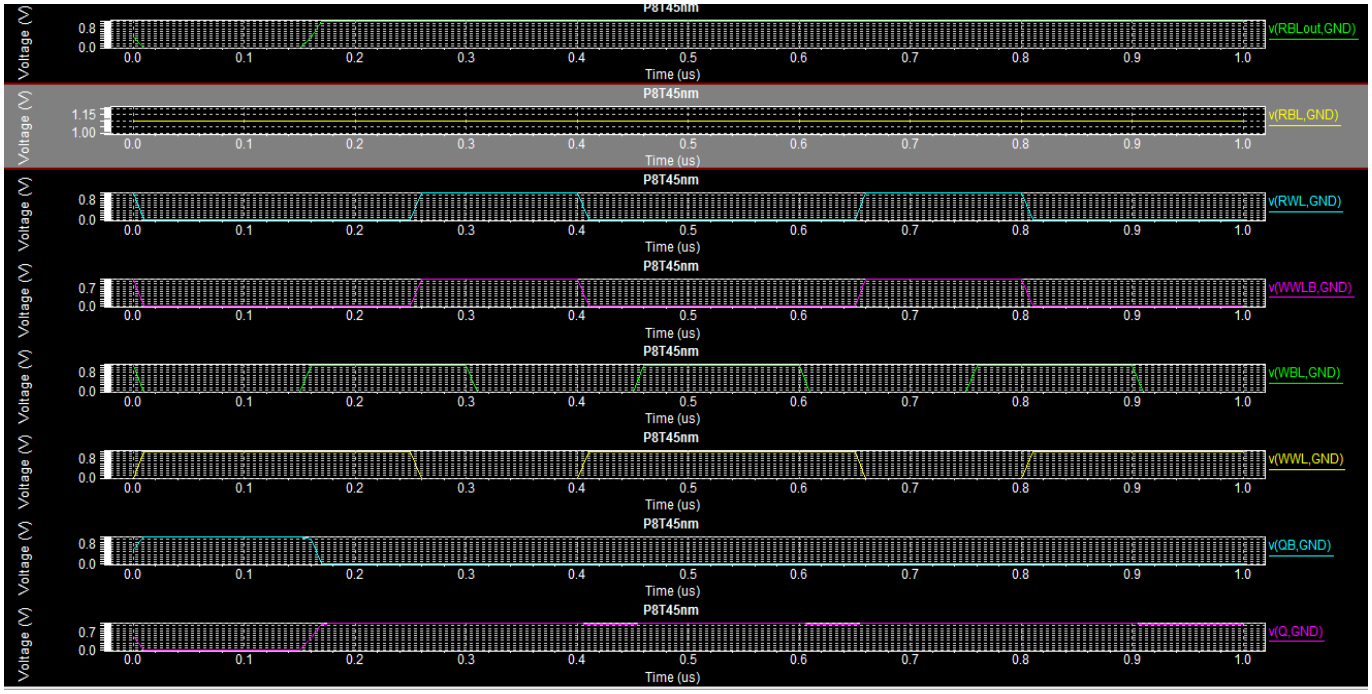

Figure 6: Transient results of proposed 8T SRAM Cell

Here in this simulation, upto 280n sec the WWL is asserted high and RWL is deactivated, during this time interval the data is written onto the SRAM cell depending on the value of WBL. The value of WBL is assigned at Q and value of QB is reverse to that of Q. During this time read operation is isolated from the write operation. Later the RWL is activated and the value at stored node Q can be read at RBL. In this way for different values of wordlines and bitlines, the corresponding values at storage nodes Q and QB are plotted.

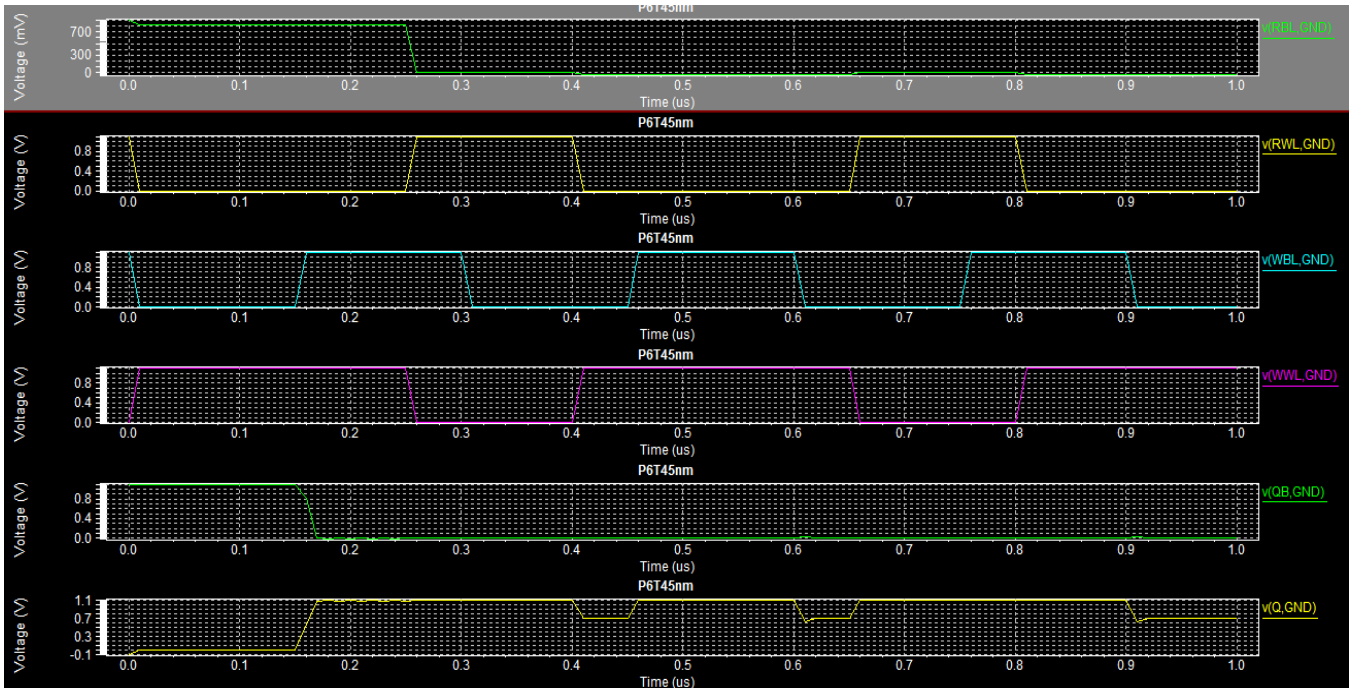

Figure 7: Transient results of proposed 6T SRAM Cell

During the simulation, upto 280n sec the WWL and WBL is asserted low and high and RWL is deactivated, during this time interval the data is written onto the SRAM cell depending on the value of WBL. The value of WBL is assigned at Q and value of QB is reverse to that of Q. During this time read operation is isolated from the write operation. Later the RWL is activated and the value at stored node Q can be read at RBL. In this way for different values of word lines and bit lines, the corresponding values at storage nodes Q and QB are plotted.

Table 1: Comparison of power dissipation and average delay w.r.t conventional and proposed SRAM architectures in CMOS 45nm Technology

Technique	Power Dissipation(µW)	Average Delay(µs)
Conventional 6T SRAM	4.41	0.29
Conventional 8T SRAM	11.13	0.29
Conventional 10T SRAM	32.02	0.14
Proposed 8T SRAM with virtual ground with 10 Transistors	17.98	0.077
Proposed 6T SRAM	4.18	0.21

Table 2: Comparison of power dissipation and average delay w.r.t conventional and proposed SRAM architectures in CMOS 32nm Technology

Technique	Power Dissipation(µW)	Average Delay(µs)
Conventional 6T SRAM	2.77	0.29
Conventional 8T SRAM	7.00	0.27
Conventional 10T SRAM	23.86	0.14
Proposed 8T SRAM with virtual ground with 10 Transistors	2.96	0.004
Proposed 6T SRAM	1.13	0.21

Table 3: Comparison of power dissipation and average delay w.r.t conventional and proposed SRAM architectures in CMOS 22nm Technology

Technique	Power Dissipation(µW)	Average Delay(µs)
Conventional 6T SRAM	1.73	0.3
Conventional 8T SRAM	3.78	0.29
Conventional 10T SRAM	18.14	0.14
Proposed 8T SRAM with virtual ground with 10 Transistors	0.251	0.002
Proposed 6T SRAM	0.246	0.21

From the Table 1, 2 and 3, it is evident that the power dissipation [9], [10] is approximately remained equal in conventional and proposed architectures of SRAM in CMOS 45nm, 32nm and 22nm technology. Also it is noticed that there is considerable change in average delay i.e., the delay has been decreased in proposed architectures of SRAM when compared with the conventional architectures. Also it is noticed that the power dissipation and delay have been reduced w.r.t advancement in CMOS technology.

Figure.8 and Figure.9 depicts the comparative analysis details between the proposed and conventional approaches with respect to the power dissipation and delay incurred respectively. As seen from the figure.8, the power dissipated by the proposed both technologies such as 8T SRAM with virtual ground and proposed 6T SRAM is observed to be less compared to the conventional approaches such as conventional 6T SRAM, 8T SRAM and 10T SRAM.

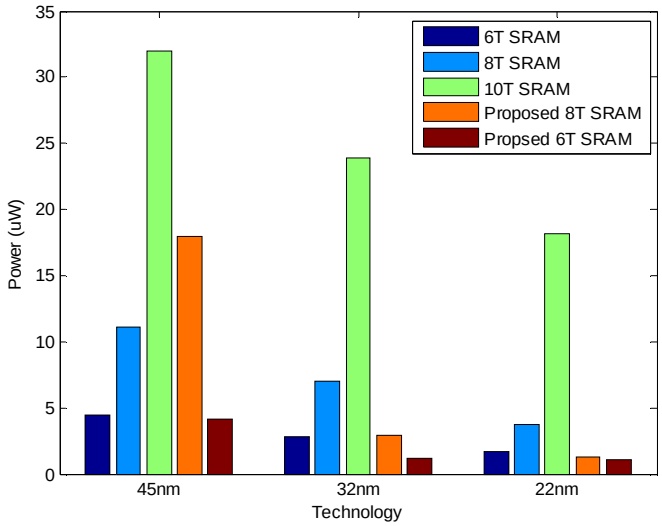

Figure 8 : Power dissipation comparison

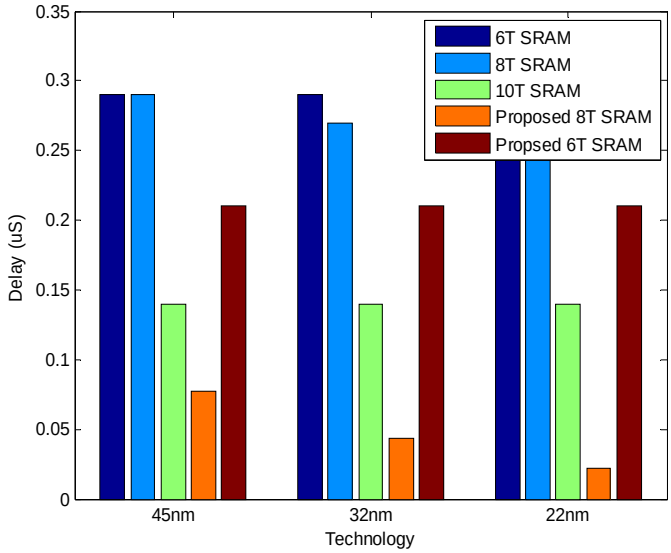

Figure. 9 : Delay analysis

Moreover, at every phase of technology like 45nm, 32nm, and 22nm, the power dissipation of proposed designs have less value compared to the conventional approaches. Similar the delay incurred in the proposed 6T and 8T architectures is also observed to be less compared to the conventional ones. Since the proposed designs have only line word Bit line (WBL) and one read Bit line, the power consumption as well as delay will be considerably less. Moreover, in the proposed designs, particularly 8T circuit, there is a virtual ground that enhances virtual power lines to keep the power dissipation less. As read Bit line doesnot require recharge, the power dissipation will be very less.

5. CONCLUSION AND FUTURE SCOPE

This paper introduced new 6T SRAM and 8T SRAM architectures to optimize the power dissipation at circuitry level. Simulation experiments conducted over the proposed and conventional architectures revealed the efficiency of proposed design. Further, the comparisons were done between the existing SRAM architectures and proposed 8TSRAM and 6T SRAM during their operation in terms of average delay and power dissipation. Delay is reduced significantly during the operation of SRAMS. Also as the CMOS technology is advanced there is betterment in the performance of SRAMs in terms of power dissipation and delay. In the extended work, we plan to provide the comparative analysis of proposed SRAMs with adiabatic SRAM cells.

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