ISSN 2278-3091
Volume 9, No.3, May - June 2020
International Journal of Advanced Trends in Computer Science and Engineering
Available Online at http://www.warse.org/IJATCSE/static/pdf/file/ijatcse201932020.pdf
https://doi.org/10.30534/ijatcse/2020/201932020

Design of Reversible and Non- Reversible Binary to Gray and Gray to Binary Converter using Quantum Dot Cellular Automata

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ABSTRACT

The advancement in technology increases day by day, that the conventional based CMOS VLSI technology reached its peak due to physical limits like power dissipation and size. In order to overcome this, a new alternative method has introduced to recurrently improve the development of digital electronics. Quantum-Dot Cellular Automata (QCA) approach is nanotechnology which is an emerging technology provides an efficient platform to overcome the confines of existing CMOS. In this research investigation a novel design of 4-bit reversible and non-reversible binary to gray (B-G) and gray to binary code (G-B) converter was simulated with the help of QCA tool and the obtained results were found to be efficiently better when compared with that of the previous one.

Key words: Quantum-dot Cellular Automata (QCA), CMOS, Binary to gray Code Converter, Gray to binary converters.

1. INTRODUCTION

Innovation advancement and modern industrial competition have been driving the semiconductor business to make smaller, faster and less power consumption powerful devices. By the emphasis of miniaturization, the modern semi-conductor technology is characterized. Traditionally the microelectronics is scaled down to Nano electronics, this future system that comprise of these nanometric structures require both novel modern switching devices and architectures. Quantum-Dot Cellular Automata (QCA), an embryonic invention proposed by Craig S. Lent et al in 1993 [1]. He focused on the idea of employing cellular Architectures which are companionable with Quantum Devices. The QCA allows to operate in THz frequency range with larger the device integration density more than that of CMOS [2-4]. In the CMOS VLSI circuits, the data transfer by the means of electric current between the transistors, whereas in QCA the binary information (0s and 1s) is projected in the form of charge configuration in the cell of QCA [5-7]. The most efficient cell reduction techniques are implemented on code converters.

The essential unit in QCA is cell which is formed by four Quantum-Dots placed at the four corners of a square [8-10]. Quantum dots are nano-based material with zero dimension, synthesised from usual semiconducting materials like InAs/GaAs. The cell also consists of two electrons which occupy the diagonal due to coulomb electro-static repulsion. In the cell the position of electrons is denoted by the polarization P (P = +1 and P = - 1).

The linear arrangement of QCA cells patterns a binary wire the information is transferred along the wire by the Columbic interaction between the adjacent QCA cells. For electrostatic communication, the input cell is strongly polarized in one direction and the signal propagates from one end to another. The essential power required to run the circuit and to control information flow in QCA circuits is carried out by clock [11]. Here the clock involves of 4 phase such as Hold, Relax, Release, and Switch. The QCA circuit is divided into clock zones and the cells in the zone are controlled using the signal. There is 90o phase lag between each clock. To govern the polarization effects and reactions, one should hold the polarization of the first cell fixed and lower the potential barrier of its neighbouring cell to let the electrons of the adjacent cell to displace. To perform phenomenon should repeat repeatedly to pass the information through cells these clock zones are necessary.

The intersection of two QCA wires is known as QCA crossover. There are two types of cross overs mostly used in QCA those are Multi-layer approach and co-planar approach. In Multi-layer approach, data is transferred through another layer over the main layer whereas, in Coplanar approach, by rotating the QCA-cells at 45o vertical wire can be achieved [12-15].

Code converters are circuits that convert code into another which is programmed in logic arrays and used in many fields such as protecting information from third parties and increase data flexibility. It is also efficient in the security department for devising and cracking codes. These reversible code converters can show the results of converted binary code as well as given input binary code such that this system performs a crucial role in the field [16-20].

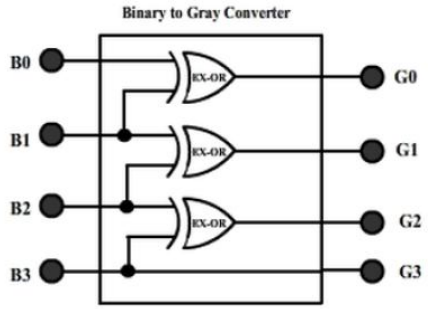

Figure 1: 4-bit B to G code converter schematic

1.1. Binary to Gray (B-G) converter

Binary code is the simplest form of computer code which consist of a sequence of bits either '0' or '1' [16-18]. Let's assume four digits B3, B2, B1, and B0 are taken as a binary number and G3, G2, G1, and G0 be gray code (Figure. 1), the logic expression of the B to G code conversion is expressed as, G3 = B3; G2 = B3 ⊕ B2; G1 = B2 ⊕ B1; G0 = B1 ⊕ B0;

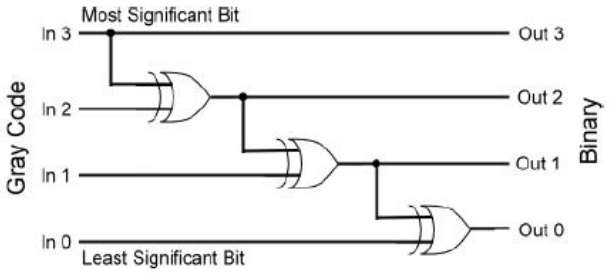

Figure. 2: 4-bit G to B converter schematic.

1.2 Gray to Binary converter

Gray code is known as reflective code [19, 20]. In Gray code successive code bits vary in a one-bit position that's why it is popular for unit distance code, and G to B code conversion (Figure. 2) expression written as,
B3 = G3; B2 = B3 ⊕ G2; B1 = B2 ⊕ G1; B0 = B1 ⊕ G0;
Whereas, ⊕ represents the Ex-OR operation between the digits.

2. PROPOSED METHOD

2.1. Feynman Gate

Feynman gate (FG) is known as CNOT gate which consist of 2 x 2 reversible gate, where A and B inputs are plotted to P and Q outputs, P = A and Q = (A⊕ B) Figure 3. shows the logic schematic of Feynman Gate. FG is designed to use it for designing Reversible code converters Figure 4 represents the proposed layout of Feynman gate, whereas the waveform of Feynman is shown in Figure 5.

Figure 3: Schematic layout of the Feynman Gate

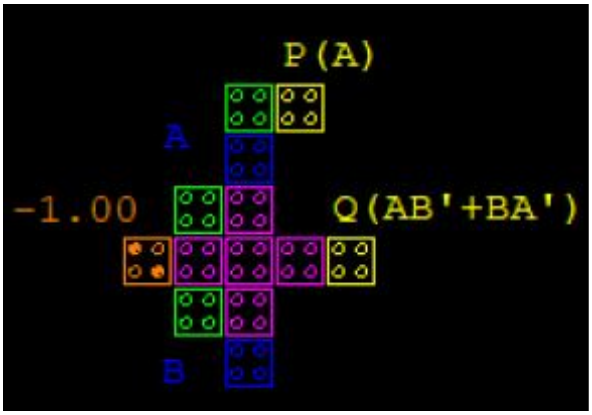

Figure 4: Proposed Feynman Gate QCA simulation

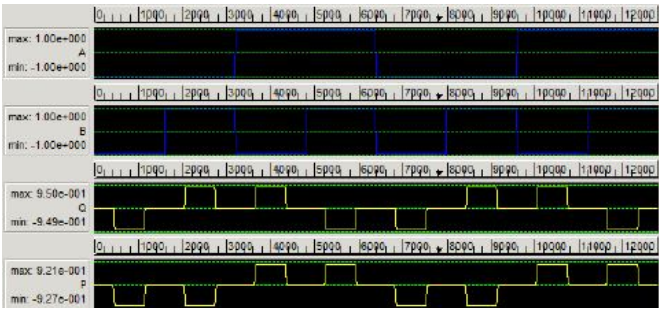

Figure 5: Feynman gate output waveforms

2.2. Non-reversible 4-bit binary to gray and gray to binary code converters

The proposed layouts 4-bit binary to gray code converter consist of 33 cells with area of 0.04 μm^2 and the non-reversible gray to binary code consisting of 39 cells with area 0.06 μm^2 the cell count is reduced in this layout and 2 crossovers are used between the cells as shown in Figure 6 and 7 [16-18]. Figure 8 and 9 show the waveform of the non-reversible 4-bit B to G and G to B code converters. The obtained results were equated with that of the existing approaches and found to be efficient as tabulated in Table 1&2.

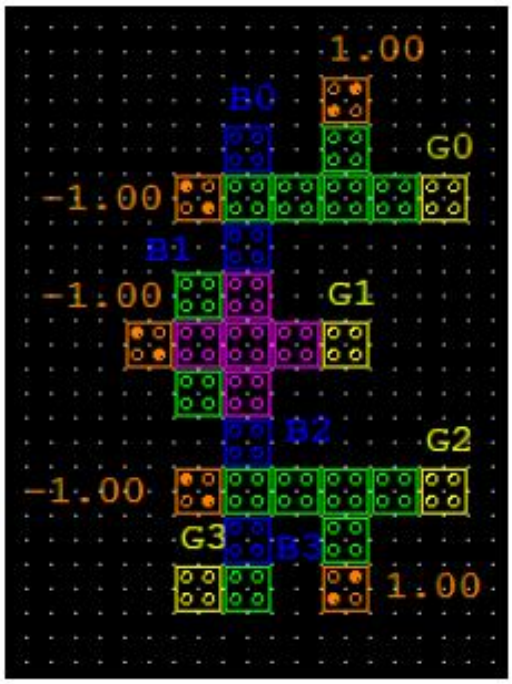

Figure 6: QCA layout of 4-bit B to G

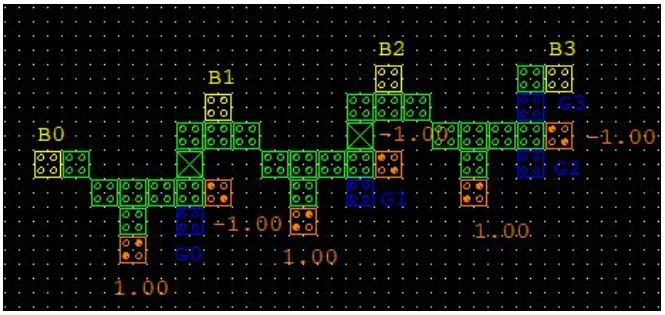

Figure 7: 4-bit G to B code converter

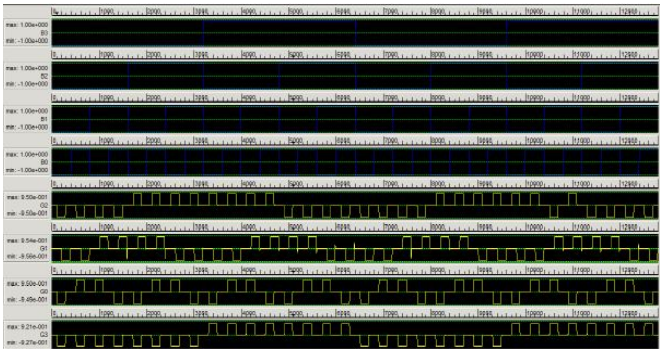

Figure 8: 4-input B to G code converter wave form

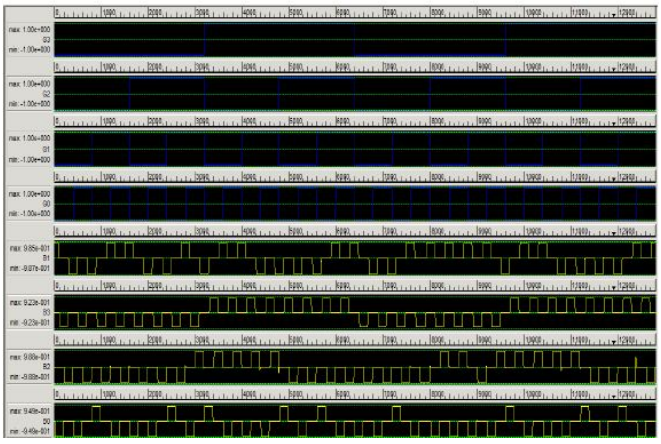

Figure 9: Waveform for 4-bit G to B code converters

Table 1: Non-reversible converter comparison table for B-G

Parameters	**4-bit B to G code converter**			
	Proposed	**Previous Work**		
		[16]	**[17]**	**[18]**
Cells	33	37	127	192
Area (μm^2)	0.04	0.04	0.41	0.34
Crossover	0	0	3	3
Latency	0.5	0.95	0.75	2

Table 2: Non-reversible converter comparison table for G-B

Parameters	**4-bit G to B code converter**			
	Proposed	**Previous Work**		
		[16]	**[17]**	**[18]**
Cells	39	47	99	269
Area (μm^2)	0.06	0.05	-	0.69
Crossover	2	0	0	0
Latency	0.75	1	0.75	6

2.3. 4-bit Reversible B to G and G to B code converter

A novel layout for reversible 4-bit B to G and G to B code converters using Feynman gate is proposed. Table 3 & 4 shows the simulation factors of the proposed layout with previous work [19, 20]. Figure 10 & 11 shows the layout of 4-bit reversible B to G and G to B. The count of QCA cells and area of the proposed layouts has been reduced and the performance was found to be improved when compared with that of the previous work, the waveforms of 4-bit reversible B to G and G to B was shown in Figure 12 & 13.

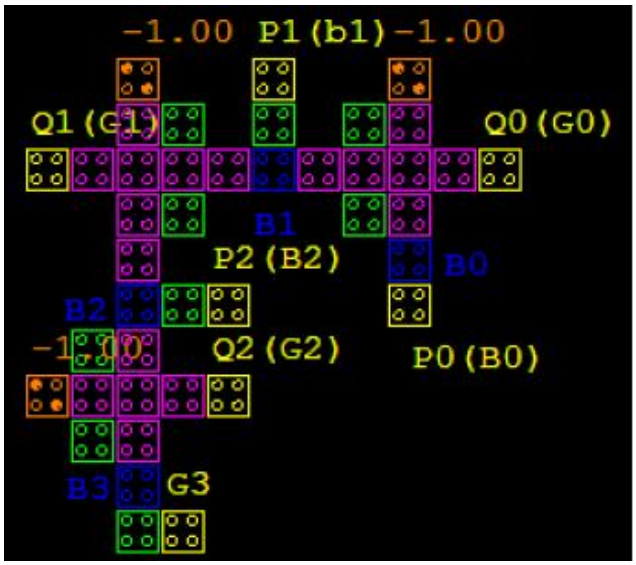

Figure 10: QCA layout of reversible binary to gray.

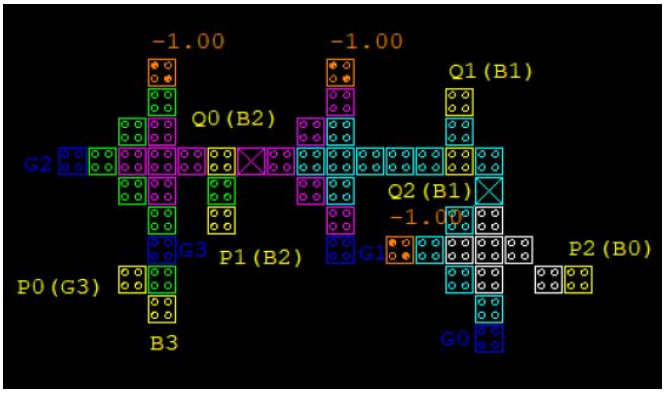

Figure 11: QCA layout four 4 -bit reversible Gray to Binary converter.

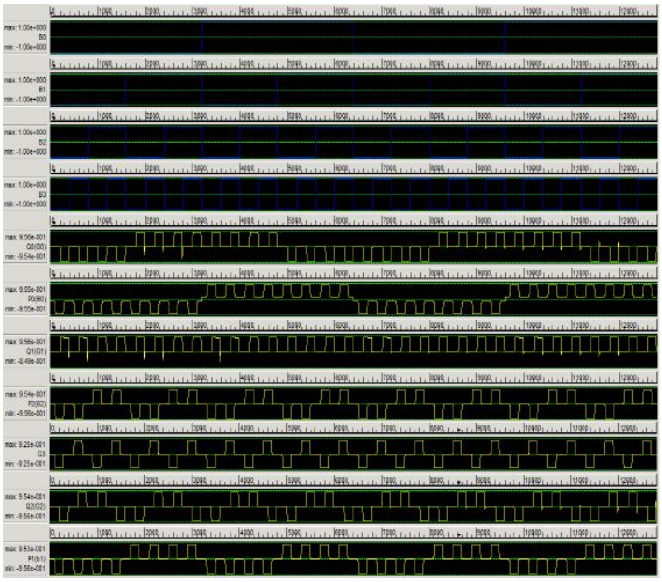

Figure 12: Waveform of 4-bit reversible binary to gray code converter.

Figure 13: Waveform of 4-bit reversible gray to binary code converter.

3. RESULTS AND DISCUSSION

The layouts of all circuits have been designed in QCA designer 2.0.3. The parameters are used for bistable Approximation, 12800 Number of samples, 65.000000nm radius of effect, 0.001000 convergence tolerance, 11.500000 layer separation, 12.900000 relative permittivity, $9.800000e^{-22}$ J clock high, $3.800000e^{-023}$ J clock low, 0 clock shift, 2.000000 clock amplitude factor and 100 maximum iterations per sample. The tabular forms show the comparative analysis of proposed models with existing models this paper mainly focused on reducing cell count which further reduces the cell area, that was successfully achieved by proposed layouts and the following Table 3 & 4

forms describes the comparative analysis of the proposed work with that of the previous work.

Table 3: 4-bit reversible converter for B-G

Parameters	4-bit B to G code converter		
	Proposed	Previous Work	
		[19]	[20]
Cells	49	108	118
Area (μm^2)	0.06	0.11	0.38
Crossover	0	1	2
Latency	0.75	0.75	0.75

Table 4: 4-bit reversible converter for G-B

Parameters	4-bit G to B code converter		
	Proposed	Previous Work	
		[19]	[20]
Cells	52	77	112
Area (μm^2)	0.010	0.1	0.36
Crossover	2	1	2
Latency	0.75	0.75	1

4. CONCLUSION

The paper is about designing 4-bit B to G code and G to B reversible and non-reversible B to G and G to B code converters using Quantum-Dot cellular Automata, adapting majority gate techniques. By employing Feynman gate the QCA cell count is reduced thereby the area was reduced. The proposed layouts are shown good expected results and comparative analysis is also done with best existing models.

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