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Performance Analysis of a Low-Power High-Speed Hybrid Multiplier Circuit

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ABSTRACT

In this paper, a hybrid multiplier circuit design employing hybrid logic style compared with transmission gates is reported. Multipliers play a crucial role in VLSI signal processing and various different applications. Area, Speed and Power are the fundamental factors in any VLSI systems. The primary goal is to enhance the general performance parameters of the multiplier such as delay, power and transistor count in comparison with the existing multipliers. The key role of hybrid logic approach is to take advantage of the features of numerous styles in an effort to enhance the general performance. The hybrid logic style including very susceptible CMOS inverters coupled with transmission gates is used inside the proposed circuit which offers high performance and occasional power design. Design metrics together with the speed, power and count of transistor are taken into consideration. All the circuits were designed the usage of Microwind device and simulated in 90nm technology. From the simulation consequences, it is determined that there's 53.4% reduction of energy and 38.9 % reduction of delay in the proposed multiplier for 1.2V power supply while compared to the present multiplier the use of transmission gates with 90nm technology.

Key words : High speed, hybrid design, low power, transmission gates, weak inverters.

1. INTRODUCTION

Multipliers play a crucial role in cutting-edge virtual signal processing and various different packages. High speed multiplier is the essential constructing block in a DSP system. Parallel multipliers are used for figuring out the high speed multiplication on the way to lessen the general power consumption of the DSP. It's far greater essential to reduce the energy dissipation of the parallel multipliers. Numerous techniques had been developed to reduce the strength consumption of parallel multiplier. Parallel multipliers are realized as array type shown in Figure 1 or tree type architectures. Distinctive logic styles each having its personal merits and bottlenecks, turned into investigated to implement hybrid multipliers[8]-[11][13]. Multipliers are built using the binary adders and full adders, that is one of the maximum essential building block of all of the afore mentioned circuit programs [4] and half adders. The designs are broadly categorized as Static style and Dynamic style. The on-chip region requirement is high in static full adders even as compared with its dynamic counterpart. Static full adders are generally greater dependable, easier with a good deal less power requirement .The conventional domain has vital logic styles which includes static CMOS [8] CPL[5][9] dynamic CMOS logic[10]TGA[1][2] More than one logic style referred to as hybrid logic design for the implementation is used for the alternative adder designs. To enhance the overall performance of the full adder these designs exploit the capabilities of various logic styles. CPL using 32[5] transistors show favorable voltage swing recovery. Despite the fact that, CPL is not appropriate for low strength applications because of its immoderate transistor be counted and overloading of its inputs. Both NMOS and PMOS transistors are blended the use of parallel logic styles in transmission gates. Low power CUK converters were proposed in [14]. When performance was compared, transmission gate circuit consumed less power as compared to CPL using CMOS logic style. Improving the various performance parameters like delay, power, and count of transistor of the multiplier in comparison with the existing ones is the main objective. The circuit becomes carried out using 90-nm generation by means of the usage of Microwind tool. The common power consumption (0.534 mW) of the proposed circuit become decreased via the usage of very vulnerable CMOS inverters added with strong transmission gates of 1.2 V which is used for designing hybrid multipliers. Figure 1 shows the basic 4X4 array multiplier structure.

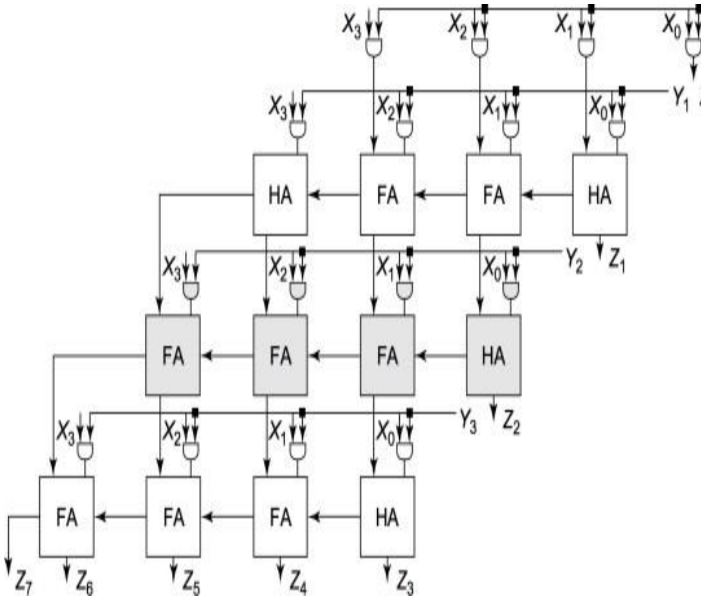

Figure 1: Structure of 4X4 Array Multiplier

2. EXISTING MULTIPLIER DESIGN USING TRANSMISSION GATE

A transmission gate is defined as an electronic element that will selectively block or pass a signal level from the input to the output. This solid-state switch is comprised of a PMOS transistor and NMOS transistor which is shown in Figure 2. The transmission gate consists of two MOSFETs, one n-channel responsible for correct transmission of logic zeros, and one p-channel, responsible for correct transmission of logic ones.

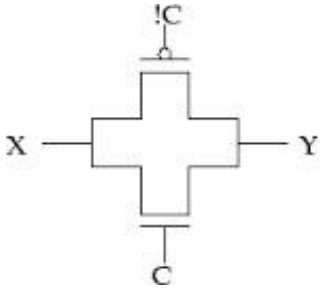

Figure 2: Basic Transmission Gates

2.1 Half Adder Using Transmission Gates

Figure 3 shows the existing full adder circuit using the Transmission Gate (TG) logic. It consists on nmos and pmos transistors with common source and drain connection and separate connection for gate. The circuit has a total of 12 transistors, consisting of transmission gates, PMOS and NMOS.

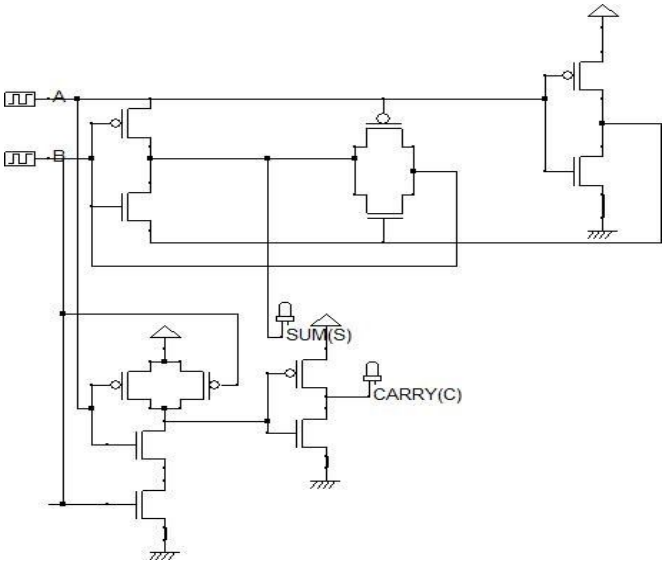

Figure 3: Half Adder using Transmission Gates

2.2 Full Adder Using Transmission Gates

Figure 4 shows the existing full adder circuit using the Transmission Gate (TG) logic. It consists on NMOS and PMOS transistors with common source and drain connections and separate connection for gate. The circuit has a total of 20 transistors, consisting of transmission gates, PMOS and NMOS.

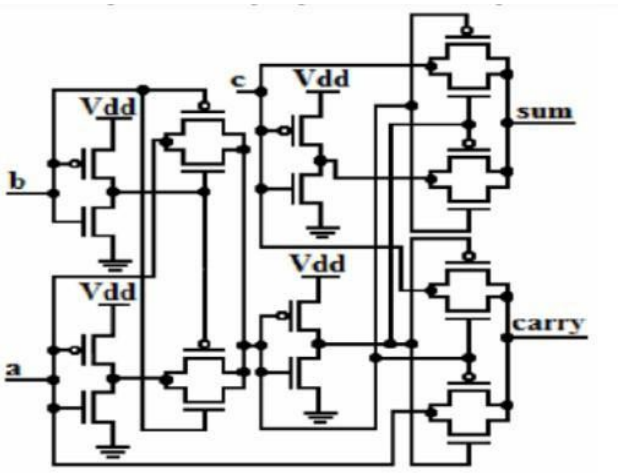

Figure 4: Full Adder Using Transmission Gate

3. DESIGN APPROACH OF HYBRID MULTIPLIERS

Due to the advancements made in the technology, many researchers are trying to design multipliers with some specific design targets. The required design targets are high speed and low power consumption. To achieve the above mentioned targets, low power AND gates, full adders and half adders were used to implement 4X4 multipliers, which provides greater efficiency and good driving capability. The blocks of AND gates, full adders and half adders are used in this designing process.

3.1. XNOR module

The power consumption of the full adder circuit is due to the XNOR module. To limit the power to the viable growth this module is designed. Here in Figure 5 the modified XNOR module the consumption is reduced significantly with the aid of vulnerable inverters formed via transistors. For few cases the level restoring transistors guarantees the full swing of the levels of output signals. In resting cases it avoids the voltage degradation problem and produces the output. As compared with that of 4T XNOR [6]-[7] here the XNOR uses six transistors to get better logic swing. In this paper, the low-power and high-speed is offered by modified XNOR module.

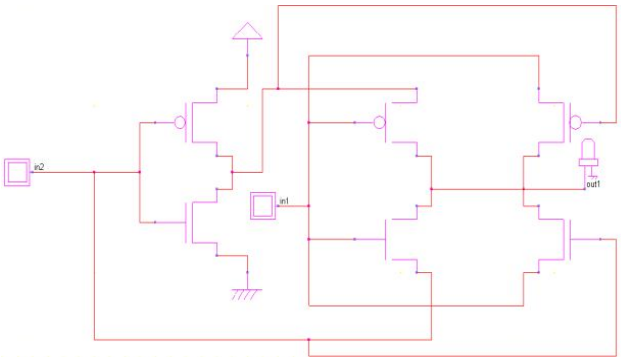

Figure 5: Circuit of XNOR module

3.2. Carry Generation Module

The modified structure of carry generation module is shown in Figure 6. The transistors were used for implementing the output carry signals. The input carry signal propagates through single transmission gate handiest. It reduces the general bring propagation course substantially. The reduction in propagation delay of the carry signal is guaranteed by the strong transmission gates.

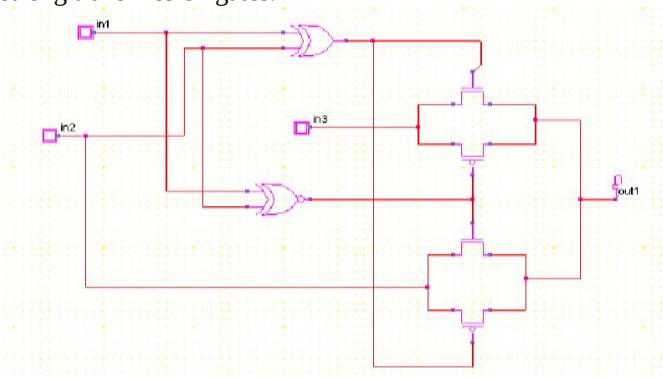

Figure 6: Carry generation module using Hybrid Technique

3.3 Full adder module

The full adder circuit is designed as proven in Figure 7. Module 1 and module 2 are the XNOR modules that generate the sign bit of sum and module 3 generates the output convey signal. The entire adder circuit is optimized in phrases of power, area and delay because of person layout of each modules.

Figure 7: Full adder module

4. PROPOSED MULTIPLIER CIRCUIT USING HYBRID LOGIC

Figure 8 shows the proposed multiplier circuit using hybrid logic. This proposed multiplier circuit consists of 224 transistors comprising of 8 full adders (128 transistors), 4 half adders (32 transistors), 16 AND gates (64 transistors).

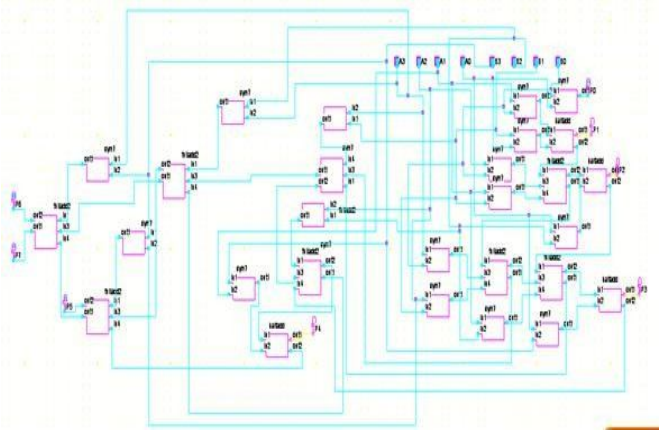

Figure 8: Proposed Multiplier design

The detail diagram of the proposed multiplier is shown in Figure 8. The XNOR modules give the sum output. The inverter comprised of transistors generates the complement of the input in2.It Is efficiently used to layout the controlled inverter the usage of the transistor pairs. The managed inverter output is essentially the XNOR of in1 and in2. However it has a few voltage degradation trouble. Reading the fact desk of a full adder, the condition for output is as follows, if in1= in2, then out1= in2; else, out1 =in3. The parity between inputs in1and in2 is checked via in1 in2 function. If they're same, then out1 is equal as in2, that is implemented the use of the transmission gate found out by using transistors. In any other case, the input conveys signal in3 is meditated as out1.

5. RESULTS AND DISCUSSION

The simulation of the proposed multiplier is done by using Microwind Tool with of 90nm generation. Figure 9 shows the

simulation output of existing multiplier circuit designed using transmission gate. Here, for example, the input A0A1A2A3B0B1B2B3 is given as 00000000, 11111111, 00110011 and it produces an output P0P1P2P3P4P5P6P7 of 00000000, 10000111, 00001001 respectively.

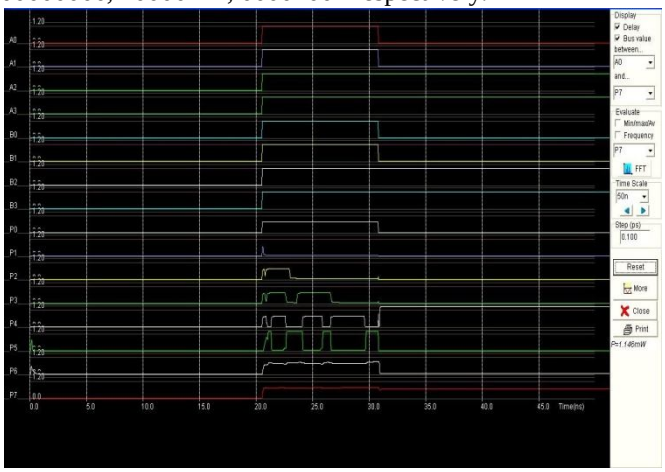

Figure 9: Simulation Output of Multiplier Circuit Using Transmission Gate

Figure 10 shows the simulation output of proposed multiplier circuit using hybrod technique. Here, for example, the input A0A1A2A3B0B1B2B3 is given as 00000000, 11111111, 00110011 and it produces an output P0P1P2P3P4P5P6P7 of 00000000, 10000111, 00001001 respectively.

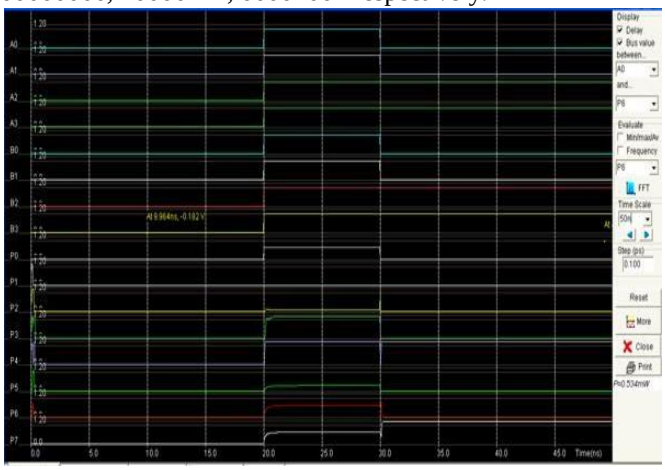

Figure 10: Simulation Output of the Proposed Multiplier Using Hybrid Logic

To optimize each delay and power of the circuit, the Power Delay Product (PDP), the power consumed has been reduced in the proposed layout. It was decided that in the proposed circuit, the power consumption may be minimized through mainly sizing the transistors in inverter circuits. By specially sizing the transistors of the transmission gates the carry propogation delay may be progressed. To investigate the success of the proposed multiplier during its actual use in VLSI applications, a practical simulation environment output is shown in the Table 1. The overall performance evaluation of the proposed multiplier was achieved with version in supply voltage for 90nm generation.

Table 1: Performance Analysis of multiplier in 90nm technology with 1.2 V power supply

Design	**Transmission Gates**	**Proposed (Hybrid Circuit)**
Power (mW)	1.146	0.534
Delay (ps)	1400	855
PDP (pJ)	1.604	0.456
Transistor count	272	224

The transistor count of the proposed multiplier is not the minimum, yet the transistor count is comparable with other references. For evaluation, the proposed multiplier in addition to the existing ones had been simulated using the Microwind tool. The simulation turned into achieved for varying supply voltage such as 1.2V and 1.8 V in 90-nm generation.

6. CONCLUSION

A multiplier using hybrid logic style is presented in this paper that targets high performance and low power design. The hybrid logic style such as very weak CMOS inverters coupled with transmission gates is used in the proposed circuit. The simulation became achieved the usage of Microwind tool with 90-nm technology and as compared with different existing design techniques. The simulation results show that the proposed hybrid logic multiplier circuit cause reduction in power and improved PDP compared with the existing designs. Thus the power consumption and delay of proposed hybrid multiplier is reduced by 53.4% and 38.9% respectively when compared to existing design approach. It has a drawback of voltage degradation for some cases.

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