Volume 9, No.4, July – August 2020 International Journal of Advanced Trends in Computer Science and Engineering Available Online at http://www.warse.org/IJATCSE/static/pdf/file/ijatcse185942020.pdf

https://doi.org/10.30534/ijatcse/2020/185942020

Cooling Microprocessors with Commercial Thermoelectric Module Powered by Pulsed Current



Saleh Alshehri

Computer Science and Engineering Department, Jubail University College, Jubail Industrial City, 31961, Kingdom of Saudi Arabia shehri@ucj.edu.sa

ABSTRACT

Computer chips can be cooled by many techniques such as forced air cooling, liquid nitrogen, heat pipes and other. While thermoelectric is being used in many industrial applications, it is an excellent choice for electronic cooling. The presented research focuses on cooling microprocessors using thermoelectric in transient mode where the supply electrical current is in form of pulsed shapes. The study provided experimental tests that were performed to investigate the cooling capability of thermoelectric cooling module when supplied with pulsed electrical current. The first experimental setup was designed to identify the value of the optimum electrical current for the thermoelectric cooling module at which lowest hotspot temperature. The second experimental setup was designed to investigate the behavior of this thermoelectric module performance when it was supplied with pulsed shape of electrical currents instead of continuous electrical current level.

Various parameters were investigated to predict the minimum hotspot temperature as well as the ripple of the hotspot temperature. Initial current value, its duration, the afterward OFF time duration and ON time duration of the current are the parameters under investigation. The results of the experimental tests showed very clearly that all these parameters have effect on the cooing capability of the thermoelectric cooling module for reducing the temperature of the hotspot.

To be able to choose the optimum operating parameters of the thermoelectric cooling module for the desired cooling capability of hotspot, neural networks were used for this purpose. The result was a simple design tool to be used to design the cooling system of microprocessors using thermoelectric cooling module. Regardless of the data scarcity, the accuracy of the neural networks for hotspot temperature and temperature ripple acceded 99% and 92% respectively.

Key words : Microprocessor hotspots, electronic cooling, thermoelectric generator, thermoelectric cooler, neural network.

1. INTRODUCTION

Thermoelectric (TE) technology has two main types of industrial applications namely power generation and cooling. Generating electrical power is based on Seebeck phenomena [1]. If the TE module is placed between any temperature difference places, it generates electricity. The other type of industrial application is when the TE module is supplied with electrical power which is based on the Peltier effect [1]. It converts this electrical power to thermal energy for cooling or heating purposes. Figure 1 shows TE unicouples for the applications of electrical power generation and heating/cooling.

As shown in Figure 1, the TE module is constructed using two thin ceramic wafers holding a series of positive (P) and negative (N) doped semiconductors substances. Each P and N legs constitute a unicouple. A collection of these unicouples are connected electrically in series and thermally in parallel to form the TE module with different electrical power generation or heating/cooling capabilities.



The Very-Large-Scale Integration (VLSI) has reached very advanced stage where over 1000 million transistors are packed in a single chip. The packaging density creates very serious challenge [2-3]. The generated heat fluxes can reach 100 W/cm2. The microprocessors architecture necessitates the generation of local heat rates higher in certain locations than other locations, resulting in different heat fluxes across the microprocessors. In this study, the locations with high heat

fluxes are called hotspots (HS) [4]. The heat fluxes at these hotspots can be over 1000 W/cm². To overcome these thermal challenges, integrated circuit (IC) thermal managements must be designed so as to insure the temperature of the HS be below certain threshold value. Additionally, the value of the threshold temperature depends on the microprocessor' manufacturers. Presently, there are two main types of IC thermal management's techniques, namely, active and passive [5]. Some of these techniques include heat sink air cooling, two-phase heat pipes and thermosyphons, microchannel liquid heat removal and thermoelectric devices. Each of these techniques has advantages and disadvantages [6-10].

Since thermoelectric cooler (TEC) module does not have moving parts, it is very reliable [1,11]. It is also modular by design [1,11]. There have been many attempts to use TE devices for cooling electronic components [12-17]. Thermoelectric technology was used specifically for hotspot cooling [18-23].

For only one value for hotspot heat rate and one value for the background heat rate, the main objective of this study is to develop an initial design tool to obtain the wanted microprocessor hotspot minimum temperature and temperature ripple. This is based on generating operating square pulses for the TEC to work in transient mode. It was decided to use NN for two reasons. First, NN is one of most efficient model to be used for regression especially for nonlinear systems [24]. Second, NN needs smaller set of training samples [25]. Several numbers of experiments were conducted. The results were collected to train neural networks (NN). The resulting NNs are then used as a predicting tool to obtain the wanted HS temperature and temperature ripple. To expand the capability of the design tool that is developed in this paper, another study is currently being conducted to generate the necessary test results for different values of hotspot and background heat rates.

To operate the TEC, supply electrical current must be provided. At the steady-state, the current is constant and its optimum value can be found at which the hotspot temperature reaches its minimum value. In transient operation mode, however, the electrical current is supplied to the TEC in forms of pulsed shapes. In this case, the supplied electrical power is mainly depending on the ON and OFF time durations that the current will be at. Obviously, for longer OFF time duration, the electrical power needed for the TEC will be lower. This would affect the TEC performance for reducing the hotspot temperature to an acceptable value. The pulsed shapes of the TEC electrical current would also create a ripple on the temperature of the HS. Note that the ripple temperature of the HS is defined in this study by the difference between the highest and lowest temperatures during the course of applying pulsed shape electrical current. It is necessary to minimize this ripple value in order to minimize the temperature fluctuation/gradients, and thus minimizing the induced thermal stresses inside the microprocessors. As such, it is important to develop an initial tool (to be expanded in future to account for different values of heat rates for the hotspot and background) that can help the designer to identify the

temperature of the HS and the temperature ripple for any given set of input parameters.

2. EXPERIMENTAL TESTS

2.1 Steady-state Mode

The first part of the experiment was done in previous study [21]. The aim was to investigate the TEC cooling capability of a commercial TE module and to find experimentally the optimum operating current. The experiment was built using an aluminum sheet to mimic the microprocessor, a ceramic heater to mimic the HS, patch heater to mimic the background heat, TEC module and a heat sink with electrical fan. All these parts were enclosed in an assembly with XPS insulation. The needed power to all these parts were provided using individually controlled power supplies. The temperatures of various locations inside the assembly were collected and monitored using 7 k-type thermocouples connected to external PC. Figure 2 shows overview of the major parts of the experimental setup [21].

Each test component was individually supplied with a separate power supply. The following are the test parameters:

• The power supply connected to the patch heater (background) with voltage = 8.49 V and current = 0.41 A (3.48 W).

• The power supply connected to the ceramic heater (hotspot) with voltage = 7.18 V and current = 2.17 A (15.58 W).

• The power supply connected to the external fan with voltage = 9.6 V and current = 0.23 A (2.3 W).

TEC was supplied with gradually increasing current from 0 A (open circuit condition) to 8.0 A. The incremental step size was 0.5 A. In each current step, the temperature of all locations inside the assembly was monitored until the steady-state condition was achieved. The HS, background and surroundings temperatures were obtained as shown in Figure 3. As shown in this figure, the optimum current obtained in the first part was 4.5 A. This current and some other values are used in the second part of the experiment as discussed next.



Figure 2: Main components of the experimental setup [21]



Figure 3:Effect of thermoelectric current on the temperatures at different locations for the case of hotspot heat rate of 15.58 W and background heat rate of 3.48 W

2.2 Transient Mode

The optimum thermoelectric current to get the lowest hotspot temperature which was obtained in the first part (at steady-state condition) is used in the second part of the experiment in transient mode. This optimum electrical current (4.5 A) was used to conduct 14 tests where the TEC supply current is applied in a form of pulsed shape. The heat flux of HS was of 5.97 W/cm^2 . For each test, the electrical current was set to either 4.5 A or 7.0 A for a period of time. Then it was set to OFF (0 A) then ON (4.5 A). The duty cycle is the ratio between OFF and ON time. This duty cycle represents the portion of the electrical power that will be consumed by the TEC module. In all of the fourteen tests, the same procedure was applied as follows:

1. Initial current pulse was set to certain values (4.5 and 7 A).

2. The pulse then set to 0 A for a certain period of time. This state is called "OFF".

3. The OFF period was followed by another period called "ON".

The effect of such scenario was obvious on each test. All various thermocouples continued monitoring the various temperatures in the experiment setup. The two main outputs which were observed in this research were HS temperature and the temperature ripple. Figure 4 to Figure 9 show the results of these tests. The differences in HS minimum temperatures and the temperature ripples for each test can be noticed in these figures.



Figure 4: Effect of the pulsed thermoelectric current of 15 s OFF and 15 s ON at 4.5 A on the temperatures at different locations for the case of hotspot heat rate of (QHS) of 15.58 W and background heat rate (QBG) of 3.48 W



Figure 5: Effect of the pulsed thermoelectric current of 30 s OFF and 30 s ON at 4.5 A on the temperatures at different locations for the case of hotspot heat rate of (QHS) of 15.58 W and background heat rate (QBG) of 3.48 W



Figure 6: Effect of the pulsed thermoelectric current of 15 s OFF and 45 s ON at 4.5 A on the temperatures at different locations for the case of hotspot heat rate of (QHS) of 15.58 W and background heat rate (QBG) of 3.48 W



Figure 7: Effect of the pulsed thermoelectric current of 1 s OFF and 10 s ON at 4.5 A with 130 s initial setup current on the temperatures at different locations for the case of hotspot heat rate of (QHS) of 15.58 W and background heat rate (QBG) of 3.48 W



Figure 8: Effect of the pulsed thermoelectric current of 1 s OFF and 5 s ON at 4.5 A with 130 s initial setup current on the temperatures at different locations for the case of hotspot heat rate of (QHS) of 15.58 W and background heat rate (QBG) of 3.48 W



Figure 9: Effect of the pulsed thermoelectric current of 0.5 s OFF and 7.5 s ON at 4.5 A with 130 s initial setup current on the temperatures at different locations for the case of hotspot heat rate of (QHS) of 15.58 W and background heat rate (QBG) of 3.48 W

For three different pulsed shapes, Figure 10 shows that the lower OFF time duration has resulted in lower HS temperature. The 0.5 s OFF followed with 7.5 s ON is the best among the other since it gave the minimum HS temperature. A tool is needed to test other parameters values to find out the lowest HS temperature with minimum possible electrical operating power conditions. For the case of starting with open circuit condition (i.e. no initial setup current), Figure 11 shows comparison of the hotspot temperature of three other different pulsed shapes. As shown in this figure, the pulsed

shape of 15 s OFF then 45 s ON has resulted in the lowest HS temperature. Additionally, for the same OFF period of the pulsed shape, the longer ON period resulted in lower HS temperature. For example as shown in Figure 11, for 15 s OFF period, increasing the ON period from 15 s to 45 s causes the HS temperature to reduce from 59.08°C (occurred after about 3 cycles) to 47.28°C (occurred after about 2 cycles).

It is important to point out that the experimental tests for different pulsed shapes were conducted at one value of hotspot heat rate (QHS = 15.58 W) and one value of background heat rate (QBG = 3.48 W). Changing these values would result in obtaining different hotspot and background temperatures. For the values of QHS and QBG, the experimental test results showed that four parameters can control the HS temperature. These parameters are the initial current, the duration of the initial current, the OFF time duration and the ON time duration. Only two parameters are needed to predict temperature ripple. They are the OFF time duration and the ON time duration. The collection of all pulsed shapes and the obtained test results are listed in Table 1. The operating parameters were initial current, its duration, OFF time and ON time. The outputs were the HS temperature and its ripple.



Figure 10: Comparison of the hotspot temperature of different pulsed shapes with a period of 130 s as initial setup current at 4.5 A for the case of hotspot heat rate of (QHS) of 15.58 W and background heat rate (QBG) of 3.48 W



Figure 11: Starting with open circuit condition (i.e. no initial setup current), comparison of the hotspot temperature of different pulsed shapes for the case of hotspot heat rate of (QHS) of 15.58 W and background heat rate (QBG) of 3.48 W

Table 1:Collection of all tests input and output parameters.

Initial curren t (A)	Duratio n (s)	OFF duratio n (s)	ON duratio n (s)	HS min. temp (°C)	HS temp. rippl e (°C)
4.5	15	15	15	59.08	9.53
4.5	30	30	30	59.28	18.75
4.5	15	15	45	47.28	13.96
7	15	5	5	59.12	1.53
4.5	15	5	5	58.89	1.30
7	45	10	10	58.52	4.19
4.5	45	5	5	58.46	4.08
4.5	130	1	1	60.50	1.00
4.5	130	1	5	42.40	5.19
4.5	130	1	10	39.35	0.59
4.5	130	1	15	38.80	1.04
4.5	130	1	20	36.68	1.13
4.5	130	0.5	7.5	38.41	0.29
4.5	130	0.5	10	38.01	0.59

For a given operating conditions, a design tool is needed to determine the HS minimum temperature and the corresponding HS ripple temperature. In this study, the Neural Network (NN) was built to construct a tool for predicting the HS temperature and the temperature ripple. Second NN was built to predict the temperature ripple. Both NNs can be used for design purposes. They can be used to predict the HS temperature and the temperature ripple value. Both values are better to be minimum with emphasis of the HS temperature while lower weight can be given to the temperature ripple value to come up with the best operating parameters for a given cooling capability design. For

demonstration purpose, Figure 12 shows an example of the constructed NNs model. The QHS and QBG were 15.58 W and 3.48 W respectively. The HS temperature (NN first output) is dependent on all the four parameters while the temperature ripple (NN second output) is dependent on only the OFF time and ON time parameters. Because the results of this model are applicable only for the case of hotspot heat rate of 15.58 W and the background heat rate of 3.48 W, another study is currently being conducted to generate test results for different values of hotspot and background heat rates so as to expand the capability of the constructed NNs model for different operating conditions. The obtained results will be published at a later date.



Figure 12: NNs for predicting HS temperature and temperature ripple.

The performance accuracy of sample design tool shown in Figure 12 for the HS temperature prediction NN was above 99%. Additionally, the performance accuracy was 92% for temperature ripple NN prediction. Figure 13 and Figure 14, respectively, show the regression plots of both HS temperature and temperature ripple NNs.



Figure 13: Regression plot for the HS temperature NN.



Figure 14: Regression plot for the HS temperature ripple NN.

For the constructed NN model shown in Figure 12, a Graphical User Interface (GUI) was built to test the resulting NNs. The GUI is shown in Figure 15. As shown in this figure, the GUI is a simple tool to choose the four parameters that produce the wanted HS temperature and corresponding temperature ripple for the TEC device. Figure 15 shows the results of an example in which the hotspot and ripple temperatures are 38.41°C and 0.91°C, respectively.



Figure 15: HS temperature and ripple prediction tool GUI

The tool can also be used to find out the HS temperature for different ON time duration. This is important since the ratio of OFF time to ON time is needed for determining the supply electrical power to run the TEC, which is desirable to be as minimum as possible. Figure 16, shows that for OFF time duration of 1 s, the HS temperature starts to drop to the lowest value (38.41° C) at about 9 s if the random choice of initial current to be ON for about 100 s. In this case the minimum duty cycle in this setup is 1/9 (0.11) which means that about 11% of the supplied electrical power can be reduced compared to the case of applying constant electrical power at 4.5 A. However, the same lowest HS temperature can be reached if OFF time was set to 5 s and the ON time is about 16

s. The duty cycle is 5/16 (0.31) which means that 31% of TEC operating power can be reduced in this case.



Figure 16: HS temperature vs ON time when OFF time is 1 s and 5 s.

3. SUMMARY AND CONCLUSION

The work in this study was performed to investigate experimentally the potential use of thermoelectric technology for cooling microprocessors with optimal choice of operating parameters. In the first part of the experiment, the optimum electrical current to operate the TEC in its maximum cooling capability was determined. This current value was used in the second part of the experiment to generate pulsed electrical current instead of constant current. This was done to study the possibility of lowering the HS temperature while reducing the TEC operating power supply. The background heat flux was 0.73 W/cm^2 and a hotspot heat flux was 5.97 W/cm^2 which is equivalent to 3.48 W and 15.58 W respectively.

At the open circuit condition, the hotspot temperature was 89.3° C. The minimum HS temperature for steady-state experiment was 40.0° C at TEC operating current of 4.5 A. When pulsed current was used in the second part of the experiment, the HS we reduced to 38.0° C. The power supply was reduced by almost 31%. The HS temperature reductions at the steady-state and condition transient condition were 55% and 57%, respectively.

With a hotspot heat rate of 15.58 W and background heat rate of 3.48 W, neural network was used to construct a predicting tool. This tool was able to predict the HS temperature and the temperature ripple when four different parameters were used. These parameters were the initial TEC current, the duration of this initial current, the OFF time and the ON time. The developed tool in this study is currently being expanded to include different values of hotspot and background heat rates.

REFERENCES

- 1. D. Rowe. **THERMOELECTRICS HANDBOOK: MACRO TO NANO**, *CRC Press, Taylor & Francis Group*, 2000.
- 2. R. Viswanath,,W. Vijay, A. Watwe and V. Lebonheur. Thermal performance challenges from silicon to systems. *Intel Technol. J.*, Vol. 4, pp. 1–16, 2000.
- 3. ITRS, International Technology Roadmap for Semiconductors, 2004.
- H. Hamann, A. Weger, J. Lacey, Z. Hu, P. Bose, E. Cohen and J. Wakil. Hotspot limited microprocessors: Direct temperature and power distribution measurements. *IEEE J. Solid-State Circuits*, Vol. 4, pp. 56–65, 2007.

https://doi.org/10.1109/JSSC.2006.885064

- S. Pagani, P. Manoj, A. Jantsch and J. Henkel.Machine Learning for Power, Energy, and Thermal Management on Multicore Processors: A Survey. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 39, pp. 101-116, 2020.
- 6. S. Garimella. Advances in Mesoscale Thermal Management Technologies for Microelectronics. *Microelectron. J.*, Vol. 37, pp. 1165–1185, 2006.
- S. Garimella, V. Singhal and D. Liu. On-chip thermal management with microchannel heat sinks and integrated micropumps. *Proc. IEEE 94 (8)*, pp. 1534–1548, 2006.

https://doi.org/10.1109/JPROC.2006.879801

- C. Green, A. Fedorov and Y. Joshi. 2009. Fluid-to-fluid spot-to-spreader (F2/S2) hybrid heat sink for integrated chip-level and hotspot level thermal management. ASME J. Ele. Packag., Vol. 131, pp. 025002-1–025002-10, 2009.
- 9. V. Sahu, Y. Joshi and A. Fedorov. 2009. Hybrid solid state/fluidic cooling for hot spot removal. *Nanoscale Microscale Thermophys. Eng.*, Vol. 13, pp. 135–150, 2009.
- 10. N. Ahammed, G. Lazarus and S. Wongwises. **Thermoelectric cooling of electronic devices with nanofluid in a multiport minichannel heat exchanger**. *Experimental Thermal and Fluid Science*, Vol. 74, pp. 81-90, 2016.
- 11. Y. Cai,Y. Wang,D. Liu and F. Zhao. Thermoelectric cooling technology applied in the field of electronic devices: Updated review on the parametric investigations and model developments. *Applied Thermal Engineering*, Vol. 148, pp. 238-255, 2019.
- I. Chowdhury, R. Prasher, K. Lofgreen, G. Chrysler, S. Narasimhan, R. Mahajan, D. Koester, R. Alley and R. Venkatasubramanian. On-chip cooling by superlattice-based thin-film thermoelectrics. *Nature Nanotechnol*, Vol. 4, pp. 235–238, 2009. https://doi.org/10.1038/nnano.2008.417
- P. Wang, A. Bar-Cohen, B. Yang, G. Solbrekken and A. Shakouri. Analytical Modeling of Silicon Thermoelectric. *Microcooler. J. Appl. Phys.*, Vol. 100, p. 014501, 2006.

- 14. L. Goncalves, J. Rocha, D. Couto, P. Alpuim and J. Correia. **On-chip** Array of Thermoelectric Peltier. Microcoolers. Sens. Actuators. Vol. A145-146. pp. 75-80, 2008.
- 15. M. Gupta, M. Sayer, S. Mukhopadhyay and S. Kumar. Ultrathin Thermoelectric Devices for On-chip Peltier Cooling.IEEE Trans. Compon., Packag. Manuf. Technol., Vol. 1, pp. 1395-1405, 2011.
- 16. O. Sullivan, M. Gupta, S. Mukhhyopadhyay and S. Kumar. Array of Thermoelectric Coolers for On-Chip Management. Journal of Electronic Thermal Packaging, Vol. 134, pp. 1-8, 2012. https://doi.org/10.1115/1.4006141
- 17. R. Rao and V. Patel. Multi-objective optimization of two stage thermoelectric cooler using a modified teaching-learning-based optimization algorithm.*Engineering Applications* of Artificial Intelligence, Vol. 26, pp. 430-445, 2013.
- 18. A. Bar-Cohen and P. Wang. **On-chip** hot spot remediation with miniaturized thermoelectric coolers. Micrograv, Sci, Technol, Vol. 21, pp. 351-359, 2009.
- 19. V. Litivinovitch and A. Cohen. Effect of Thermal Contact Resistance on Optimum Mini-contact TEC Cooling on On-chip Hot Spots. Proceedings of Inter. PACK0'9, San Francisco, CA, 2009.
- 20. M. Redmond, K. Manickaraj, O. Sullivan and S. Kumar. Hotspot Cooling in Stacked Chips Using Thermoelectric Coolers. IEEE Transactions On Components, Packaging and Manufacturing Technology, Vol. 3, pp. 759-767, 2013.

https://doi.org/10.1109/TCPMT.2012.2226721

- 21. S. Alshehriand H. Saber. Experimental investigation of using thermoelectric cooling for computer chips. Journal of King Saud University – Engineering Sciences, Vol. 32, pp. 321-329, 2019.
- 22. S. Alshehri. Cooling Computer Chips with Cascaded and Non-Cascaded Thermoelectric Devices. Arabian Journal for Science and Engineering, Vol. 44, pp. 9105-9126. 2019.
- 23. H. Saber, S. Alshehri and W. Maref. Performance optimization of cascaded and non-cascaded thermoelectric devices for cooling computer chips.Journal of Energy Conversion and Management, Vol. 191, pp. 174-192, 2019.
- 24. M. Almaiah and M. Al-Zahrani. Multilayer Neural Network based on MIMO and Channel Estimation for Impulsive Noise Environment in Mobile Wireless Networks, International Journal of Advanced Trends in Computer Science and Engineering, Vol. 9, pp. 315-321, Jan. 2020.

https://doi.org/10.30534/ijatcse/2020/48912020

25. S. Panda, S. Mishra and M. Senapati. Detection and Classification Methods for EEG Epileptic Seizures, International Journal of Advanced Trends in Computer Science and Engineering, Vol. 8, pp. 2925-2934, Nov. 2019.

https://doi.org/10.30534/ijatcse/2019/40862019