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Two Stage Miller Compensated Op-Amp design in 180 nm CMOS for High Gain Methodology

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ABSTRACT
This paper discusses a CMOS two degree operational amplifier has been supplied which operates at 2.5 V power deliver at 180 nm era and whose input is th bandwidth operational amplifiers exists for certain applications. This requires research in the vicinity of op amp bandwidth extension without affecting different rusted Bias Current. The supply voltage has been scaled all the way down to lessen common power consumption of the system. The fundamental intention of our work is to lower energy dissipation, high gain and high swing. At huge supply voltages, there is a alternate-off amongst speed, strength and benefit. Performance of any circuit relies upon upon velocity, power and benefit. This op-amp has very low standby power consumption with a high driving capability and operates at low voltage so that the circuit operates at low strength.

Key words: CMOS, Two Stage Miller Compensated, OpAmp, High Gain

1. INTRODUCTION

Operational amplifier is most versatile and essential building block in analog signal processing packages. The operational amplifier (Op Amp) is a excessive benefit, DC coupled voltage amplifier with a differential input and, single or differential output to be used with negative feedback to exactly define a closed loop transfer characteristic. The number one requirements for an op amp are sufficiently big open loop benefit, massive team spirit advantage bandwidth, excessive input impedance, low output impedance, and high speed. These amplifiers are key factors of maximum of the analog subsystems, specially in switched capacitor filters. For previous couple of many years a CMOS implementation of analog circuits proved better than its contrary numbers because the equal generation can be used to put into effect analog as well as virtual building blocks at the identical chip [15].

Amplifier Operational amplifier is most flexible and essential constructing block in analog signal processing applications. The operational amplifier (Op Amp) is a immoderate advantage, DC coupled voltage amplifier with a differential enter and, unmarried or differential output to be used with bad remarks to exactly outline a closed loop transfer characteristic. The fundamental necessities for an op amp are sufficiently big open loop benefit, massive crew spirit benefit bandwidth, excessive input impedance, low output impedance, and excessive tempo. These amplifiers are key elements of maximum of the analog subsystems, especially in switched capacitor filters. For previous couple of many years a CMOS implementation of analog circuits proved higher than its opposite numbers because the same generation can be used to put in force analog further to virtual building blocks at the equal chip. This paper is targeted at the format of -degree unbuffered operational amplifier for use within unmarried chip mixed signal system [16, 17]. In order to obtain higher overall performance, MOS transistors are scaled down which facilitates incorporation of more quantity of transistors on identical chip. The non-forestall growth in processing capability in step with chip and working frequency is result of scaling. Scaling down of CMOS feature sizes allow yet faster speeds, the deliver voltage is scaled all of the way right down to decorate tool reliability and enhance electricity intake. Operational amplifiers are used as a essential building block in many analog and mixed signal structures [2, 3]. During designing of op-amp various electric powered characteristics which includes gain, offset, section margin, unity benefit bandwidth and so on. All have taken into consideration. To meet the preferred specification higher compensation method and topology needs to be decided on. Among various introduced topologies, right here we have selected up degree op-amp topology for excessive enter impedance and low output impedance. The first level offers high advantage and 2nd level provides huge output swing. In several op-amp packages, benefit with single stage isn't sufficient. To acquire better benefit greater ranges have to be delivered which gives extra phase shift to the system. For Closed loop circuit balance and well maintained importance and time response frequency repayment is wanted. The vital function of compensation approach is that they can boom the segment margin [4-7]. The recognition of a CMOS op-amp that combines a suitable gain with high cohesion advantage frequency has been a difficult problem [13]. Operational amplifiers (op-amps) designed o apprehend amazing degree functioning circuits beginning from clean dc bias technology to excessive speed sign conditioning or filtering. Operational amplifier can be used effectively for

practical outcomes as an instance switched capacitor designing, analog to digital converters and so on.[14].The goal of this paper is to perform a comparative assessment among diploma CMOS op-amp using miller compensation capacitor and stage CMOS op-amp the usage of reimbursement capacitor together with nulling resistor effect . Design has been performed in tanner EDA tool along facet simulation effects by using TSMC 180nm CMOS technology.

Operational amplifiers (op amps) are the maximum flexible and an vital part of many analog and blended-sign systems. They are hired from dc bias programs to excessive velocity amplifiers and filters. General motive op amps can be used as buffers, summers, integrators, differentiators, comparators, terrible impedance converters, and masses of other programs. Its overall performance makes fantastic effect on the analog structures. With the improved laptop aided design (CAD) tools, improvements of semiconductor modeling, regular miniaturization of transistor scaling, and the superior fabrication techniques, the integrated circuit marketplace is growing fast and continuously [15]. Nowadays, due to the company fashion of utilising desired process era to place into effect both analog circuits and digital circuits at the equal chip, complementary metallic-oxide semiconductor (CMOS) era has emerge as dominant over bipolar generation for analog circuit layout in a blended-sign gadget. While many digital circuits may be tailored to a smaller tool stage with a smaller strength deliver, maximum gift analog circuitry requires widespread change or maybe a redecorate to perform the same feat. With transistor period being scaled down to three tens of nanometers, analog circuits are becoming an increasing number of tough to improve upon. So, even as transistor is scaled, the better turns into its packing density, the better its circuit pace, and the lower its power dissipation [1]. The guidelines for analog circuits are pretty one in all a kind to those implemented to digital circuits. Voltage scaling plays important position in low strength circuit layout. However analog circuits advantage marginally from scaling, as the minimal length transistors cannot be utilized in analog circuits due to noise and offset voltage constraints. The primary difference is the important limits to the cut price of the energy consumption. Decreasing, the supply voltage sadly does not lessen the strength consumption of analog circuits [18]. This is in particular because of the truth that the energy consumption of analog circuits at a given temperature is essentially set with the useful resource of the specified sign-to-noise ratio (SNR) and the frequency of operation (or the required bandwidth).

2. RELATED WORK

The Operational Amplifier (Op-Amp) is a fundamental constructing block in Mixed Signal format. [8] D. Nageshwarrao,2013 labored on operational amplifiers that became an fundamental part of many analog and blended sign structures. As the call for for mixed mode included circuits will growth, the layout of analog circuits along side operational amplifiers in CMOS era turns into greater vital. Operational amplifiers with mild DC advantage, immoderate output swing and reasonable open loop Gain Band Width product (GBW) are generally executed with stage structures. This paintings offers a two level CMOS operational amplifiers, which has been designed, exhibits a Unity Gain Frequency (UGF) of 20MHz and a advantage of 42dB with 50 degree segment margin. To increase the benefit and segment margin new method has been proposed. Simulation effects are benefit of 48dB, concord gain frequency of 40MHz, Phase margin of 89 diploma. Design has been accomplished in Cadence tool.

[9] Ketan J. Raut,2014 supplied the layout of -level operational amplifier (Op Amp). The circuit became designed in favored 100 and eighty nm virtual n-properly CMOS technique. The design consists of very much less number of transistors, therefore the format is place optimized. Achieved open loop gain of the amplifier is seventy 4.89 dB. The harmony gain bandwidth (UGB) is 7.Three MHz and the phase margin is forty eight degree with a ten pF capacitive and 1 M ohm resistive load. The common power consumption of the amplifier is zero.402 mWand slew fee is 10 V/us.

[10] Shilpa Goyal,2015 worked With the continuous developing fashion inside the path of the decreased deliver voltage and transistor channel length, designing of immoderate normal overall performance analog incorporated circuits together with operational amplifier in CMOS (complementary steel oxide semiconductor) era turns into extra critical. In this paintings the 2 stage CMOS Operational amplifier (op-amp) has been designed using miller repayment technique which operates at 2.5V. Miller reimbursement technique has been hired with techniques, first is the usage of unmarried miller reimbursement capacitor even as second method uses unmarried miller compensation capacitor in collection with nulling resistor. To reap improved segment margin which advocate stability of a machine [13], new layout has been proposed with the assist of second method. The simulation become completed the use of TSMC 180nm CMOS technique and layout has been accomplished in tanner EDA tool While designing numerous elements are considered along with region, electricity, deliver voltage and cutting-edge. Thus, to advantage optimized universal performance devices are scaled down for this reason.. Along with terrible feedback configuration addition of every degree in multistage op-amps introduces some different pole within the machine which creates balance hassle. For this reason, a miller reimbursement technique has been hired in gadget.

Operational amplifier is keep in mind to be the most critical electronic tool. The method inscribed in this work is to layout a degree CMOS operational amplifier (Opamp) and analyze the effect of various parameters on the traits of Opamp layout. This paintings is specially specializing in format of optimized Opamp benefit. Keeping this as a prime element, Opamp specifications are taken under consideration, i.E., Gain, section margin, slew fee, power dissipation and others. [11] Kavyashree C L, 2017 afforded a layout and implementation of degree CMOS operational amplifier which operates at ±1V deliver voltage and

Simulation procedure is finished with the resource of the use of an EDA device cadence virtuoso with 90nm technology. The acquired benefit is 84db with segment margin of 560 and the energy dissipation is of 38.02µW The simulation has been finished the usage of Cadence device with 90nm technology. The benefit has been elevated through optimizing the parameters like (W/L) values. Using the design equations, by using using deciding on and punctiliously sizing the shape of the circuit. The layout plays a benefit of 84db with segment margin of 560 below unity advantage remarks configuration and the electricity dissipation is of 38.02µW.

A need for high bandwidth operational amplifiers exists for certain applications. This requires studies in the area of op amp bandwidth extension with out affecting distinctive parameters notably. [12] Goyal, 2015 mentioned the winning repayment techniques for operational amplifiers and present day buffer compensation approach has been followed to format a high advantage low electricity operational amplifier. This approach offers advanced gain-bandwidth product (GBW) with right swing. The proposed classic two-diploma op amp produces an open loop benefit above seventy eight dB, gain- bandwidth product (GBW) of five.82 MHz and 63.9o segment margin in 0.18 µm CMOS generation. The circuit is operated on the deliver voltage of three.Three V with electricity dissipation of 154.3µW. The capability of the method adopted, to use the smaller repayment capacitor, Cc, which improves the slew charge, additionally useful for the vicinity of compensation circuit.

3. METHODOLOGY

Operational amplifiers are an integral a part of many analog and combined sign structures. Opamps with vastly exclusive degrees of complexity are used to comprehend functions ranging from dc bias generation to high speed amplification or filtering. In this chapter ideal op amp and its parameters values [14], fundamental op amp shape and its parameters inclusive of advantage bandwidth product, commonplace mode rejection ratio, power deliver rejection ratio and many others are mentioned. Ideally op amp is differential amplifier with two inputs and one output, endless gain, limitless enter resistance in order that no loading impact can arise and zero output resistance.

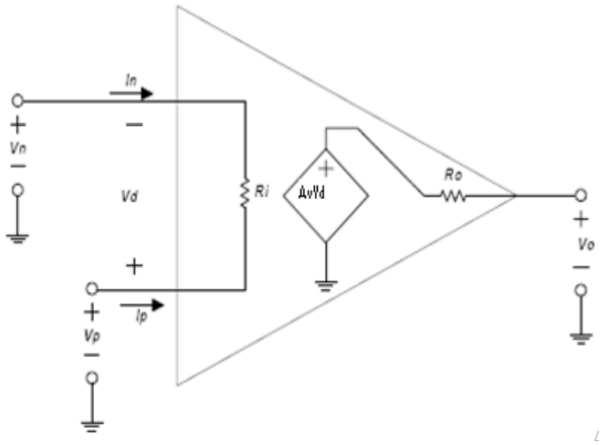

Figure 1: Standard op amp notation

The Thevenin amplifier version is shown in Fig. 1 beneath, displaying trendy op amp notation. It amplifies the voltage difference, Vd = Vp - Vn, on the enter port and produces a voltage, Vo, at the output port this is referenced to floor. The perfect op amp version was derived to simplify circuit calculations and is typically utilized by engineers in first order approximation calculations. The best version makes 3 simplifying assumptions:

- Gain Av = ∞
- Input Resistance Ri =∞
- Output Resistance Ro = 0

Applying these assumptions to Fig. 1 results in the ideal op amp model shown in Fig. 2

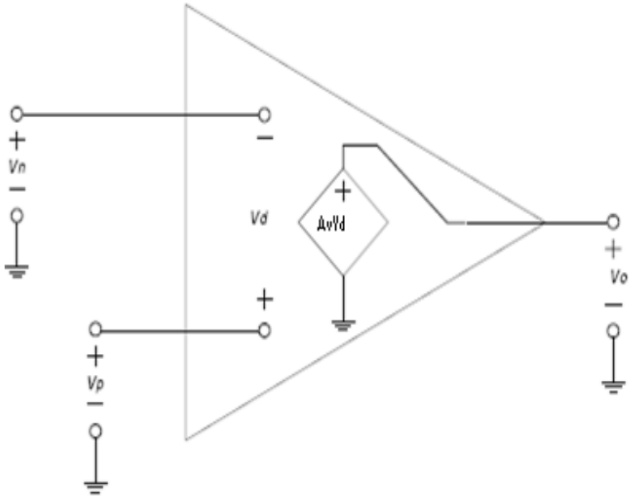

Figure 2: Ideal op amp model

The level circuit structure has historically been the maximum popular approach to Op-Amp design. It can provide high gain and excessive output swing. It is an tremendous instance to illustrate many critical design principles that area additionally immediately applicable to other designs. The -stage refers to the wide variety of gain degrees inside the Op-Amp shown in Fig 3. The output buffer is typically present simplest when resistive loads desires to be driver. If the burden is purely capacitive, it is not wished. The load is thought capacitive. The first degree is a pMOS differential pair with nMOS current mirrors. Second stage is a not unusual-supply amplifier.

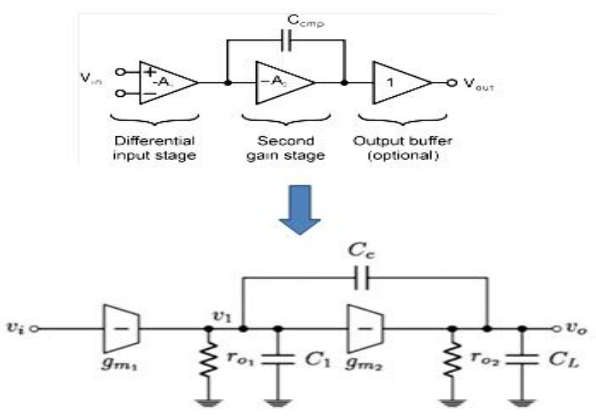

Figure 3: Two stage architecture

4. RESULT AND DISCUSSION

The amplifier is to be powered from a 1.8 volts power supply. The different bias voltages which are required by op amp circuit are produced by bias circuit. Based on the proposed compensation technique a CMOS op amp has been designed and simulated in a standard 0.18 µm CMOS technology. The power consumption is 523 microwatt. Fig 4 shows the Op-Amp Schematic.

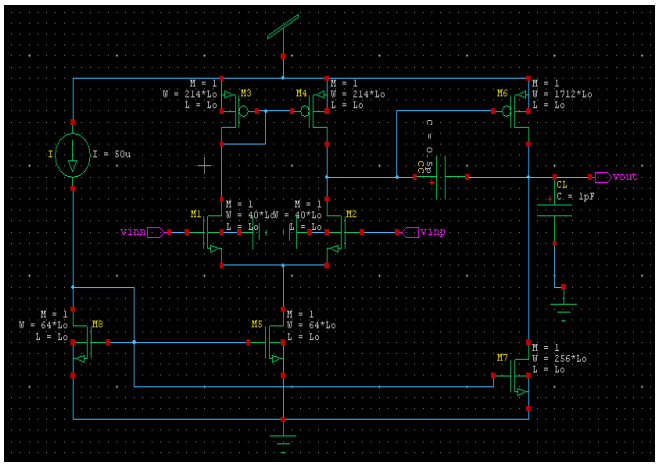

Figure 4: Proposed Op-Amp Schematic

Figure 5: Specification of Two Stage op-Amp Design

DC gain	1000 = 60 dB
Phase Margin	(PMmin) = 60°
Slew Rate	20 V/µs
Input Common Mode Range	(ICMR+)= 1.6 V
Input Common Mode Range	(ICMR-)= 0.6 V
Power dissipation	$(PD)_{max}$ = 300 µW
Gain Band Width product	(GBW) = 30 MHz

In this paper we are working on 180nm CMOS (Vdd= 1.8V); Lmin= 180 nm and CL= 2pF mention in fig 5.

Step 1: Extraction of Technology parameters for Design process shown in below fig 6.

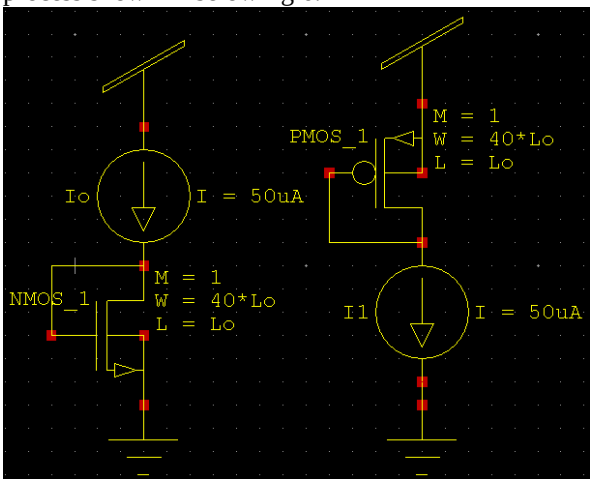

Figure 6: Experimental setup for technological parameter extraction

$\mu_p C_{ox}$ = 60 µA/V^2 (for L= 500 nm)

$\mu_n C_{ox}$ = 300 µA/V^2 (for L= 500 nm)

Step 2: Op-Amp Design and DC simulation (Verifying ICMR)

- At ICMR+ = 1.6 V: All Transistors in Saturation (with Gm= 543 µS for M1 and M2), P_D =584 µW
- At ICMR- = 0.6 V: All Transistors in Saturation (with Gm= 483 µS for M1 and M2), P_D =550 µW

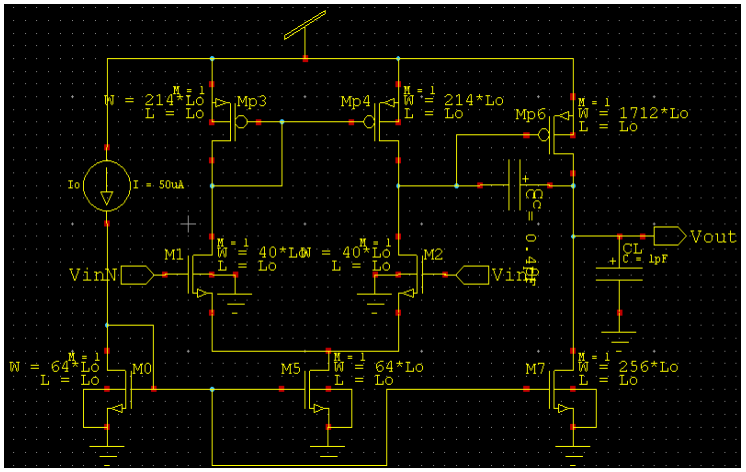

Figure 7: Two stage miller compensated Op-Amp schematic

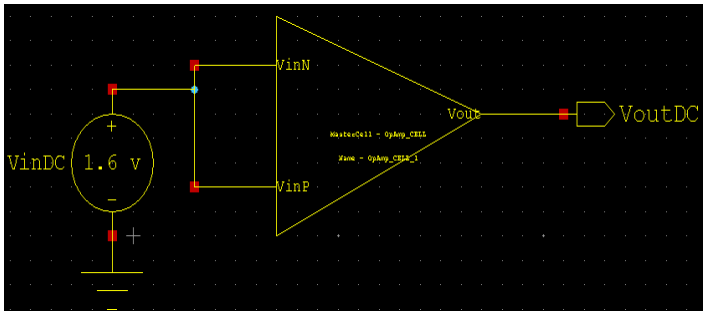

Figure 8: Dc analysis validation for ICMR and Gm

Figure 7 shows the two stage miller compensated Op-Amp schematic and fig 8 shows the Dc analysis validation for ICMR and Gm

Step 3: AC simulation (Verifying DC gain, GBW and Phase Margin)

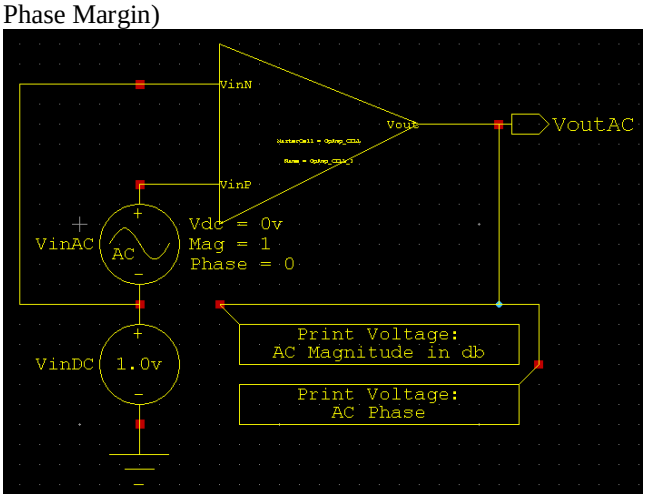

Figure 9: AC analysis validation for frequency response (GBW and phase margin)

Phase Margin achieved: 57^o
DC gain= 72 DB
GBW= 32 MHz
Fig 9 shows the AC analysis validation for frequency response between GBW and phase margin.

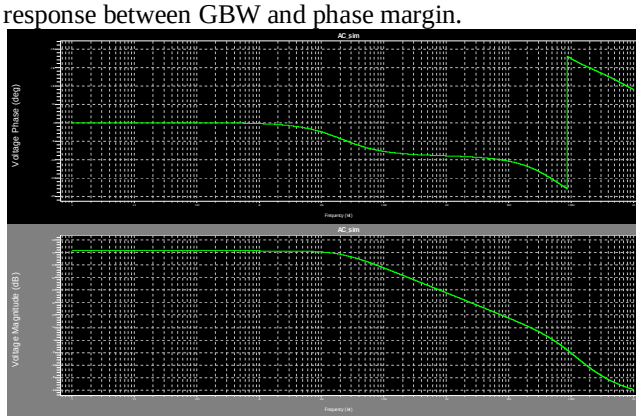

Figure 10: Frequency response of proposed Op-amp (GBW and phase margin)

Fig 10 shows the frequency response of Op-amp between GBW and phase margin.

Step 4: Transient simulation of Op-Amp in negative feedback (Verifying slew rate)

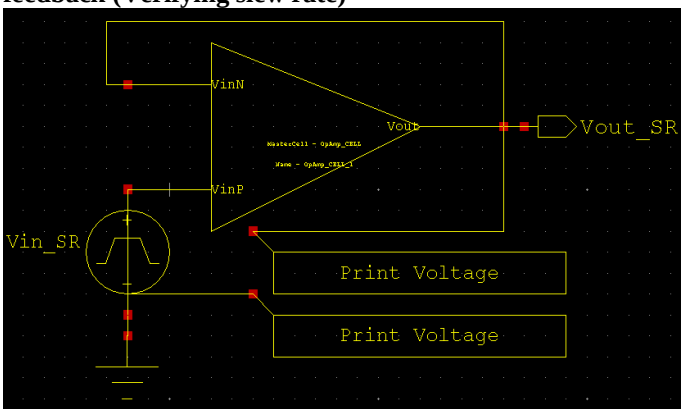

Figure 11: Slew rate setup validation

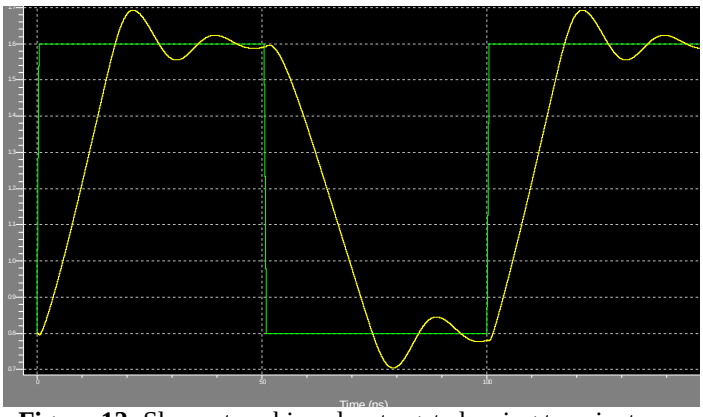

Figure 12: Slew rate achieved as targeted, using transient simulation

Measuring slew rate from step response: SR = 24 V/µs. Fig 11 shown the slew rate for setup validation and Fig 12 shows the slew rate archive that has been targeted using transient simulation.

5. CONCLUSION

In this thesis a two stage high gain low power operational amplifier has been designed. In the design of the operational amplifier the compensation capacitor play an important role for power consumption and noise parameters. As the power consumption decreases with the compensation capacitor value, current buffer approach has been used which is less sensitive to process variations. The operational amplifier has been designed and simulated using Tanner EDA (SPICE Platform) in 0.18 µW CMOS-1.8V process technology. The operational amplifier achieves dc gain 60 dB, unity gain bandwidth 30 MHz, phase margin 60°.

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