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Design of Reversible Decoder with minimum Garbage Output

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ABSTRACT

Reversible logic is helpful in designing low power applications. Many reversible gates have been introduced in recent time for use in reversible computing. Those gates are used in the design of various circuits. In some works, decoders using reversible logic have been also proposed. This paper proposes three new reversible gates that can perform multiple logical operations alone. Using these gates, new circuits for 2-to-4 and 3-to-8 decoders are proposed followed by two new designs for general decoder. The performances of the proposed decoder circuits are studied in terms of hardware complexity, power, gate count, number of ancilla inputs and garbage outputs. Comparisons of these circuits with similar existing decoder circuits are also presented. The proposed circuits are found to have better performance characteristics particularly garbage output is least amongst available designs.

Key words : Ancilla input, Garbage output, Reversible decoder, Reversible gate, Reversible logic.

1. INTRODUCTION

Heat dissipation has been a major challenge in conventional electronics. Landauer in [1] has described how erasing of bits leads to heat dissipation. The idea of reversibility has emerged to overcome this issue in traditional irreversible logic. Bennett has also shown in [2] the usefulness of reversibility to overcome the challenge of heat dissipation. Reversible logic has drawn attention of many researchers latterly.

There are many literatures available on reversible logic; starting from gates, circuits to synthesis. Peres, Fredkin, Toffoli, Feynman, etc. [3] are some reversible gates widely discussed. Other reversible gates are also proposed [4]-[8]. Many more reversible gates can be designed. For example, 8!=40,320 numbers of 3-input reversible gates are possible [9]. Various circuits for reversible adder [3],[7], comparator [10], multiplexer [11], multiplier [12],[13],[14], flip-flops [8],[11],[15], counters [8],[15], registers [11], encoders [16],[17], decoders [8,17-25], etc. are proposed in literatures. Design of Arithmetic and Logic Unit (ALU) [26] are presented in [3],[6],[27] using reversible logic. Other reversible approaches like quantum dot cellular automata [28] are also popular these days.

The quantum gate libraries are used to map a reversible gate or a reversible circuit into a quantum circuit [29]. This mapping manipulates classical Boolean values so that these reversible functions can be used in quantum computing. The quantum cost of a gate or circuit can be derived with reference to the gate library considered in [29]. One such popularly used library is the NCV gate library [30] comprising of the gates: NOT, controlled-NOT (CNOT), controlled-V, and controlled-V^+ [30],[31]. In quantum computing, these four gates are treated as the primary gates [31].

This paper is arranged as follows: Section-2 introduces to the background and objectives of this work. Relevant definitions are presented in Section-3. Section-4 proposes new reversible gates. In Section-5, new designs of reversible decoders are proposed. Section-6 presents performance comparison of the proposed decoders with similar available designs. Section-7 concludes the paper.

2. BACKGROUND AND OBJECTIVES

A digital decoder [27] uniquely decodes logically-related bit patterns to its outputs. For example, in binary to octal decoder, input is in the binary form and output is the octal equivalent of the input binary number. Decoders are widely used in computer as well as in communication and signal processing techniques.

There are not many works reported on reversible decoder circuits. Authors in [8] propose a 2-to-4 decoder with a new reversible gate and a 3-to-8 decoder circuit with the new gate along with the Fredkin gate. A general design for *n-to-*2^n decoder is also presented. The circuit for reversible 2-to-4 decoder proposed in [17] uses the Feynman, control V and control V^+ gates. In [18], authors present a 2-to-4 decoder with the Feynman and Fredkin gates. A general design for *n-to-*2^n decoder is also presented here. New designs for 2-to-4 and 3-to-8 decoders are proposed in [19] along with a circuit for *n-to-*2^n decoder by using a new gate and the Fredkin gate. The new circuit for 3-to-8 decoder presented in [20] uses the Fredkin and DVSM gates. In [21], authors design 2-to-4, 3-to-8 and 4-to-16 decoders by using the R-I and NOT gates.

The *n-to-*2^n decoder design proposed in [22] uses a modified Fredkin gate and the Feynman gate. Authors in [23] use the Toffoli and Feynman gates to present a general model for *n-to-*2^n decoder. In [24], authors present 2-to-4, 3-to-8 and 4-to-16 decoders by using the Fredkin, Feynman and Peres gates. Design of a 2-to-4 decoder is proposed in [25] with the Peres, Feynman and NOT gates.

The performances of reversible logic circuits are usually evaluated in terms of power, number of gates, number of garbage outputs and number of ancilla inputs [6],[20]. Designer of reversible circuit attempts to optimize these parameters. To decrease the number of qubits in quantum circuit, the number of garbage outputs and ancilla inputs is needed to be minimized [32]. The 2-to-4 decoder in [8] has the minimum number of garbage outputs and ancilla inputs among all the 2-to-4 decoder circuits discussed above. The number of garbage outputs and ancilla inputs is minimum for the circuits in [8],[20]. Among the *n-to-*2^n decoder circuits in [8] has the minimum number of garbage outputs and ancilla inputs.

It may be noted from the discussion above that

- low-cost decoder design is still a challenge to be appropriately addressed and people are trying to achieve better designs.
- new reversible gates are introduced to design circuits for specific operations. For example, new gates are introduced in [8],[19] to design decoders.

Considering these observations, the present work aims to design

- new reversible gates which can help to construct decoder circuits with lesser costs.
- new circuits for 2-to-4 and 3-to-8 decoders for improved performance.
- new circuits for n-to-2^n decoder for improved performance.

3. BASIC DEFINITIONS

This section presents various definitions related to the domain of reversible logic and decoder.

3.1 Reversible logic

Definition 1: A reversible logic is an n-input and n-output function $f: B^n \rightarrow B^n = \{0,1\}$ that satisfies one-to-one and on-to mapping among the inputs and outputs [8]. Hence, the inputs to a reversible logic can be derived back from its outputs.

3.2 Reversible gate

Definition 2: A reversible gate is a logic gate with n-input and n-output lines that satisfies one-to-one and on-to mapping [8],[9]. Reversible gate implements a reversible logic function, and hence Definition-2 holds here.

3.3 Reversible logic circuit

Definition 3: A reversible logic circuit is a combinational circuit realized with cascade of reversible gates without any feedback and fan-out [9],[30]. Definition-2 also holds here as reversible logic circuit implements a reversible logic function.

3.4 Quantum cost

Definition 4: For a reversible gate (or circuit), quantum cost is the number of elementary quantum gates required to represent the gate (or circuit) [29],[33]. As circuits are reversible in quantum technology, quantum cost is popularly used as a performance measure for reversible gates and circuits [29]. It can be obtained by using the methods discussed in [30], [31].

3.5 Ancilla input

Definition 5: In reversible logic circuit, an ancilla input is a constant input line [8]. The ancilla inputs appear as qubits in quantum circuit. Hence, the ancilla count (number of ancilla inputs) is expected to be minimum possible in a reversible circuit to achieve optimization [32].

3.6 Garbage output

Definition 6: In reversible logic circuit, a garbage output is an unused output line [8]. It is desired that the garbage count (number of garbage outputs) be minimum possible in a reversible circuit to reduce the number of qubits in the equivalent quantum circuit [32].

3.7 Gate count

Definition 7: In a reversible logic circuit, gate count is the number of gates used in the circuit [8]. A lower gate count helps to achieve compactness of circuit [5].

3.8 Decoder

Definition 8: Decoder is a digital combinational circuit which converts *n* binary inputs to 2^n distinct outputs [26]. Decoders are used in computer to translate instructions into signal in control unit. Communication system, monitor, printer, etc. also use decoder. Decoders may be also used to design full adder, multiplexer, and comparator.

3.9 Hardware complexity

Definition 9: Total Number of XOR, AND and NOT etc. operations performed by a circuit or gates is called hardware complexity. For example, in a circuit if α number of OR operations is performed, β number of AND operations performed and γ number of NOT operations performed, then the hardware complexity is $\alpha+\beta+\gamma$. The following section presents new reversible gates with their definitions and properties.

4. PROPOSED REVERSIBLE GATES

This section proposes three new reversible gates: Names are given as OM, SOM and UM gates. These gates are discussed in detail in the following with their block diagrams and truth tables.

4.1 OM Gate

Definition 10: If *A, B, C* are inputs and *X, Y, Z* are outputs of the *3X3* OM gate, then

$$X = A,\ Y = A.B \oplus \overline{C} \text{ and } Z = \overline{A}.B \oplus \overline{C}$$

The OM gate is presented in figure 1. It can perform the following Boolean operations:

- NOT operation : when *A=0* or *B=0*, then $Y=\overline{C}$
- AND operation : when *C=1*, then $Y=A.B$
- NAND operation : when *C=0*, then $Y=(A.B)$

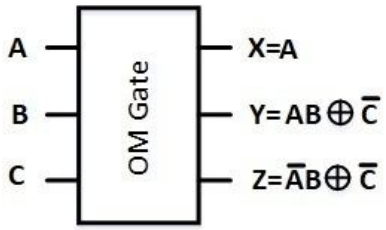

Figure 1: Block diagram of OM gate

Table 1: Truth table of OM gate

A	B	C	X	Y	Z
0	0	0	0	1	1
0	0	1	0	0	0
0	1	0	0	1	0
0	1	1	0	0	1
1	0	0	1	1	1
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0

The truth table of the OM gate is shown in table 1. Here, A, B ,and C are input and X, Y, and Z are output. The table shows that the input side has one to one mapping with the output, the gate is reversible.

4.2 SOM Gate

Definition 11: *If A, B, C, D* are inputs and *W, X, Y, Z* are outputs of the *4X4* SOM gate then

$$W = A.B \oplus C \oplus D, X = A.\overline{B} \oplus C$$
$$Y = \overline{A}.B \oplus C \oplus D, Z = \overline{A}.\overline{B}.\oplus C \oplus D$$

The SOM gate is shown in figure. 2. The following Boolean operations can be performed by this gate:

- NOT operation: when *A=1* and *C=0*, then $X=\overline{B}$
- AND operation: when *C=0* and *D=0* then *W=A.B*
- XOR operation: when *A=1* or *B=0* then *Y=C xor D*
- NAND operation: when *C=0* and *D=1* then $W=\overline{(A.B)}$
- XNOR operation: when *A=0* and *B=0* then $Z=\overline{(C \text{ xor } B)}$

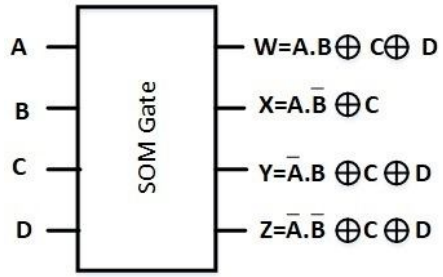

Figure 2: Block diagram of SOM gate

Table 2: Truth table of SOM gate

A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	0	1
0	0	0	1	1	0	1	0
0	0	1	0	1	1	1	0
0	0	1	1	0	1	0	1
0	1	0	0	0	0	1	0
0	1	0	1	1	0	0	1
0	1	1	0	1	1	0	1
0	1	1	1	0	1	1	0
1	0	0	0	0	1	0	0
1	0	0	1	1	1	1	1
1	0	1	0	1	0	1	1
1	0	1	1	0	0	0	0
1	1	0	0	1	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	1
1	1	1	1	1	1	0	0

The truth table of this gate is shown in table 2. In the table, A, B, C, and D are input and W, X, Y, and Z are output.

4.3 UM Gate

Definition 12: If *A, B, C, D, E, F* are inputs and *U, V, W, X, Y, Z* are outputs of the *6X6* UM gate, then

$$U = A \qquad V = AB \oplus \overline{C}$$
$$W = \overline{A}.B \oplus \overline{C} \qquad X = A \oplus D$$
$$Y = D.E \oplus \overline{F} \qquad Z = \overline{D}.E \oplus \overline{F}$$

The UM gate is presented in figure. 3. The Boolean operations which can be performed by using the UM gate includes:

- NOT operation: when *A=0* or *B=0* then $V=\overline{C}$
- AND operation: when *C=1* then *V=A.B*
- XOR operation: *X=A xor B*
- NAND operation: when *C=0* then $V=\overline{(A.B)}$

Besides the above operations, Copy (or Transfer) operation of bit can be performed using the UM gate. For example, if input D=0, then copy of input bit A can be found at output X, similarly if input A=0, then copy of input bit D can be found at output X.

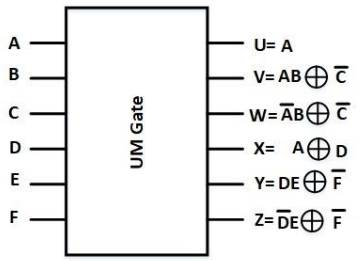

Figure 3: Block diagram of UM gate

The truth table of UM gate is not presented here.

In the following, new circuits for reversible decoders are proposed by using the OM, SOM and UM gates.

5. PROPOSED REVERSIBLE DECODER CIRCUITS

This section presents new circuits for 2-to-4 and 3-to-8 reversible decoders. Two general designs for *n-to-2*^{n} decoder are also proposed. The decoder circuits are verified by simulating in the HSPICE.

5.1 Circuits for reversible 2-to-4 decoder

In a 2-to-4 decoder with inputs A and B, the four desired logical outputs area A.B, $\bar{A}$.B, A.$\bar{B}$ and $\bar{A}$.$\bar{B}$. Here, two new circuits for 2-to-4 decoder are introduced. The first design uses the UM gate as shown in figure. 4. This design needs the input bit A twice and also the bit B twice. As fan out is not allowed in reversible circuit, two Feynman gates are required to copy these bits. This yields an extra quantum cost of 2.

To reduce the cost further, another design is proposed as shown in figure. 5. This design uses the SOM gate only.

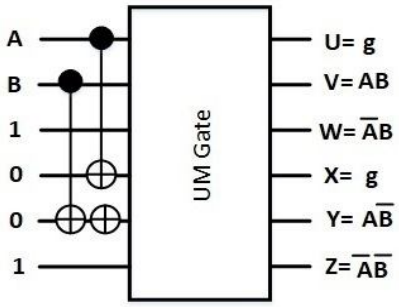

Figure 4: 2-to-4 decoder using UM gate

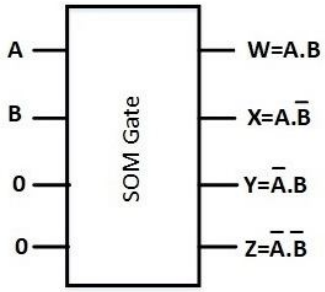

Figure 5: 2-to-4 decoder using SOM gate

The performance parameter values for these decoder circuits are shown in table 3. It may be noted from the table that the costs of the decoder in figure. 5 are lesser in comparison to the first design in figure. 4. It may be also observed that the decoder with the UM gate has a gate count of 4 and the design with the SOM gate has a gate count of 1. In the decoder with the UM gate, the number of ancilla inputs and garbage outputs is 6. The decoder with the SOM gate has 2 ancilla inputs and no garbage output. Therefore, the proposed 2-to-4 decoder by using the SOM gate has better performance parameter values. New 3-to-8 decoder designs are proposed in the following with the SOM gate as 2-to-4 decoder at the core.

Table 3: Performance of the proposed 2-to-4 decoder designs

Parameters	UM Gate	SOM Gate
Ancilla Count	4	2
Garbage Count	2	0
Gate Count	1	1
Hardware Complexity	2(β+γ)	β+2γ
Power	0.246μW	0.283μW

From the table 3, it can be noted that SOM gate based decoder is better. The ancilla count twice less than the UM gate based decoder. Also, in this decoder is garbage output is nill, on the other hand the UM gate based decoder has 2 garbage output.

New 3-to-8 decoder designs are proposed in the following with the SOM gate as 2-to-4 decoder at the core.

5.2 Circuits for reversible 3-to-8 decoder

In the first design for 3-to-8 decoder, the outputs of the 2-to-4 decoder (SOM gate) are connected to two UM gates as shown in figure. 6. This design needs the input bit I_2 twice in each UM gate. Therefore, the two Feynman gates in the circuit contribute an additional.

The second design attempts for an improved realization with the SOM and OM gates as shown in figure. 7. The 2-to-4 decoder at the core is similar to the one used in the first design. One OM gate is connected to each output of the 2-to-4 decoder. The performance parameter values for the two decoder circuits are presented in table 4. It may be noted from the table that the number of gates used in each of the decoder circuits is 5. The decoder circuit in figure. 7 has less number of ancilla inputs and garbage outputs.

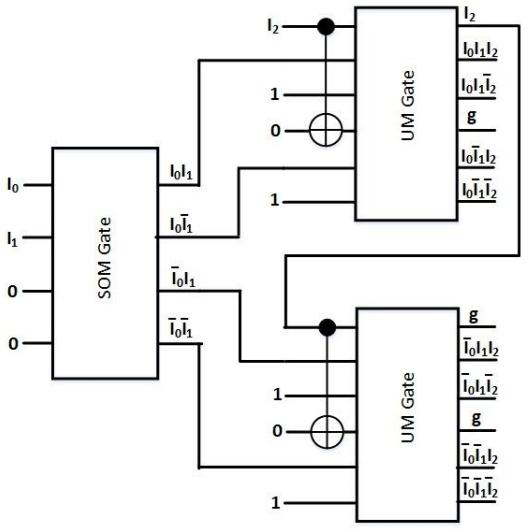

Figure 6: 3-to-8 decoder using SOM and UM gate

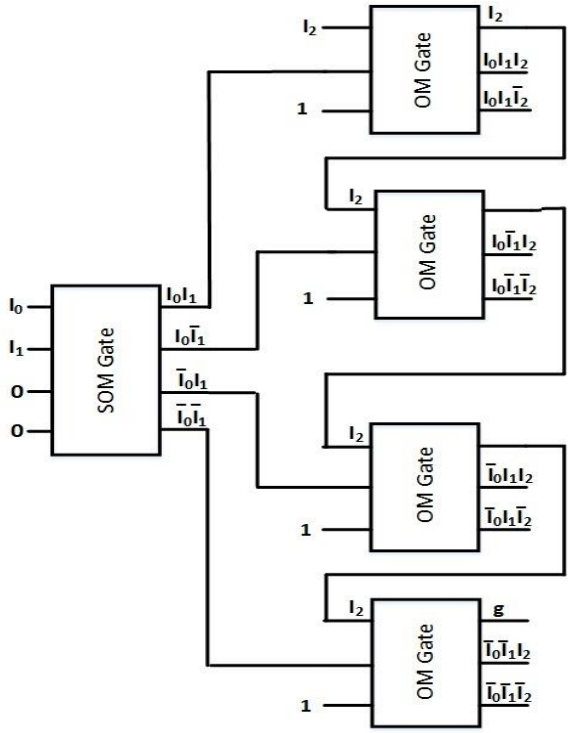

Figure 7: 3-to-8 decoder using SOM and OM gate

Table 4: Performance of the proposed 3-to-8 decoder designs

Parameters	SOM/UM Gate	SOM/OM Gate
Ancilla Count	4	2
Garbage Count	2	0
Gate Count	5	5
Hardware Complexity	5β+6γ	5(β+2γ)
Power	0.637μW	0.588μW

5.3 Circuits for reversible *n-to-2^n* decoder

The first design for *n-to-2^n* decoder is an extension of the 3-to-8 decoder with the SOM and UM gates. The 3-to-8 decoder in figure. 6 can be extended to realize a 4-to-16 decoder by using 2 more UM gates after each UM gate in the 3-to-8 decoder circuit. Therefore, a reversible *n-to-2^n* decoder can be derived by adding 2^{n-2} numbers of UM gates after the *(n-1)-to-*2^{n-1} decoder circuit. This design is shown in Figure. 8. The various parameters for the design may be derived to be as follows.

Gate Count : $2^n - 3$

Ancilla count : $3x2^{n-1} - 4$

Garbage count : $2^{n-1} - 1$

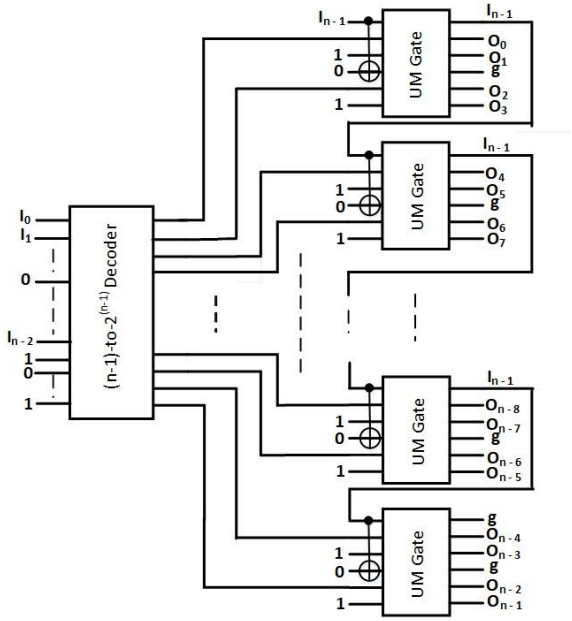

Figure 8: *n-to-2^n* decoder using SOM and OM gate

In a bid to improve circuit performances, another design for *n-to-2^n* decoder is proposed as shown in figure. 9 which uses the SOM and OM gates. Here, the 3-to-8 decoder in figure. 7 is used as a basic structure upon which additional layers are built to derive the *n-to-2^n* decoder. By using 2 more OM gates after each OM gate, the 3-to-8 decoder circuit in figure. 7 may be expanded to derive a 4-to-16 decoder. Hence, in the *n-to-2^n* decoder circuit, there will be 2^{n-1} number of OM gates after the *(n-1)-to-*2^{n-1} decoder circuit.

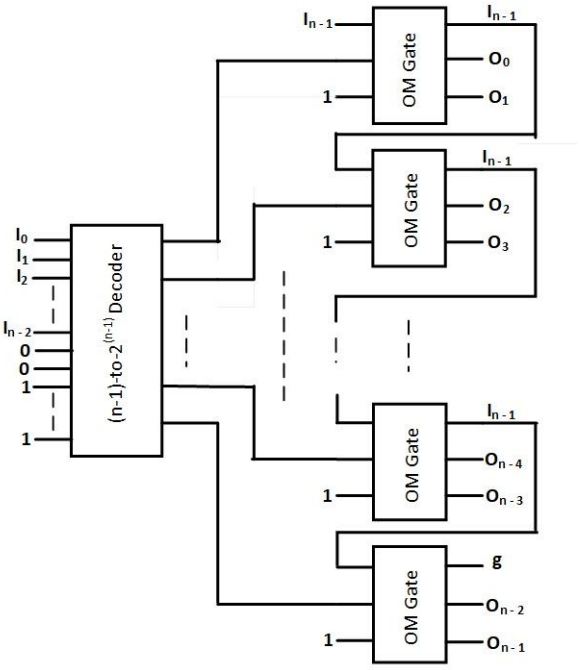

Figure 9: *n-to-2*^{n} decoder using SOM and OM gate

The performance parameters of this design are as follows.

Gate Count : $2^n - 3$

Ancilla count : $2^n - 2$

Garbage count : *1*

The following section presents a comparison of the proposed decoder circuits with existing similar decoder designs.

6. PERFORMANCE COMPARISON

The proposed 2-to-4 decoder circuits are compared with other available designs in table 5. The gate count and the count of ancilla inputs and garbage outputs of this circuit match with those of the decoder designs in [8], [17] and [25]. However, these values are the minimum for these parameters.

Table 5: Performance comparison of the proposed 2-to-4 decoder designs.

Decoder Circuit	Gate Count	Ancilla Count	Garbage Count
Proposed, Figure. 5	1	2	0
Proposed, Figure. 4	3	4	2
Ref[8]	1	2	0
Ref[17]	1	2	0
Ref[18]	3	3	1
Ref[19]	1	4	2
Ref[21]	4	1	2
Ref[22]	3	3	1
Ref[24]	6	5	3
Ref[25]	6	2	0

Table 6: Performance comparison of the proposed 3-to-8 decoder designs.

Decoder Circuit	Gate Count	Ancilla Count	Garbage Count
Proposed, Figure. 7	5	6	1
Proposed, Figure. 6	5	8	3
Ref[8]	5	6	1
Ref[18]	7	8	3
Ref[19]	5	8	3
Ref[20]	5	6	1
Ref[21]	8	5	3
Ref[22]	7	7	7
Ref[23]	10	8	3
Ref[24]	10	9	4

It may be also noted that the proposed decoder in figure. 7 has better performance characteristics in comparison to the proposed decoder in figure. 6. The gate count and the number of ancilla inputs and garbage outputs for this decoder are similar to those of some existing designs. However, these values are the minimum for these parameters.

In table 6, the proposed 3-to-8 decoder circuits are compared with their available peers. From the table it can be noted that [8], [20] and [21] has least gate count. The proposed design in figure 7 has also the same least gate count. The ancilla count in [24] is the minimum, however our proposed design in figure 7 one more than that. The garbage count is least in [8] and [20]. The proposed decoder in figure 7 has also the same minimum value.

Finally, a performance comparison for the proposed *n-to-2*^{n} decoder circuits is presented in table 7. It may be observed from the table that both the proposed circuits in figure. 8 and 9 have lower garbage output in comparison to the other existing designs. The design in figure. 9, has the least garbage output among all decoders. Except for the designs proposed in [18], [22] and [23], other designs in table 7 have the same gate count. The gate count for the design in [23] is evaluated little differently, where a nesting structure is considered. In the designs presented in [18] and [22], the gate count is marginally higher. The proposed circuit as shown in figure. 9, the number of ancilla inputs is also minimum. To be noted that the garbage count for this circuit is fixed and is equal to 1. Hence, notable improvement is found in the number of ancilla inputs and garbage outputs. From the result it is observed that the garbage output is the minimum.

Table 7: Performance comparison of the proposed *n-to-2*^{n} decoder designs

Decoder Circuit	Gate Count	Ancilla Count	Garbage Count
Proposed, Figure 9	$2^n - 3$	$2^n - 2$	1
Proposed, Figure 8	$2^n - 3$	$3x2^{n-1} - 4$	$2^{n-1} - 1$
Ref [8]	$2^n - 3$	$2^n - 2$	n - 2
Ref [17]	$2^n - 1$	2^n	n
Ref [18]	$2^n - 3$	2^n	n
Ref [21]	$2^n - 1$	$2^n - 1$	$2^n - 1$
Ref [22]	10	2^n	n

7. CONCLUSION

This paper has introduced three new reversible gates with their definitions and characteristics. The new 2-to-4 decoder derived with the SOM gate has been found to have the minimum garbage output when compared with existing designs. This manuscript has also introduced two new circuits for 3-to-8 decoder. In this case also garbage count is minimum. The power analysis is done for the proposed 2-to-4 and 3-to-8 decoders (figure 4 to figure 7). These values of power are reported in Table 3 and Table 4. The HSPICE tool is used for the analysis.

These 3-to-8 decoder circuits have been scaled up to derive two general designs for *n-to-2*^{n} decoder. After performance comparison with similar existing decoders, it has been found that the decoders derived with the SOM and OM gates have notable improvements in terms of the garbage output. From table 7, it is observed that the garbage output is the minimum among all the available designs. The count of ancilla inputs is also at par with the available minimum value. Similarly, gate count is also amongst the list of available minimum value. One future work will be to optimize the gate count. More suitable reversible gates and circuits may be also designed to improve decoder performance.

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