ISSN 2278-3091
Volume 8, No.6, November – December 2019
International Journal of Advanced Trends in Computer Science and Engineering
Available Online at http://www.warse.org/IJATCSE/static/pdf/file/ijatcse141862019.pdf
https://doi.org/10.30534/ijatcse/2019/141862019

Delay Estimation of Different Approximate Adders using Mentor Graphics

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ABSTRACT

In these paper comparisons of different types of approximate adders. Comparing the parameters like delay and power dissipation among approximate adders like carry look ahead adder, hybrid adder, reverse carry propagate adder. Usage of these adders where exactness is not required these adders produce approximate results which may suffice the requirement of the user. The implantation of these adders is done in a mentor graphics tools using 130 nm technology. Average improvement of 27% delay and also high accuracy is observed.

Key words: Accuracy, approximate, exactness, hybrid, reverse carry propagate adder.

1. INTRODUCTION

Adders are chiefly utilized in math rationale units. Adders likewise can perform numerous other math tasks, for example, subtraction, increase and dissection which are control devouring tasks in workstation. Decreasing the postpone and power utilization is a significant testing task. The power utilization decrease and speed improvement are the key points in the plan of computerized preparing units, particularly the versatile frameworks. Regularly, an expansion in the speed is accomplished at the expense of more power utilization for precise preparing units. The best ways to deal with is to make improvements in both the power and speed is in fining the calculation precision. This methodology, that are surmised figuring, potency utilized in the applications where few mistakes may be tolerated.

Adders, which are the primary parts in number juggling units of DSP frameworks, which are regulation eager and regularly structure problem area areas on the kick the bucket. These realities have been the inspirations for understanding this part utilizing the inexact registering approach. Earlier inquires about on rough adders have adopted binary regular strategies of concentrating on blunder weight and blunder likelihood decreases. The first method relies on a half-and-half structure adder that uses two different parts, accurate MSBs, and inaccurate least notable bits (LSBs). The blunder looks in the convey contribution of the most correct section of the critical piece (MSB) and the total sum in the smallest significant part. It limits the fault weight to the MSB's conveyance contribution. Since the larger part of the exercises typically occurs in the smallest significant bit part, the regulation may be achieved by using the cross-breed adder method. Unadulterated rough adder systems are used in the following methods. For these adders, the main approach is delay, dropping the blundering probability of total sum as well as decreasing control.

2. RELATED WORKS

Basically, adders are of two types conventional adders and approximate adders. The conventional adders produce constant outputs and the circuit equations cannot be modified where as in approximate adders the circuit equations can be modified. Approximate adder are the modified versions of conventional adders. We modify conventional adders either to reduce the area or to increase the speed or for power dissipation factors. The approximate adders are classified into two categories that is error weight and error probability. In error weight we use hybrid structures where exact most significant bit and estimated last significant bit are considered. Errors are appeared in the most significant part. Mostly used method is error weight because of its advantages. In error probability the error can be corrected by adding an additional error correction circuit but it add area and power complexities. Generally the flow of adder is from least significant bit to the most significant bit but in the reverse carry propagate adders the carry flow is reverse that is the carry flow is from most significant bit to the first significant bit these makes the carry in stable in the flow.

Table 1: Truth Tables For the some of the adders like Conventional Full Adder, AMA:I TO AMA:IV, AXA:I, Estimated Carry Look Ahead Adder And Hybrid Adder.

Inputs			Conv.FA		AMA-I		AMA-II		AMA-III		AMA-IV		AXA-I		ACLA adder		Hybrid adder	
A	B	Cin	S	Co	S	Co	S	Co	S	Co	S	Co	S	Co	S	Co	S	Co
0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
0	1	0	1	0	0	1	1	0	0	1	0	0	0	1	0	1	1	0
0	1	1	0	1	0	1	0	1	0	1	1	0	1	0	0	1	0	1
1	0	0	1	0	0	0	1	0	1	0	0	1	0	1	1	0	1	0
1	0	1	0	1	0	1	0	1	0	1	0	1	1	0	0	1	0	1
1	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
1	1	1	1	1	1	1	0	1	0	1	1	1	1	1	1	1	1	1

This section shows the review of some of the state-of-the-art approximate full adders made use of in hybrid adders. Consequently, using pass transistor or transmission gate for applying an exact full adder results to the decrease of the energy and time delay. While in case of pass transistors, full voltage swipe in the output will not arrive, therefore lower dc noise margin is observed. As mentioned, equivalent to the work on Estimated Mirror Adder, by shortening the internal construction of the transmission gate based approximate full adders were proposed. Equivalent to the TGAs, estimated full adder called estimated EXNOR-based adders and inaccurate adders based on pass transistors have been proposed, respectively. Hence this work achieved lesser area and power ingesting by reducing the total number of transistors. In this work, the signal Cout is not put back by the static logic, and hence, it is not conceivable to generate a long linked structure of full adders required for producing the carry circulation adders. Now, the case of estimated EXOR adder-I whose truth table is represented in table I is an exception. But, by applying the state logic, the efficiency of the proposed estimated full adder is vanished. In [10], only the usefulness of a only one full adder has been considered without assessing its efficiency in the ripple carry adders.

3. A. REVERSE CARRY LOOK AHEAD ADDER

The conventional full adder that is the convey spread adders main structure square has triple contributions with the similar weight. It also has two yields for a total addition effect with the similar load as the sources of information and a conveyance yield with double the weight. The convey spread postponement (tCP) is one of the most important planning parameters in a full adder because of the way that it decides the deferral of the basic way of multi-bit adders. In the most optimistic example, the postponement of the convey-generating adder is nxtCP assuming that n is the adder's bit width. Consequently, a clock cycle of less than nxtCP may also result in a breach of the time of the contract, followed by a minor error. A little short-defer infringement may lead to a lot of mistake attributable to the way that the blunder happens on the MSBs of the summation. This is the aftereffect of the age and proliferation of the convey contribution of the most significant bits through little critical piece full adders. In view of this thinking,on the off chance that the request for the convey proliferation is switched, one may expect that the measure of mistake because of the planning infringement diminishes. This has propelled us with imagining estimated full adders in which the convey proliferation happens in the invert request (counter-stream bearing).

RCPA 1:

In these reverse carries propagate adder first model the forecast signal is considered as one of the input. Which makes considerable amount of changes in the sum and carry expressions. The implementation these structure in mentor graphics tool in 130-nm technology. The delay and power analysis of these circuit are calculated. The implementation is done using not,and,nand,or,nor gates.

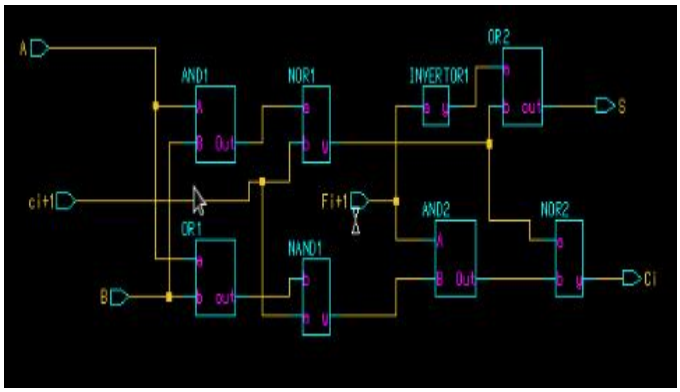

Figure 1: (a) RCPA1

RCPA 2:

In these reverse carries propagate adder second model the forecast signal is considered as AND operation of two input signals. These change in the forecast signal makes abrupt changes in the sum and carry experssions. The circuit is constructed using and ,nor ,invertor and calculated delay and power.

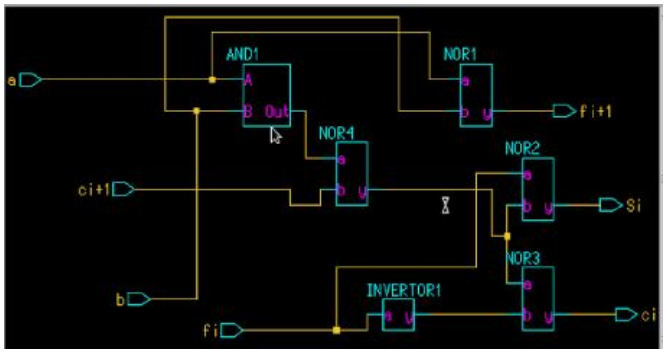

Figure 1: (b) RCPA2

RCPA 3:

In these reverse carry propagate adder third model the forecast signal is considered as OR operation of two input

signals. These change in the forecast signal makes abrupt changes in the sum and carry expressions.

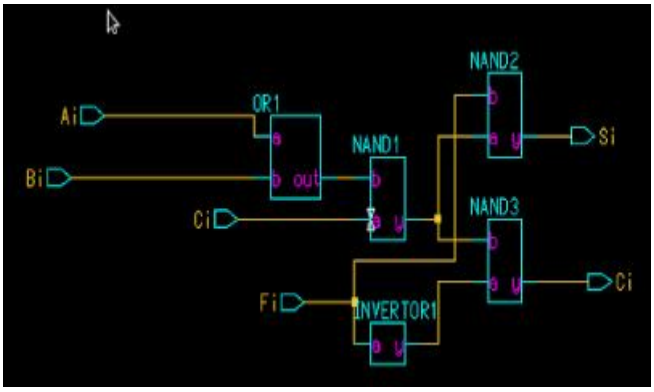

Figure 1: (c) RCPA3

3.B.APPROXIMATE CARRY LOOK AHEAD ADDER:

In carry look ahead adder both generate and propagate terms are considered in the output carry equation but in estimated carry look ahead adder only the propagate term. The generate term is removed to reduce the complexity, delay power consumption and varies parameters. The expression for sum remain constant. The disadvantage of these method is exactness decreases. It is widely used in single processing applications.

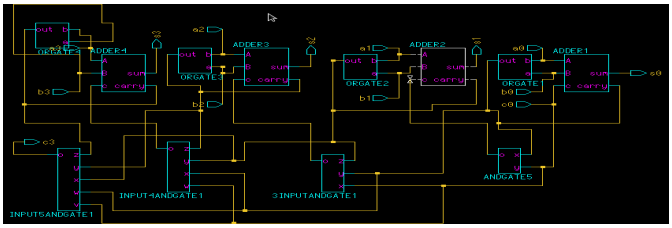

Figure 2: Approximate carry look ahead adder

Cout=P.Cin where p is propagate which is equal to Ai+Bi

3.C.HYBRID ADDER

Hybrid full adder is an circuit with both transmission gate logic and CMOS (complementary metal oxide) logic. By using both this logics in a single circuit can reduce the power and propagation delay. Three modules are considered one for sum other for carry. When compared with normal adders it acquires the advantages of both CMOS and Transmission gate logics.

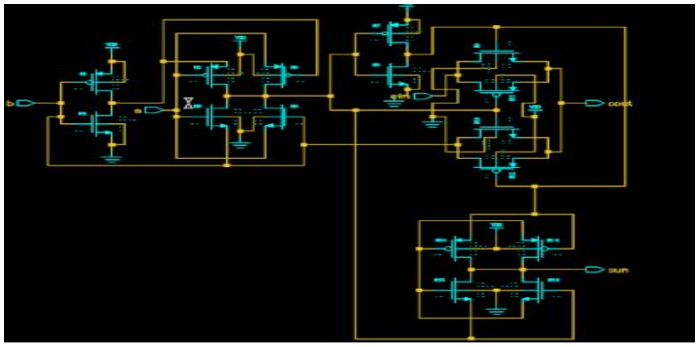

Figure 3: Hybrid Adder

4. SIMULATION COMPARISION

In these sections the comparison of results for Reverse carry propagate adder (3 types), Approximate carry look ahead adder and hybrid adder with the existing adders. These simulations have been done in Mentor graphics tools with 135 nm is compared with the cadence virtuoso tool with 45nm technology at 1V power supply. The maximum delays, power consumption and number of transistors are compared. The user can also measure the accuracy or in exactness of the output.

Table 2: Performance Comparison Of RCPAS,ACLA &Hybrid Adders with proposed and existing adders

	RCPA 1	RCPA 1 (MG)	RCPA 2	RPCA 2 (MG)	RCP A3	RCPA 3(MG)	ACL A	ACL A(M G)	HYBRI D FA	HYB RID FA(M G)
DEALY	50.8ns	50.311 ns	51.4ns	21.153 ns	51.7n s	53.062 3ns	19.8n s	18.9n s	252.3ps	20.9ns
POWER	180.2n w	91.72n w	126.9n w	75.50n w	139.1 nw	53.062 3nw	255.8 uw	558.6 1uw	590.89u w	550.76 1uw

5. CONCLUSION

In these papers the comparison the delay, power of different approximate adder like reverse carry propagate adder, approximate carry look ahead adder and hybrid adder. And observed that the delay of approximate carry look ahead adder is very minute when compared with other adder. The power dissipation is very less of ripple carry adder-2.the delay of hybrid adder is also similar to that of approximate carry look ahead adder. These adders can be used for digital signal processing where the user doesn't require the actual/ exact output.

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