



Optimal Design of CMOS 0.18 μ m Low Noise Amplifier using Multi-Objective Artificial Bee Colony Algorithm

Hamid BOUALI¹, Bachir BENHALA¹, Hamid BOUYGHF²

¹LEAB, Department of physics FS, Meknes, Moulay Ismail University, Morocco, bouali_hamid@hotmail.com

²LEAB, Department of physics FS, Meknes, Moulay Ismail University, Morocco, b.benhala@umi.ac.ma

²LEEA, Department of Electrical Engineering, FST, Mohammedia, Hassan II University, Morocco, hamid.bouyghf@gmail.com

ABSTRACT

This paper presents, an optimal design of the CMOS Low Noise Amplifier (LNA) for Radio Frequency (RF) receivers using the Multi-Objective Artificial Bee Colony (MOABC) Algorithm. The main aim of this work is to find the optimal device sizes of an LNA cascode with inductive source degeneration structure to achieve high voltage gain (A_v) while maintaining low noise figure (NF). The considered LNA operates at 2.4 GHz and implemented in a 0.18 μ m CMOS process with 1.8V power supply. The results of optimization are validated using Advanced Design System (ADS) software and confirm that MOABC technique effectiveness to determine device size and optimize LNA design.

Key words: Multi-Objective, optimization, MOABC, CMOS process, Cascode structure, LNA, Noise figure, Voltage gain.

1. INTRODUCTION

The Analog circuit design optimization problems, of which approximately 75% require much more time and expertise. Therefore, the development of reliable automatic tools in integrated circuit design seems to be a priority highly attractive [1,2,3]. One solution to this problem is employing the meta-heuristics based on the intelligence of animal swarms [4] that are a relatively new techniques for solving NP-hard problems by reducing the number of redesign iterations and computing time needed to optimize the problem parameters. The most used are the Particle Swarm Optimization technique (PSO) [5], Artificial Bee Colony algorithm (ABC) [6,7] and Ant Colony Optimization technique (ACO) [8,9], that imitate the social behavior of birds, bees or ants.

The problems of analog circuits are usually formed by at least two conflicting performance parameters. That means that improving one performance, habitually leads to the degradation of another one [10]. It is therefore essential to deal with these optimization problems using multi-objective techniques. In order to solve the multi-objective analog

circuits problems, several meta heuristics algorithms have been proposed, such as Multi-objective Optimization Particle Swarm Optimization (MOPSO) [11], Ant Colony Optimization (MOACO) [12], etc.

In this work, we propose an application of MOABC algorithm [13] in order to optimize the sizing of an LNA circuit that is the fundamental building block of most receiver's front-end [14]. The main function of this block is to amplify the incoming weak signals from the antenna without adding noise. The most important characteristics of LNA circuit are high voltage gain, low noise figure, and low power consumption. The reason we choose the multi-objective technique for optimization is that LNA circuit have several parameters, which are in conflict with each other and designers must make trade-offs between these objectives such as voltage gain, noise figure and power consumption ... [4] (see Figure 1).

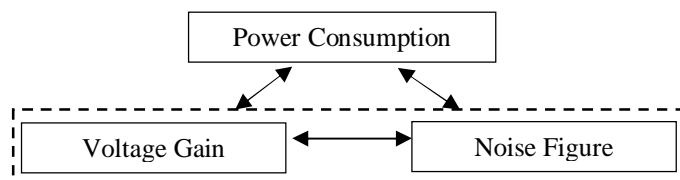


Figure 1: CMOS LNA Design Trade-Offs.

A simplified block diagram of a basic architecture used in many RF receivers is shown in Figure 2.

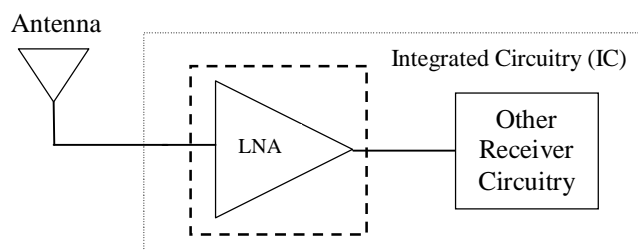


Figure 2: Location of RF-LNA block in receiver architecture

This paper is organized as follows: in Section 2, the concept of multi-objective optimization is described; In Section 3, brief introduction of the proposed MOABC meta heuristic optimization algorithm is presented; Section 4, describes the design methodology of LNA circuit using MOABC algorithm; In Section 5, the results of the LNA design and discussions are provided. Conclusion and future works are given in Section 6.

2. MULTI-OBJECTIVE OPTIMIZATION PROBLEM

The Multi-objective Optimization Problem can be defined as the problem of finding [5][6]:

A vector of decision variables that satisfies constraints and optimizes a vector function whose elements represent several objective functions.

2.1 Formulation of a multi-objective problem

Formally, a multi-objective optimization problem can be defined as follows:

Find the vector $\vec{x}^* = (x^*_1, x^*_2, \dots, x^*_n)$ which satisfies the (m) inequality constraints:

$$g_i(\vec{x}) \geq 0, \quad i = 1, 2, \dots, m. \quad (1)$$

the (p) equality constraints,

$$h_i(\vec{x}) = 0, \quad i = 1, 2, \dots, p. \quad (2)$$

and optimizes the vector function,

$$\vec{f}(\vec{x}) = (\vec{f}_1(\vec{x}), \vec{f}_2(\vec{x}), \dots, \vec{f}_k(\vec{x})) \quad (3)$$

Where,

\vec{x} is a n-dimensional vectorial decision variable. $\vec{f}(\vec{x})$ is a k-dimensional objective vector.

2.2 Notion of pareto optimum

The existence of more than one optimum (or trade-off) solution in multi-objective optimization problems makes necessary a different notion of Pareto optimum [5][6]:

- Pareto Dominance : A vector $\vec{u} = (u_1, u_2, \dots, u_k)$ is said to dominate $\vec{v} = (v_1, v_2, \dots, v_k)$ (denoted by $\vec{u} \leq \vec{v}$) if and only if u is partially less than v, i.e., $\forall i \in \{1 \dots k\} u_i \leq v_i \cap \exists i \in \{1 \dots k\} u_i < v_i$.
- Pareto Optimal Set: For a given MOP $\vec{f}(\vec{x})$, the Pareto optimal set P^* is defined as:

$$P^* : \{x \in \Omega / \exists x' \in \Omega \vec{f}(x') \leq \vec{f}(x)\}$$

- Pareto Front: For a given MOP $\vec{f}(x)$, and Pareto optimal set P^* the Pareto Front PF^* is defined as: $PF^* : \{\vec{u} = \vec{f} = (f_1(x), f_2(x), \dots, f_k(x)) / x \in P^*\}$.

3. MULTI-OBJECTIVE ARTIFICIAL BEE COLONY ALGORITHM (MOABC) PROPOSED

The Multi-Objective Artificial Bee Colony (MOABC) is one of the most recent meta-heuristic algorithms. This is a new

population based approach that has shown good performance in dealing with different types of optimization problems [7].

In this MOABC algorithm, A food source position represents a possible solution to the problem to be optimized. The quantity of nectar of a food source corresponds to the quality of the solution represented by that food source. The colony of artificial bees is classified into three types with certain responsibilities[7]:

Employed bees, Onlooker bees and Scout bees.

The algorithm structure of the MOABC optimization proposed is given as follows:

- Initialization stage:

In initialization stage, the scout bees initialize a set of (NCS) food sources position randomly and the external archive (AR) will be initialized. NCS is equal to the number of colony size of the employed and on looker's bee. Each member of the population represents a solution to the problem, noted by $food_i (i=1 \dots NCS)$.

- Employed bees' stage:

In the employed bee's stage, for each employed bee finds a new food source position (sol_i^*) in the neighborhood of its current food source position ($food_i$). The new food source is generated by the following expression:

$$sol_i^* = food_i^j + rand[-1; 1] * (food_i^j - food_k^j) \quad (4)$$

Where,

$$i \neq k; i \in (1, 2, \dots, N)$$

N is the number of employed bees

j, k is selected randomly.

$food_k^j$ is neighbor bee off $food_i^j$.

Each of employed bee compares the current food source position with a neighbor food source position and chooses out the better one using a greedy selection technique. The selected non-dominated solutions are stored in an external archive (AR).

- Onlooker bees' stage:

In the onlooker bees stage, for each bee ($food_i$), it randomly selected and learn from an external archive (AR) produced by employed bee stage, The new food source (sol_i^*) is generated by the following expression:

$$sol_i^{rp*} = food_i^{rp} + rand[-1; 1] * (AR_k^{rp} - food_i^{rp}) \quad (5)$$

Where,

$i \in (1, 2, \dots, Foodnumber) / Foodnumber$ is equal to half of the number of colony size (NCS).

$k \in (1, 2, \dots, m)$ is randomly selected. m is the size of the external archive (AR). rp is randomly selected from (AR).

After producing the new solution (sol_i^{rp*}), the greedy selection is applied to decide which solution enters in the external archive (AR).

- Scout bees' stage

In the scout bees' stage, the scout bee is responsible for finding a new food source position and evaluate the quality of their nectar. when the scout bee finds the food source , she converts to the employed bee .In this step, if the food source isn't improved by the trail number (trail number for a release food source is higher than a control parameter 'Limit'), then that food source is exhausted by its employed bee and this one becomes a scout bee .

3.1 Flowchart of the proposed MOABC algorithm

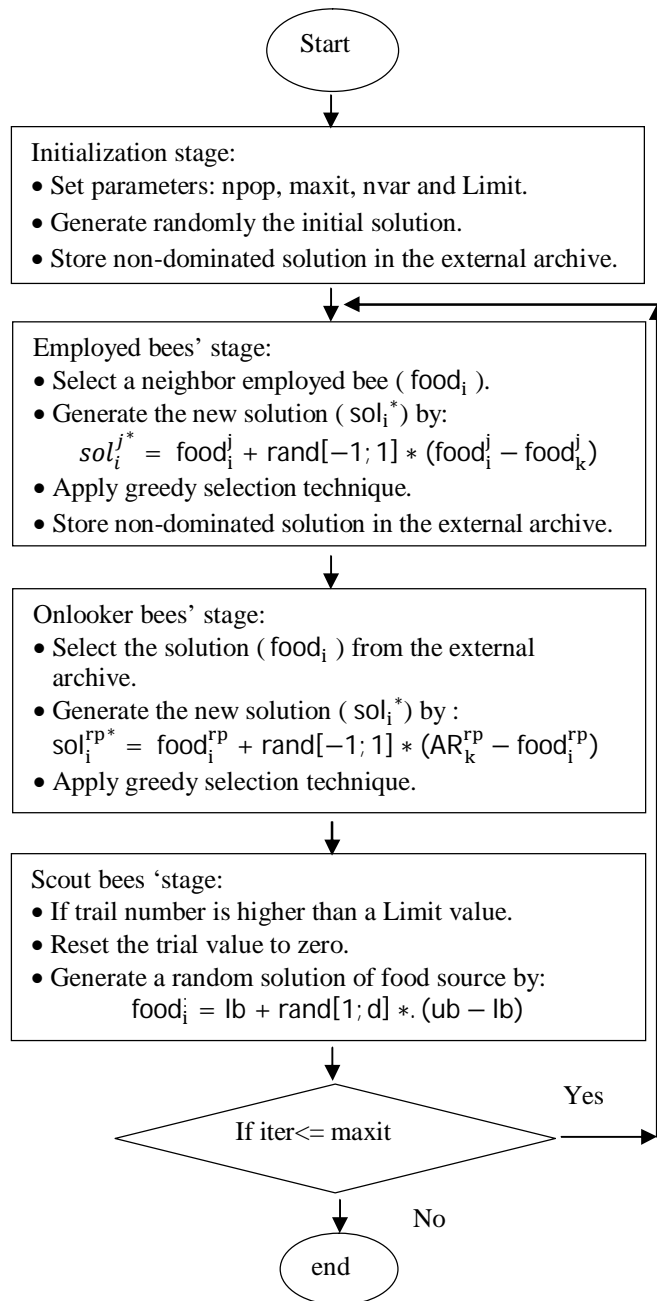


Figure 3:Flowchart of the proposed MOABC algorithm.

4. DESIGN METHODOLOGY OF RF-LNA USING MOABC ALGORITHM.

4.1 RF-LNA optimization

The most widely RF-LNA topology used is cascode structure with source inductive degeneration, because it can satisfy requirements for both noise and Gain simultaneously (see Figure 4) [8] [9].

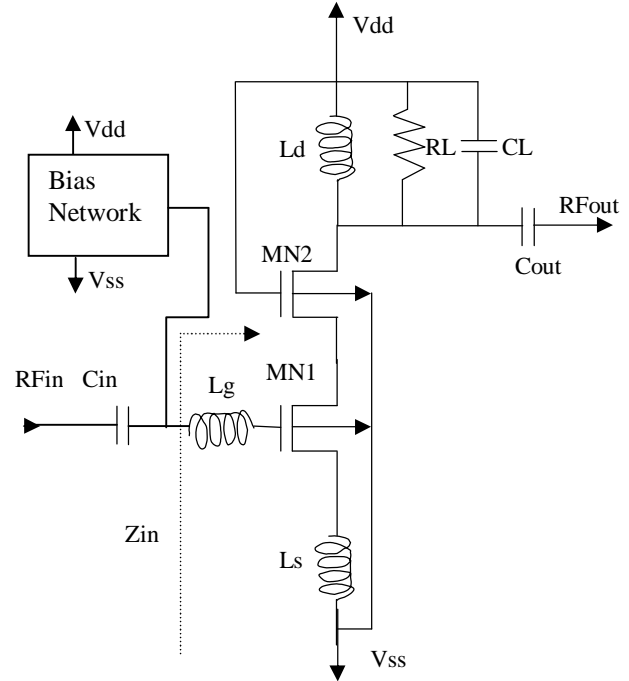


Figure 4:LNA Cascode with inductive source degeneration.

The input impedance (Z_{in}) of this structure is given by the first stage, (see Figure 4):

$$Z_{IN} = j\omega(L_g + L_s) + \left(1/j\omega C_{gs}\right) + \left(g_m/C_{gs}\right)L_s \quad (6)$$

The input matching criteria formed by L_g and L_s are estimated by ignoring Miller effect of C_{gd1} of transistor NM1 and effective gate resistance R_g :

$$L_s = R_s C_{gs} / g_m \quad (7)$$

$$L_g = \left(1/\omega_0^2 C_{gs}\right) - L_s \quad (8)$$

Where,

L_s and L_g are the gate input inductor and source degeneration inductor respectively.

R_s is the source resistance ($\sim 50\Omega$).

ω_0 is the operating frequency.

g_m and C_{gs} are the transconductance and gate-source capacitance of nmos transistor (NM1) respectively.

The voltage gain (A_v) is equal to the product of the circuit's transconductance G_m and the load resistance R_L figure 4:

$$A_v = V_{out}/V_{in} = G_m * R_L = R_L/2L_s\omega_0 \quad (9)$$

The noise figure (NF) of the cascode CS stage can be formulated as a function of width (W), drain current (Id)[10][11][12].

$$NF = 1 + (A + B + C + D)/E(10)$$

Where,

$$A = (1/4) * \gamma * g_{d0}(11)$$

$$B = g_m^2 * \left(\frac{C_{gs}}{C_{tot}} \right)^2 * (Q^2 + 1/4) * \beta / (5 * g_{d0})(12)$$

$$C = g_m * c * \left(\frac{C_{gs}}{C_{tot}} \right) * \sqrt{(\gamma * \beta) / 20}(13)$$

$$D = 1/R_L(14)$$

$$E = g_m^2 * R_s * Q^2(15)$$

Where,

- γ is the white noise factor, approximately equal to 1.05 for 180nm technology.
- β is gate noise parameter, approximately equal to 3.8.
- c is correlation coefficient,
- C_{gs} is intrinsic gate capacitance,
- C_{tot} is sum of C_{gs} , C_d and parasitic capacitance.
- Q is input quality factor of the circuit.

The Approximated expressions of g_m and g_{d0} can be expressed as follows [12]:

$$g_m = A_0 * L^{A_1} * W^{A_2} * I_d^{A_3}(16)$$

$$g_{d0} = B_0 * L^{B_1} * W^{B_2} * I_d^{B_3}(17)$$

Where, L , W and I_d refer to length and width of MOS transistors, and drain current respectively

The values of constants are shown in table 1.

Table 1: Value of constants for calculating g_m and g_{d0}

A_0	A_1	A_2	A_3
0.0463	-0.4489	0.5311	0.4689

B_0	B_1	B_2	B_3
0.0096	-0.5595	0.5194	0.4806

4.2 RF-LNA design methodology using MOABC algorithm

The optimization problem is solved by an iterative loop between an optimization algorithm (mono-objective or multi-objective) and a performance evaluator (analytical equations or simulators) [14]. At each iteration, the optimization algorithm produces new sets of design variables: transistor

size (width and length), resistance, capacitor and inductor value, ..., (see Figure 5).

In this paper, a MOABC optimization algorithm is used to optimize two objective functions of RF-LNA circuit, voltage gain and noise figure [15][16]. In order to achieve a good trade-off, have to:

- Maximize the voltage gain,
- Minimize the noise figure.

With respect to the constraints design and target specifications [16], as presented in Table 2

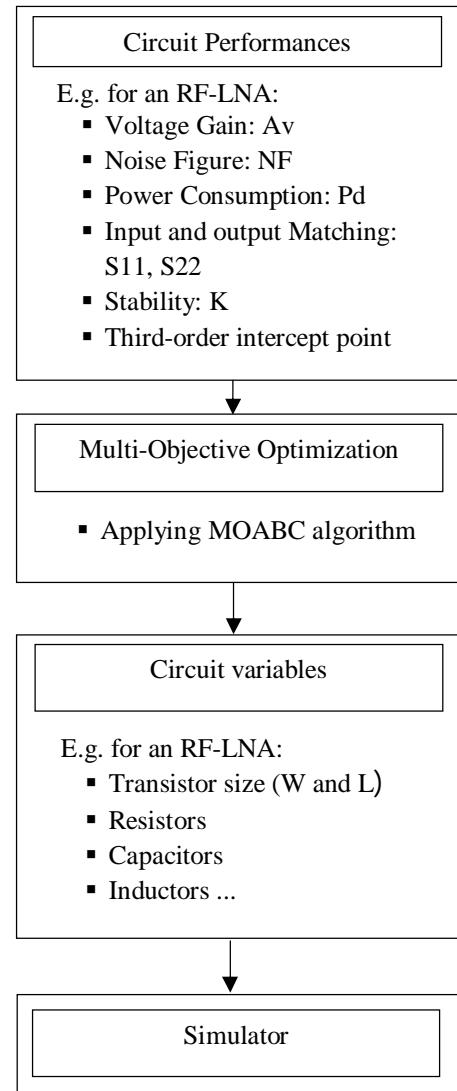


Figure 5:Flowchart of RF-LNA design methodology

Table 2: CMOS LNA Specifications

Parameters	Specification
Process	0.18 μ m CMOS
Power supply Vdd	1.8V
Operating Frequency (F)	2.4GHz
Voltage Gain (Av)	≥ 15 dB
Noise Figure (NF)	< 3 dB
Noise Figure min (NFmin)	< 2.5 dB
Power dissipation	≤ 11 mW
S11	< -10 dB
S22	< -10 dB
IIP3	> -10 dBm
Stability factor (K)	> 1

Table 3 shows the MOABC algorithm setting parameters.

Table 3: Parameters adopted for the MOABC algorithm

MOABC settings	Value
Max Iteration (MaxIt)	100
Dimension of the solution space(D)	2
Limit (=Number of onlooker's bees*D)	100
Size of the external archive (AR)	50
Number of colony size (NCS)	100
Number of employed bees (50 % of NCS)	50%
Number of onlooker's bees (50 % of NCS)	50%
Number of scouts	1

5. SIMULATION RESULTS AND DISCUSSIONS

5.1 Simulation results using MOABC/Matlab

The parameters values for MOABC algorithm used for this optimization problem are shown in Table 3.

The MOABC algorithm was applied to generate the Pareto front, illustrated in Figure 6.

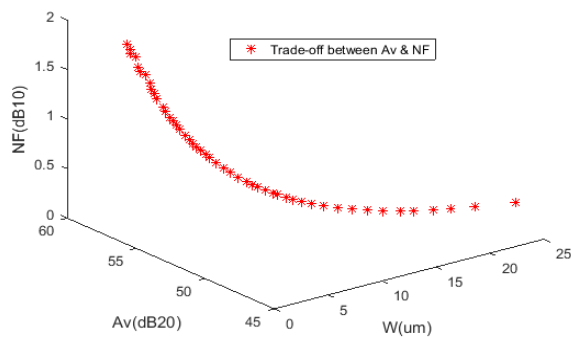


Figure 6: Optimal Pareto front obtained by MOABC

The optimal sizing of 4 solutions chosen from the archive (AR) are shown in Table 4.

Table 4: Parameters values of 4 optimal solutions

Parameters	Solution ^o			
	@1	@2	@3	@4
W(μ m)	23.3	20.3	18.5	15.8
L(μ m)	0.18	0.18	0.18	0.18
Ls(pH)	132.3	121.08	115.92	107.66
Lg(nH)	183.39	210.53	231.03	270.54
Ld(nH)	10	10	10	10
CL (fF)	439.76	439.76	439.76	439.76
RL(Ω)	753.98	753.98	753.98	753.98
Cin(pF)	10	10	10	10
Cout(pF)	10	10	10	10
Qin	4	4	4	4
Qout	5	5	5	5
Id(mA)	2	2	2	2
Vdd(V)	1.8	1.8	1.8	1.8
F(GHz)	2.4	2.4	2.4	2.4

5.2 Simulation results using ADS

The initial startup values given after executing the MOABC algorithm has been used for the design of RF-LNA based on 0.18 μ m CMOS process. The design is finally simulated with ADS (Advanced Design System) software. And its simulation results of Av and NF for 4 solutions are presented in Table 5.

Table 5: Simulations results of Av and NF

Performance		Solution ^o				Spec
		@1	@2	@3	@4	
ADS Results	Av	20.96	18.59	17.76	15.86	≥ 15 dB
	NF	2.25	2.47	2.52	2.62	< 3 dB

Figures 7,8,9,10 and 11 show the simulation results of the voltage Gain, the noise figure, input-output matching (S11,S22) and stability factor (K) based on the best optimal solution(@1) obtained by MOABC algorithm.

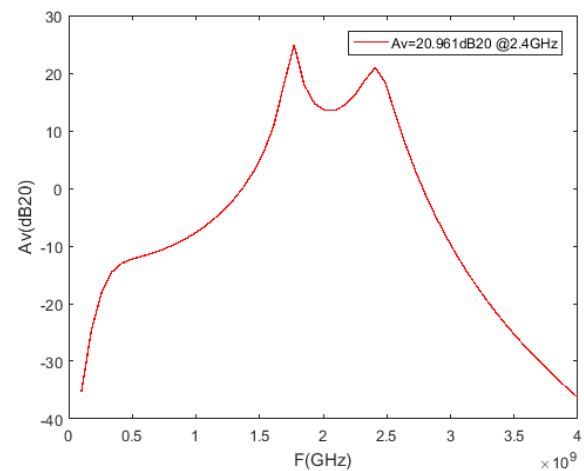


Figure 7: Voltage gain vs. frequency of @1

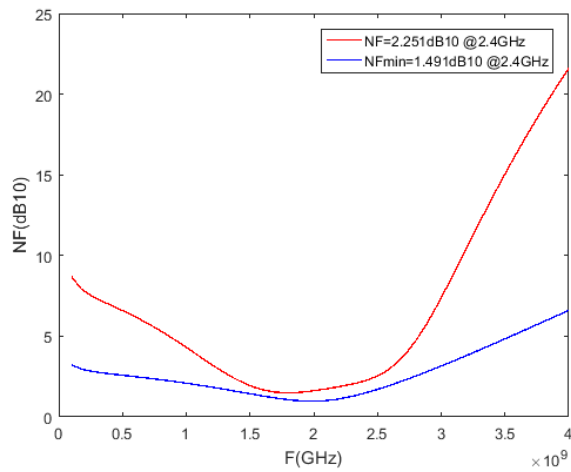


Figure 8: Noise figure vs. Frequency of @1

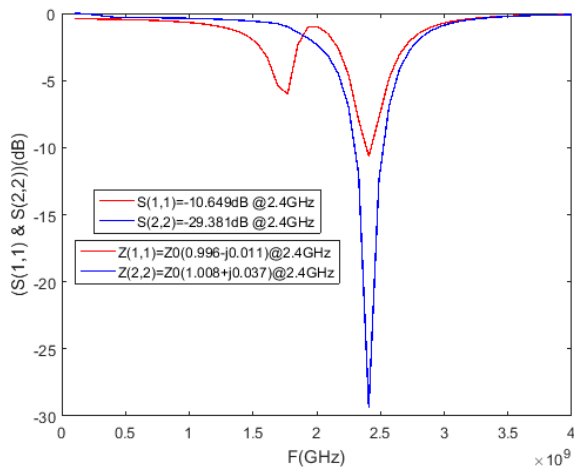


Figure 9: S11 and S22 vs. frequency of @1

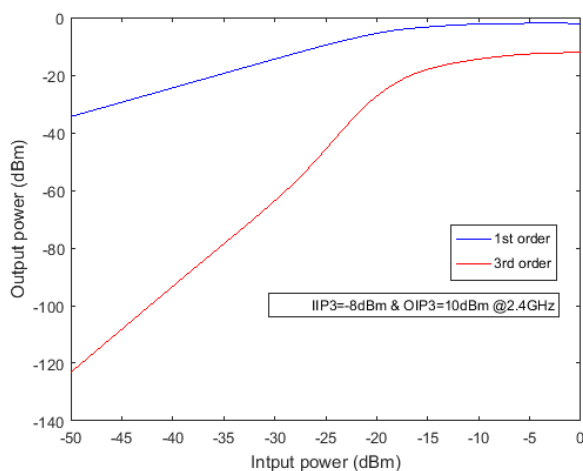


Figure 10: IIP3 of @1

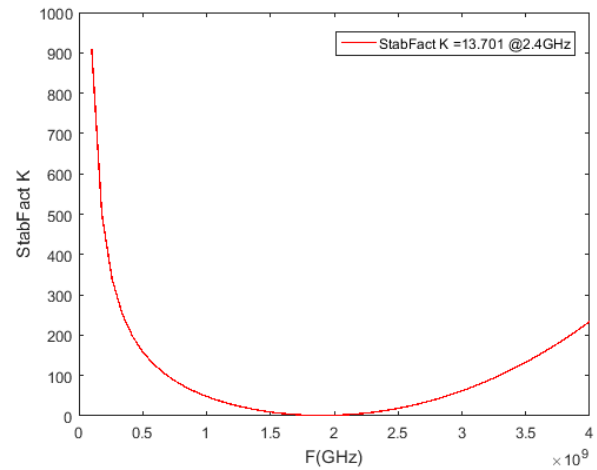


Figure 11: Stability factor (K) vs. frequency of @1

From figures 7,8,9,10 and 11 and Table 4, we notice that simulation results are in good agreement with the target specifications:

- Good matching at both poles,
 - $Z_{in} = Z_0(0.996-j0.011) \sim 50\Omega$
 - $Z_{out} = Z_0(1.008+j0.037) \sim 50\Omega$
- High voltage gain,
 - $A_v = 20.96\text{dB} = A_{v_Spec}$
- Acceptable noise figure,
 - $NF = 2.25 < NF_Spec$
 - $NF_{min} = 1.491 < NF_{min_Spec}$
- Low power dissipation,
 - $P_d = 3.9\text{mW} < P_d_Spec$
- Third-order intercept point IIP3
 - $IIP3 > IIP3_spec$
- Stability
 - $K = 13.701 > K_Spec$

6. CONCLUSION

In this paper, we have presented an application of the ABC algorithm for with the use in the multi objective optimization problems resolution. It has been considered to optimize two trade-offs RF-LNA performances, the voltage gain (A_v) and the noise figure (NF) simultaneously. The viability of the proposed MOABC algorithm was shown through the generation of the Pareto front (NF vs. A_v). The obtained results demonstrate the utility and reliability of the automatic design methodology. In addition, ADS simulations were highlighted. Now we are focusing on the application of the MOABC technique in more popular and complex integrated circuits.

REFERENCES

1. J. Rogers and C.Plett, **Radio Frequency Integrated Circuit Design**, 2003, Artech House classic.

2. C. Bowick, C. Ajluni, J. Blyler., **RF Circuit Design**, 2d ed. 2007.
3. N. Mohankumar, Girish Shankar Mishra, M. Arun Kumar and R. Poornachandran. **Performance of Gate Engineered Symmetric Double Gate MOS Devices and circuits for ultra-low power Analog and RF applications**, International Journal of Advanced Trends in Computer Science and Engineering, Vol 9, N°2, pp. 1239 – 1246, 2020.
4. B. Benhala, P. Pereira, A. Sallem, (Editors), **Focus on swarm intelligence research and applications**, NOVA Science Publishers, 2017.
5. M. Fakhfakh, Y. Cooren, A. Sallem, M. Loulou and P. Siarry. **Analog Circuit Design Optimization through the Particle Swarm Optimization Technique**, Analog Integrated Circuits and Signal Processing, Vol. 63, No 1, pp. 71-82, 2010.
6. S. Abi, H. Bouyghf, A. Raihani, and B. Benhala. **Swarm Intelligence Optimization Techniques for an Optimal RF Integrated Spiral Inductor Design**, International Conference on Electronics, Control, Optimization and Computer Science (ICECOCS), Kenitra, pp. 1-7, 2018.
7. B. Benhala. **Artificial bee colony technique for optimal design of folded cascode OTA**, 2018 International Conference on Applied Mathematics and Computer Science, ICAMCS 2018, Paris, pp. 59-64
8. B. Benhala, **Sizing of an inverted current conveyors by an enhanced ant colony optimization technique**, 2016 Conference on Design of Circuits and Integrated Systems (DCIS), Granada, 2016, pp. 1–5.
9. L. Kritele, B. Benhala, and I. Zorkani. **Ant Colony Optimization for Optimal Analog Filter Sizing**, Chapter 10, Book: Focus on swarm intelligence research and applications, Eds., B. Benhala, P. Pereira and A. Sallem, NOVA Science Publishers, pp. 193–220, 2017.
10. Mohammad AizatBasir, Mohamed Saifullah Hussin, YuhanisYusof. **Optimization of Multi-objective ENORA and NSGA-II based on Bio-Inspired Algorithms for Classification Problem**, International Journal of Advanced Trends in Computer Science and Engineering, Vol 9, N° 1.3, pp. 110 - 116
11. MounaKotti; Amin Sallem; Mariam Bougharriou; Mourad Fakhfakh ; Mourad Loulou .**Optimizing CMOS LNA circuits through multi-objective meta heuristics**, 2010 XIth International Workshop on Symbolic and Numerical Methods, Modeling and Applications to Circuit Design (SM2ACD), Gammath, Tunisia.
12. BachirBenhala, Ali Ahaitouf, Abdellah Mechaqrane. **Multiobjective Optimization of An Operational Amplifier by the Ant Colony OptimisationAlgorithm**, Scientific & Academic Publishing, Electrical and Electronic Engineering journal, Vol. 2, N° 4, August 2012, Pages 230-235.
13. H. Bouali, B. Benhala, and H. Bouyghf. **Performance study of Multi-Objective Artificial Bee Colony (MOABC) Algorithm by Numerical Problems Benchmark**, 1st International Conference on Innovative Research in Applied Science, Engineering and Technology (IRASET), Meknes, Morocco, pp. 1-6, 2020.
14. B. Prameela and A. E. Daniel, **Design of Low Noise Amplifier for IEEE Standard 802.11b Using Cascode and Modified Cascode Techniques**, Procedia Technol, vol. 25, pp. 443–449, Jan. 2016.
15. N. S. Shahraki, A. Mohammadi, S. MohammadiEsfahrood, and S. H. Zahiri, **Improving the Performance of Analog Integrated Circuits using Multi-Objective Metaheuristic Algorithms**, in 2019 5th Conference on Knowledge Based Engineering and Innovation (KBEI), Tehran, Iran, pp. 822–826, Feb. 2019.
16. C. A. Coello and M. S. Lechuga, **MOPSO: a proposal for multiple objective particle swarm optimization**, in Proceedings of the 2002 Congress on Evolutionary Computation. CEC'02, Honolulu, HI, USA, vol. 2, pp. 1051–1056, 2002.
17. K. Deb, **Multi-Objective Optimization Using Evolutionary Algorithms**, Edition 1, Wiley Publishing, 2001.
18. D.K. Shaeffer, Derek, Lee, H. Thomas, **The design and implementation of low-power CMOS radio receivers**, Kluwer academic, 2002.
19. X. Li, M. Ismail, **Multi-Standard CMOS Wireless Receivers: Analysis and Design**, Kluwer academic, 2002.
20. H. David K. Hoe and Xiaoyu Jin, **The Design of Low Noise Amplifiers in Deep Submicron CMOS Process: A convex Optimization Approach**. Hindawi Publishing Corporation VLSI Design, ID 312639, 2015.
21. D. Joshi and *al.*, **Optimization of 2.4 GHz CMOS Low Noise Amplifier Using Hybrid Particle Swarm Optimization with Lévy Flight**, 30th International Conference on VLSI Design and 16th International Conference on Embedded Systems (VLSID), Hyderabad, doi: 10.1109, pp. 181-186 2017.
22. H. Bouyghf, B. Benhala and A. Raihani, **Optimal design of RF CMOS circuits by means of an artificial bee colony technique**, Chapter 11, Book: Focus on swarm intelligence research and applications, Eds., B. Benhala, P. Pereira and A. Sallem, NOVA Science Publishers, pp. 221–246, 2017.
23. S. Boyd and *al.*, **A tutorial on geometric programming**, 'Optimization and Engineering', vol. 8, no. 1, pp. 67–127, 2007
24. R. Gonzalez-Echevarria *et al.*, **An Automated Design Methodology of RF Circuits by Using Pareto-Optimal Fronts of EM-Simulated Inductors**, IEEE Trans. Comput. -Aided Des. Integr. Circuits Syst., vol. 36, no. 1, pp. 15–26, Jan. 2017.
25. A. Sallem, B. Benhala, M. Kotti, M. Fakhfakh, A. Ahaitouf, and M. Loulou, **Application of swarm intelligence techniques to the design of analog circuits: evaluation and comparison**, Analog Integr Circuits Signal Process., vol. 75, no. 3, pp. 499–516; Jun. 2013.
26. V. Bhale, **Design and Optimization of CMOS 0.18µm Low Noise Amplifier for Wireless Applications**, Int. J. Inf. Electron. Eng., vol. 4, no. 2, 2014.