



FPGA Seven-Segment-Display by Using Altera DE2-115 Board with Practice and Implementation

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ABSTRACT

This paper presents a simple implementation of Seven-Segment Displays in very simple way by using "Altera DE2-115 Board" to understand the idea for those students who are not in the field of Electrical and computer science field. Seven-Segment Displays are used to display input data on FPGA Device. The main focused of this paper is to implement and practice Seven-Segment Displays by using Verilog file in which we must write code in C++ and execution simulations on innumerable counter designs and implement designs on FPGA device utilizing Seven-Segment Displays and Switches. The control consumption and the delay of unit is predictable using the synthesizer "Quartus Prime" and get simulation result by using "ModelSim".

Key Words: Quartus Prime Software, ModelSim, Seven Segment Display, Altera DE2-115 Board.

1. INTRODUCTION

Altera DE2 series boards have constantly been used for educational development. Features of Altera DE2-70 device responding to increased adaptable low-cost spectrum needs driven by the demand for mobile video, voice, data access, and the hunger for high-quality images but the new technology "Altera DE2-115" Cyclone ® IV series boards offer an optimal balance of low cost, low power consumption and a rich source of logical function, memory storage and DSP capabilities as compared to Altera DE2-70 series board.

Field Programmable Gate Array (FPGA) device that's mostly used for educational development in the field of electrical and computer science. In this paper Seven-Segment Displays is used to display Decimal Number by using HEX [1] and HEX [0] the values is set by using switches SW [7-4] and SW [3-0]. The values are symbolized by SW [7-4] and SW [3-0] to be displayed on HEX [1] and HEX [0], respectively. Circuit will be able to display the Decimal digits from (0 to 9). Each Verilog file description covers two blocks. These are input/output and architectural components. The input/output description specifies the input and output connections will be displayed on hardware "Altera DE2-115 Series Board".

2. SEVEN SEGMENT DISPLAYS

To display implementation Seven-Segment Displays is the superlative approach. To perform any kind of implementation on Seven-Segment Displays unit requires very less wire, low-cost and simply available in the market [2]. In this paper component the Seven-Segment Displays unit is performed using the FPGA device which efficiently utilizes low-power for the implementation with lowest latency [1]. The Seven-Segment Displays unit name define as A, B, C, D, E, F and G as exposed in Figure.1. In this paper we will study how parallel combinations of "1" and "0" can display hexadecimal numbers. In this implementation Hexadecimal numbers from (0 to 9) are display by using Seven-Segment Displays. Each segment is controlled by a single bit and combinations of segments turned ON or OFF can display all the numbers from (0 to 9) and a few characters, such A, B, C, D, E, F and G as shown in Figure.1.

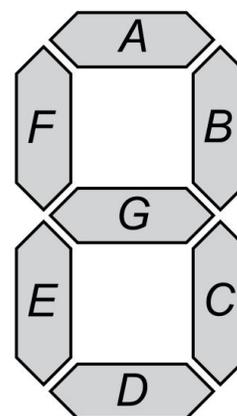


Figure 1: Seven-Segment Displays Unit.

2. BLOCK DIAGRAM OF ALTERA DE2-115 CYCLONE IV

In this diagram we specify the functionality of Alter DE2-115 board to provide maximum flexibility for the user and details about all connections are made through the Cyclone IV "Alter DE2-115 series board" FPGA device as shown in Figure 2 [3].

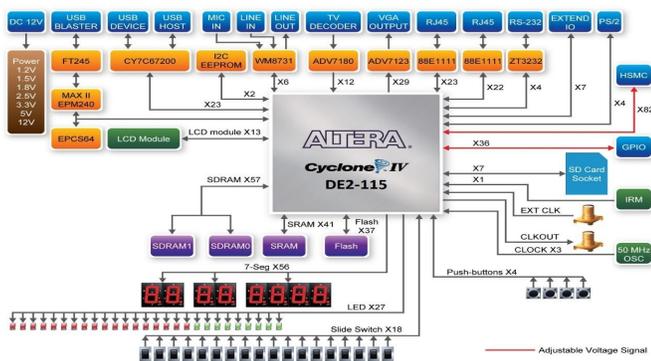


Figure 2: Block Diagram.

2.1 Board Altera DE-115

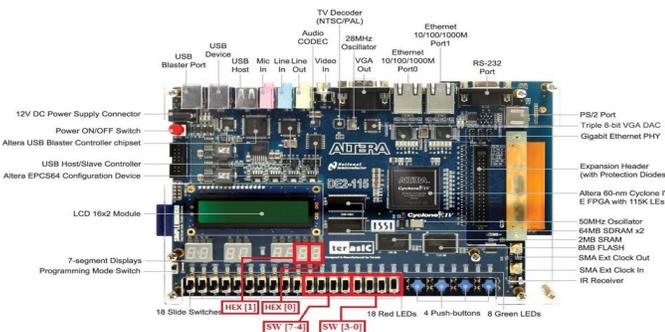


Figure 3: FPGA Device Diagram.

The focus of this paper is to study to get output on FPGA devices by using switches SW [3-0] and SW [7-4] to as input and HEX [0], HEX [1] (LCD) used as output by flashing Verilog file on Altera DE2-115 board as shown in figure 3.

Equipment Required:

1. Altera Quartus Prime software.
2. ModelSim
3. Altera DE2-115 board Development kit with 7.5-V DC power supply and USB cable.
4. USB Blaster Driver.

3. IMPLEMENTATION PROCESS STEP BY STEP

In this exercise we will use two Seven-Segment Display HEX [1] and HEX [0] as output and Eight switches SW [7-4] and SW [3-0] as input. We will display decimal numbers from (0 to 9) on Altera DE2-115 Board by using Seven-Segment Display as output as shown in Figure.3.

Open Quartus Prime Software Create a new project wizard as show in figure.4. The intent of this exercise is to write code in Verilog file to originate the logical functions are required for Seven-Segment Display. These Verilog files we will used to implementation on Altera DE2-115 board.

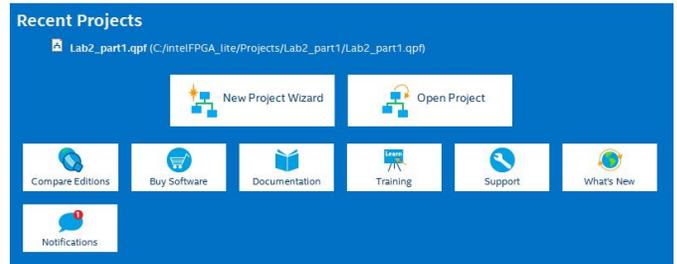


Figure 4: Creation of new project

Then click on “Next” button, after this we will be on this page. click on option “1” for the selection of directory of your project where you want to save your project then click on “Next” button as shown in Figure.6.

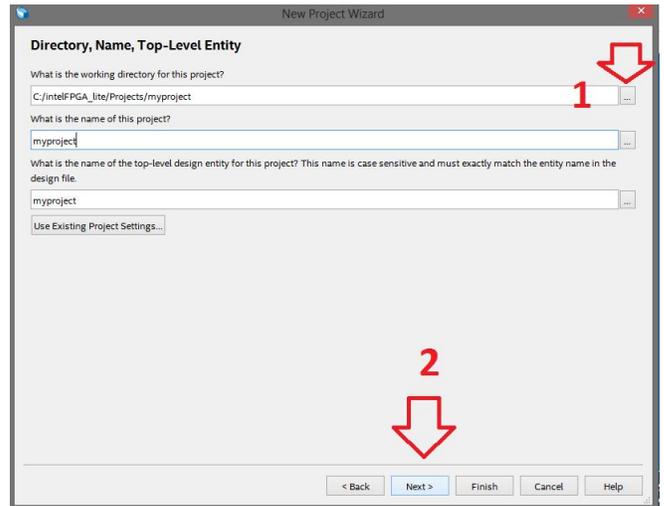


Figure 6: Selection of Computer Directory

In the next option we have to Select the cyclone family “Cyclone IV” and Device chip Number “EP4CE115F29C7” of your Altera DE2-115 Board as shown in Figure.7.

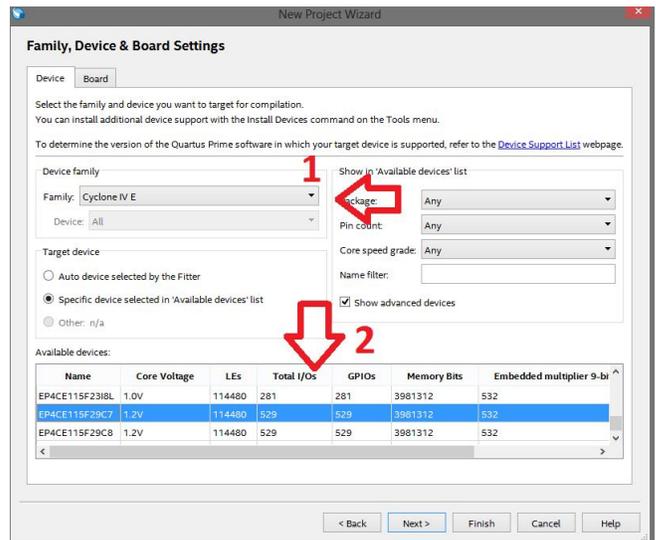


Figure 7: Select the cyclone family “Cyclone IV”

Open “File” option and create a new “Verilog File” as shown in Figure.8.

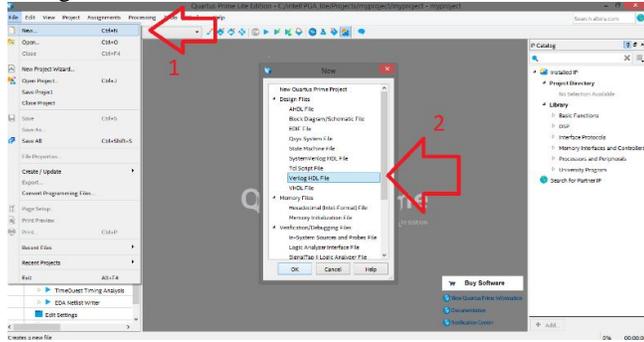


Figure: 8 create a new “Verilog File”

Create Verilog file with the name of “hexdigit” as shown in Figure 8 or any other name to write a code manually in C++ for derive the logic functions required for the Seven-Segment Display from (0 - 9) and specify each logic function as a Boolean expression as shown in Figure.9.

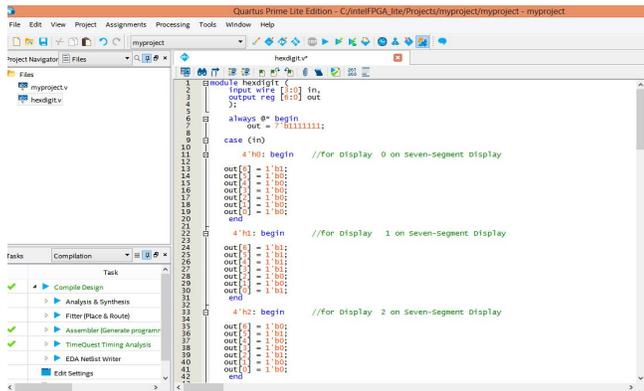


Figure: 9 Verilog file code in c++

Now Create another Verilog file with the name of “myproject” or any other name to write main function to call Verilog file “hexdigit” as show in Figure 9 to display (0 - 9) decimal on HEX [1] and HEX [0] by using Switches SW [7-4] and SW [3-0] as input as shown in Figure.10.

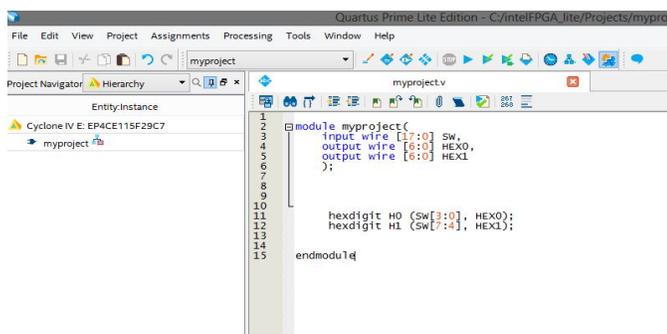


Figure: 10

At the end clicks on “Start Compile” button from the upper menu bar as shown in Figure.11.

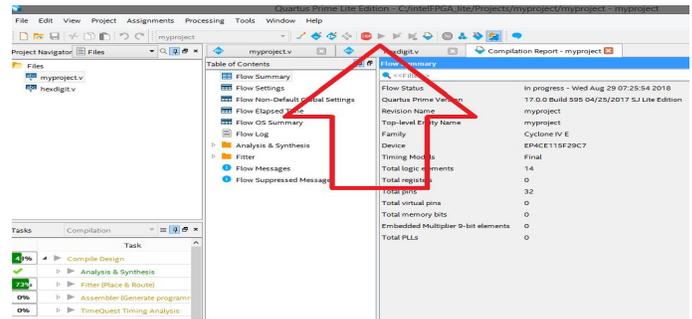


Figure 11: clicks on “Start Compile” button

When Compilation process finished open the “Modelsim” Software and create a new project imports both files that we already compiled “hexdigit” and “myproject” as shown in Figure.12.

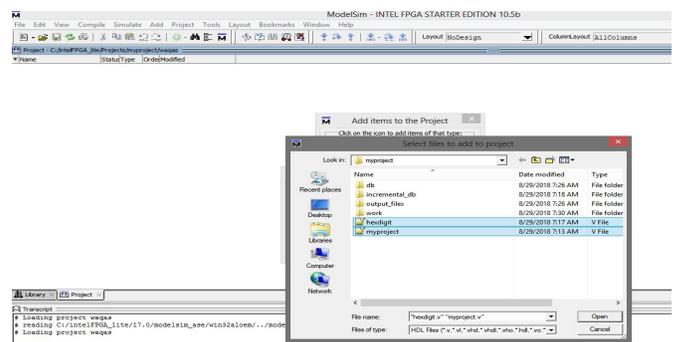


Figure: 12 Import the files “hexdigit” and “myproject”

Now press the button to Start Simulation from the upper menu bar. Now enter input, in my case I have entered “0010” for the switches SW [3-0] and “0110” for the switches SW [7-4] as shown in Figure.13 and Table1 Truth Table of Binary to Hexadecimal Conversion.

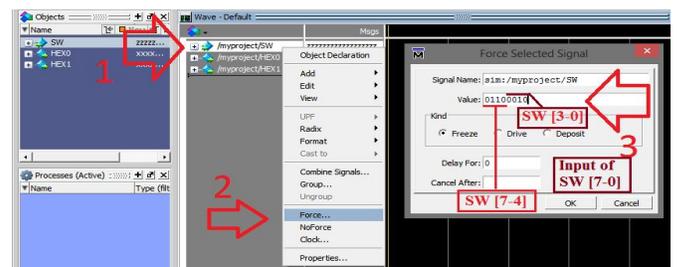


Figure: 13 Input for the switches SW [3-0] and SW [7-4]

Press the “Run” button from the upper menu bar and you will see the output of SW [3-0], SW [7-4] on HEX [0] and HEX [1] as shown in Figure.14.

4. DISCUSSION AND RESULTS

The purpose of this paper to learn how to use switches as input and get output by using HEX [0] and HEX [1] LCDs on Altera DE2-115 Board FPGA Devices. The Figure 14 has shown the

output of Hex [0] and Hex [1]. The simulation result shows the output for the Seven-Segments Display unit which have been generated by using “Modelsim” tool.

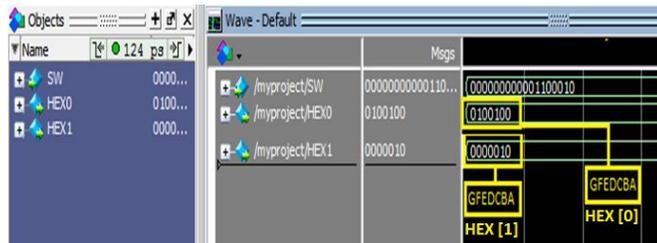


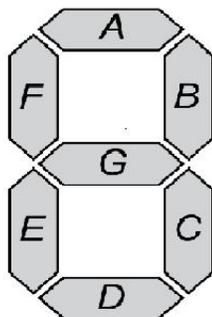
Figure 14: Simulation result by using Modelsim of seven segments display.

In Figure.13and Figure.14 shows that its take 4-bit input by using switches SW [7-4] and SW [3-0] for Seven-Segments Display unit and the outputs are given as A, B, C, D, E, F and G which have been selected the segments matching to the input data in the form of the Boolean expression. The Seven-Segment Displays unit and their output corresponding segment are represented in their Boolean expression as shown in the Truth Tabel.1. [4]. The information in the truth table have been provided “ON means 0” and “OFF means 1”. Truth Tabel 1 below shows the numbers used in hexadecimal and their equivalent in binary to decimal conversion.

Truth Table of Binary to Hexadecimal Conversion

Table: 1 Truth Table of BCD input to Seven Segment

| Digit | Display | Input | A | B | C | D | E | F | G |
|-------|---------|-------|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0000 | on | on | on | on | on | on | off |
| 1 | 1 | 0001 | off | on | on | off | off | off | off |
| 2 | 2 | 0010 | on | on | off | on | on | off | on |
| 3 | 3 | 0011 | on | on | on | on | off | off | on |
| 4 | 4 | 0100 | off | on | on | off | off | on | on |
| 5 | 5 | 0101 | on | on | on | on | off | on | on |
| 6 | 6 | 0110 | on | off | on | on | on | on | on |
| 7 | 7 | 0111 | on | on | on | off | off | off | off |
| 8 | 8 | 0111 | on |
| 9 | 9 | 1001 | on | on | on | on | off | on | on |



Output on LCD of Altera DE2-115

We have used switches SW [7-4] and SW [3-0] as inputs for the implementation of circuit on “Altera DE2-115 board” and used HEX [0] and HEX [1] LCD for the Seven-Segments Display as output as show in Figure.15.

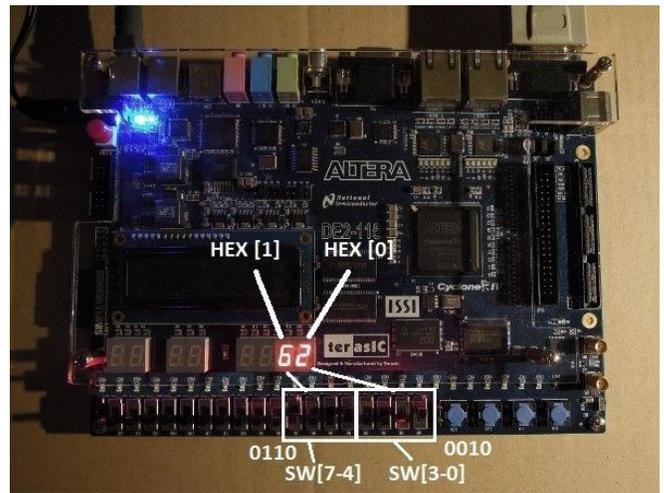


Figure.15. Output of Binary Sequence

5. CONCLUSION

Result of this implementation to learn how to specify the inputs by using switches and get output on HEX [0] and HEX [1] LEDs by using “Altera DE2-115 Board” FPGA device. The solution is to understand the idea of binary to hexadecimal conversion as show in Figure.15. “Altera DE2-115 Board” is significant for many applications in market today, so to get knowledge about implementation by using Verilog file practice on it as you want and performed simulations on various counter designs and implement designs on FPGA device utilizing switches, LEDs and seven-segment displays.

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4. IJISSET - International Journal of Innovative Science, Engineering & Technology, Vol. 1 Issue 5, July Be aware of the different meanings of the homophones “affect” (usually a verb) and “effect” (usually a noun), “complement” and “compliment,” “discreet” and “discrete,” “principal” (e.g., “principal investigator”) and “principle” (e.g., “principle of measurement”). Do not confuse “imply” and “infer.”