ISSN 2278-3091
Volume 10, No.2, March - April 2021
International Journal of Advanced Trends in Computer Science and Engineering
Available Online at http://www.warse.org/IJATCSE/static/pdf/file/ijatcse1141022021.pdf
https://doi.org/10.30534/ijatcse/2021/1141022021

Design and Implementation of DDS Module on FPGA

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ABSTRACT

The paper concerns the construction scheme of Direct Digital Synthesis (DDS) generator based on widely developed Field Programmable Gate Arrays (FPGA) technology. based on (DDS) it generates sine wave that frequency and phase is manageable is designed with direct digital synthesis (DDS) technology. It is showed that the design based on FPGA with DDS is dependable and practicable. The output wave by test reaches the essential aims, easy control and high performance. The DDS produce sinusoidal signal owns the features of modest circuit, easy to be measured, unchanging performance, high frequency conversion speed and fine accuracy etc. And its output frequency falls within the range of 0Hz ~ 150KHz with 5 Hz of steps.

Keywords— Direct digital synthesizer (DDS); FPGA; pipeline technology; look-up table

I.INTRODUCTION

Frequency synthesis technology is widely used in telecommunications, aerospace, instrumentation and other fields. At present, the commonly used frequency synthesis includes three branches such as direct, phase-locked, and direct digital ones. There into, Direct digital frequency synthesis (DDFS, generally referred to as DDS) is a new frequency synthesis technique through which waveforms are synthesized directly from phase of signals [1]. In recent years, DDS has been widely used in digital message systems due to its fine frequency resolution, high frequency conversion speed, and continuously variable phase characteristics etc. With the development of microelectronics technology, field programmable gate array (FPGA) devices show a rapid development [2].And the device shows daily increasing attractions to hardware design engineers and therefore has already been widely used in digital processing for its merits ofhigh run speed, large scale integration and outstanding field-programmable advantages, etc. This paper describes the principle and design of FPGA-based DDS, especially

II. LITERATURE SURVEY

K.ANITHA1, UMESHARADDY2, B.K.SUJATHA,[1] FPGA Implementation of High Throughput Digital QPSK Modulator using Verilog HDL. This paper proposes a Quadrature Phase Shift Keying (QPSK) using two dissimilar methods. QPSK is one of the forms of Phase Shift Keying (PSK) variation scheme. Generally a conventional QPSK modulator with Direct Digital Synthesizer (DDS) and arithmetic multiplier splits base band signal into I and Q phase which devours low throughput with difficulty in hardware implementation. Hence to create high throughput QPSK modulator, the first proposal customs an up and down accumulator for carrier generator in its place of DDS and arithmetic multiplier is modified as BOOTH multiplier. The second proposed method will produce the QPSK signal which is based on deposited QPSK phase data in ROM which eliminates totally the DDS and multiplier blocks of the modulator.

S.O.POPESCU, A.S. GONTEAN, [2]The paper presents the comparison performance in terms of error performance between two modulation techniques, the BPSK and QPSK modulation. Together modulations were executed on the Spartan 3E Starter Kit board. In order to compare the error performance of the two modulation techniques, it is necessary to express the error performance in terms of the average energy per bit (Eb). A brief explanation of theoretic aspects of the BPSK and QPSK modulations is also illustrated in the paper. This paper focuses on error performance of the BPSK and QPSK modulation techniques. Both modulations had been implemented on FPGA.

C. Erdoğan, I. Myderrizi, and S. Minaei,[3] FPGA Implementation of BASK-BFSK-BPSK Digital Modulators Field-programmable gate-array (FPGA) executions of binary amplitude-shift keying (BASK), binary frequency shift keying (BFSK), and binary phase-shift keying (BPSK) digital modulators are existing. The proposed designs are expected at educational purposes in a numerical communication course. They employ the least number of blocks compulsory for achieving BASK, BFSK, and BPSK modulation, and for complete integration with the other practical parts of the Altera Development and Education (DE2) FPGA board. The input carrier signal and the bit stream (modulating signal) are operator manageable. These digital modulators were established and assembled to a Verilog Hardware Description Language (HDL) netlist, and were later implemented into an Altera DE2 FPGA board. The functionality of these digital modulators was established through simulations using the Quartus II simulation software, and experimental dimensions of the real-time controlled signal via an oscilloscope.

S.O. Popescu*, A.S.Gontean* and G.Budura[4], Simulation and Implementation of a BPSK Modulator on FPGA. The paper presents the simulation of a BPSK Modulator using Matlab/ Simulink environment and System Generator, a instrument from Xilinx used for FPGA design as well as the execution of the modulator on a Spartan 3E Starter Equipment board. The

modulator algorithm has been executed on FPGA using the VHDL language on Xilinx ISE 12.4. The modified signal obtained from simulations was related with the signal obtained later implementation . The BPSK Modulator that we realized on the Spartan 3E Starter Kit board has, as a model, the 3rd implementation in System Generator. The carrier is generated internal, but in a ROM and that is the reason of which the sinus signal is denoted discontinuous, by instantaneous samples of 16 dissimilar values.

Mai Nozaki, Shingo Yoshizawa, Hiroshi Tanimoto[5]**,** VLSI Design of an Interference Canceller for QPSK OFDM-IDMA Systems. With increasing demand of machine to machine (M2M) message, wireless communication systems request simultaneous connections for many stations to cope with thus increasing communication throughput. We focus on interleave division multiple access (IDMA) that has superior user detection presentation and describe a VLSI design of an interference canceller that makes user detection in QPSK OFDM-IDMA systems. A conventional interference canceller has an subject of degradation in interleave memory amount. We propose a new architecture of dual-frame processing in an interference canceller by making use of an OFDM-IDMA frame structure. In FPGA operation, the proposed architecture has shown fewer hardware resources related with the predictable architecture.

Akhil Khanna, Anju Jaiswal, Harsh Jain[6], Design and Synthesis of Bandwidth Efficient QPSK Modulator for Low Power VLSI Design In current years digital designs have been extremely automated, and the digital modulation offers more data capacity, compatibility, higher data security, better quality communications and quicker system accessibility with digital services. This paper offers a QPSK module based on π/4 modulation technique. A simulation investigation on the bandwidth efficiency of the QPSK modulator has been implemented with the proposed technique; and thereby compared with the conventional BPSK modulation scheme. Synthesis and implementation of QPSK modulation technique is defined viz. subsystem modules of digital communication. The QPSK modulator element will be demonstrated using HDL code and simulation is completed using Modelsim 10.d simulator followed by synthesis and FPGA implementation of the design using Xilinx ISE design suite using Spartan-six FPGA kit.

III. PRINCIPLE OF A DIRECT DIGITAL SYNTHESIZER

Figure 1 shows a basic block diagram of the DDS circuit. The DDS is generally composed of a reference clock, a phase accumulator, a phase to amplitude conversion unit, a D/A converter and a low pass filter (LPF), etc. On receiving each clock pulse clkf , an addition of frequency control word X to cumulative sum of the phase data, which is output from accumulate register, is implemented on a N-bit adder, and the sum of the results Y is immediately fed into the accumulation register. The newest phase data generated in last clock cycle are on the one hand feedback to the adder by the accumulator register, so that an addition of frequency control data X with the adder's input is implemented in the next clock cycle; the other hand, as a sample address this value is sent into the phase to amplitude conversion circuit, through which corresponding waveform data are output according to the address value. Finally, the waveform data are converted into analog waveforms by the D/A converter and low-pass filter. Linear phase accumulation will continue on the phase accumulator in the role of the reference clock, and an overflow will occur when the cumulative result of the phase accumulator is equal to or greater than N 2 , then it turn back to the initial state, and waveform of a cycle is completed and output. This cycle is a frequency one for synthesizing DDS signal [3].

Changes in output frequency is achieved by changing the frequency control word X, when the control word X changes, the address through which the phase accumulator access RAM will be accordingly changed. If the value of X is small, the accumulator will access each RAM unit, thus sampling points in the lookup table are continuously accessed, and the output frequency is low; when the value of X is larger, the phase accumulator will skip some of the RAM unit, the number of sampling points reduces while the output frequency increases.

The frequency of DDS output signal is as following

$$f_{out} = \frac{f_{clk}}{2^N} \times X \qquad (1)$$

and 1 where out f means output signal clk f system synchronization clock, N bit length of adderX frequency control word. As can be seen from the above equation, one can get waveform with any frequency by changing bit length N of phase accumulator, frequency control word X, and synchronization clock clkf .

Frequency resolution of DDS is as following:

$$\Delta f = f_{clk} / 2^N \qquad (2)$$

When the reference clock holds constant, frequency resolution is determined just by bit length of the phase accumulator. In fact, waveform output from the D/A converter can be considered as a sampling of a continuous smooth waveform, so

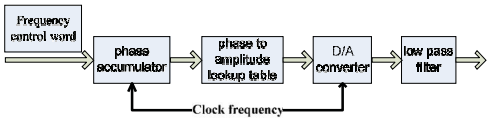

Figure 1. A basic block diagram of the DDS circuit

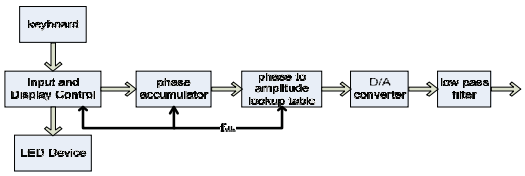

Figure 2. Block diagram of FPGA-based DDS

according to Nyquist law, the sampling rate should be more than twice the signal frequency. That's to say, if you want to fully recover signal from D/A converter's output, then the frequency of output waveform must be less than 2/ clkf , while the actual

maximum output frequency of DDS is no more than $f_{clk}/2$,

IV. DESIGN OF DIRECT DIGITAL SYNTHESIZER SYSTEM

Block diagram of FPGA-based DDS is shown in Figure 2. Quantified waveform data are stored in a ROM region, and an accumulated phase, whose value is recursive accumulation of phase with step X, as address to access the ROM unit. The obtained ROM data are then fed into the D/A converter and low pass filter, the required waveform, whose frequency is determined by clock CLK frequency clk f and step X, is finally generated. The main function of the input and display control module is to convert the frequency of the keyboard input value to corresponding frequency control word, and the frequency value is sent to LED display circuit [4]. The output frequency of DDS falls in the range of 0Hz~160KHzwith steps of 5Hz. Computational results show that, 48MHz of CLK frequency meets the design requirements:

$$f_{out} = 48MHz \cdot 40\% = 19.2MHz \geq 160KHz$$

$$\Delta f = \frac{f_{clk}}{2^N} = \frac{48MHz}{2^{32}} \leq 5Hz$$

Considering that frequency resolution should be equal to or less than the frequency step, and also word length of accumulator is generally in multiples of 8, the word length is finally chosen as N=32, while output width is 8-bit.

V. DESIGN OF SUB-MODULES IN DDS SYSTEM

A. The design of phase accumulator Operating speed of the phase accumulator directly affects the highest frequencies of output signal, so the most critical question of the module is how to improve the run speed of phase accumulator. The number of bits of frequency control word is 32, and accordingly that of the phase accumulator is also 32. If an wider bit adder is used directly to form the phase accumulator, the delay generated by the adder will leads to reduced accumulator speed. To improve the working speed of the accumulator, a pipeline design method has been adopted here [5]. Figure 3 is the diagram of a 32-bit phase accumulator with four level pipelined structures. In this module, 32-bit cumulative data are split into four bytes, and each of which is fed into a pipeline level respectively. The accumulator is composed of an 8-bit data latch, an 8-bit full adder, a 1-bit data latch. And it bears the phase accumulation function of adding the data output from a 32-bit accumulator register to a 32-bit input control word. Let the control word a be 7, then the simulation results of a 32-bit phase accumulator is shown in Figure 4.

B. Design of Phase to Amplitude lookup table Phase to Amplitude lookup table is actually a ROM region where stored encoded point array obtained by sampling a sinusoidal signal. This table is in fact a map of a phase sequence to a sampled sinusoidal signal, thereinto, the output of phase

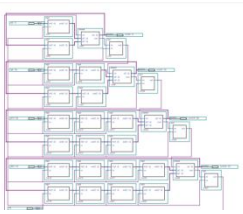

Figure 3. Diagram of a 32-bit phase accumulator with four level pipelined structure

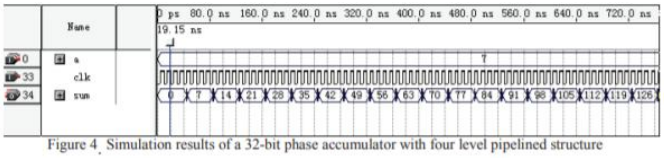

Figure 4. Simulation results of a 32-bit phase accumulator with four level pipelined structure

Figure 4. Simulation results of a 32-bit phase accumulator with four level pipelined structure

accumulator as the address for accessing corresponding ROM unit. In this case, the accuracy of output signal frequency resolution is determined by the number of bits N of phase accumulator, and the accuracy of the phase resolution is determined by ROM address width. In most Waveform Generator products, waveform data are stored in external ROM, which makes a clear system structure, convenient testing and maintenance service. But due to its low access speed the ROM itself possesses, both the overall system performance and operating frequency decreases. To solve this problem, a FPGA-based ROM for waveform data is designed. The Mega Wizard Plug-In Manager, whose settings interface is shown as Figure 5, in Quartus II is used to design a ROM. The highest 8 bits of output waveform of the phase accumulator are as address lines for accessing waveform memory, and corresponding binary sine amplitude is output, its amplitude falls in the range of 00000000-11111111. Finally, the binary sinusoidal data are used to achieve implementation of a sine ROM based on VHDL programming.

VI.SIMULATION WAVEFORMS AND EXPERIMENTAL RESULTS

The above-mentioned modules and the whole system are all designed by using VHDL. Figure 6 demonstrates the simulation waveforms of DDS main module when frequency of output signal is 10KHZ. The system described by using VHDL is compiled in Quartus Which is a set of

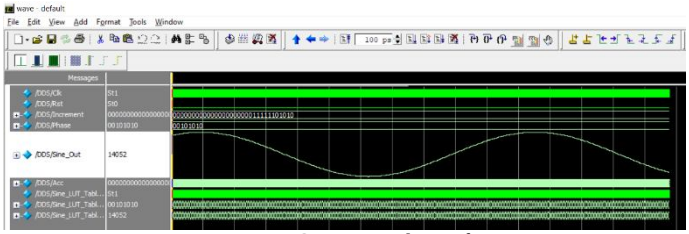

Figure 7. Output signal waveform

development tools for FPGA-based system, and then downloaded into a FPGA development board for constructing a target running environment. Figure 7 shows the output signal waveform observed on embedded logic analyzer Signal Tap T in Quartus T.

VII. CONCLUSIONS

In this paper, a DDS design and implementation method based on EDA technology is proposed. The system runs on a FPGA chip with the support of necessary peripheral circuit units and user interface devices. Output frequency falls in the range of 0Hz ~ 160KHz with steps of 5 Hz. The system for producing a sinusoidal signal keeps the features of simple
circuit, easy to be measured, constant performance, high frequency conversion speed and fine exactness etc.

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