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Global block level redundancy scheme for repair of clustered fault cells

P. Poornachandra[1], V R Seshagiri Rao[2]
[1]PG Students, Dept. of ECE, Institute of Aeronautical Engineering, Hyderabad, India
[2]Professor, Dept. of ECE, Institute of Aeronautical Engineering, Hyderabad, India

ABSTRACT

Spare full rows and columns are used in conventional memories to take care of any bad cells in memories. But this is not efficient as many chips do not become usable. Alternatively the spare redundant rows and redundant columns are bifurcated into blocks and block level repair can be attempted. A novel global feature is added to the spare blocks which enables the spare row(column) block to be used anywhere in the memory array. This memory hardware architecture can easily interface with embedded memory cores. A new algorithm, Essential Most Spare Pivoting (EMSP) is proposed which can be easily implemented in built-in configuration. The overhead area proposed in this paper is very less. The chip yield, reliability and repair rate are likely to improve significantly as per the simulation results.

Key words: SoC, VLSI, BISR, BIST

1. INTRODUCTION

Density of modern system-on-a-chip (SoC) plans will be developing rapidly; with the goal will be the limit Furthermore thickness of memories inserted inside them. Similarly as a consequence, installed memories have higher likelihood for faults and their manufacturing yield drops. Since inserted memories need aid involving those greater part about these days SoCs zone (90 % as stated by [1]), they need aid the principle wellspring for faults in SoCs Furthermore they Additionally overwhelm those general SoC yield. On move forward unwavering quality Also manufacturing yield, those the vast majority generally utilized approach may be to include a portion excess of the memories. Broken memory units are reinstated Eventually Tom's perusing excess components [2]. On account of SoC, memory testing What's more repair shed need aid gave in the chip itself (built-in self-repair, BISR), on account of it will be additional cosset compelling over utilizing outside test equipment.
Those BISR approach need three fundamental capacities. In memories need aid tried to different sorts about faults by built in self-test (BIST). In light of the flaw line data furnished Eventually Tom's perusing BIST, memories are broke down Eventually Tom's perusing the excess Investigation (RA) calculations which produce repair shed results for memories. Repair shed results comprise for majority of the data looking into which excess components are should make tended to As opposed to each solitary faun cell [3]. Execution about RA calculations will be regulated toward inherent repair shed examination (BIRA). As shown in figure 1 repair shed results given toward BIRA would connect will memories toward address reconfiguration (AR) which ensures that particular excess components are tended to As opposed to faun memory phones.

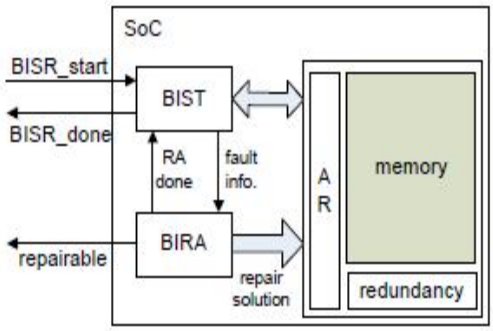

Figure.1. Built in Self repair Architecture

2. EXISTING METHOD

The memory array has sixteen rows and sixteen columns which are further divided into two column banks and two row banks. So the memory array in has four divided arrays. So there is a formation of four divided arrays [4]. Two extra row spares and column spares are provided. The column block (row block) in the extra spare columns (rows) can be utilized to replace faulty column cells (row cells) in the same column bank (row bank). Due to this, the extra spare row blocks (extra column blocks) are referred as local spare row blocks (local spare column blocks).

3. PROPOSED METHOD

In this paper the purview of spare row (spare column) blocks is expanded from local to global so that they can be used anywhere. For repair of accumulated faults, this global attribute is more useful. To allocate the global spares and columns, a novel algorithm Essential Most Spare Pivoting (EMSP) is used. The calculated area overhead for implementing EMSP is minimal.

In this paper, those global block-based excess architectures are suggested [5]. Excess rows/columns are still partitioned under row/column obstructs. However, the excess row/column squares can be used to trade faun column (column) pieces anyplace in the memory show. This worldwide trademark may be supportive for repairing bunch faults. In view of the recommended worldwide excess architectures, a heulandite modified essential spare pivoting (MESP) algorithm suitableness for BISR will be suggested [6]. The range overhead to actualizing that MESP algorithm is extremely low for less demanding discourse of the recommended strategies [11].

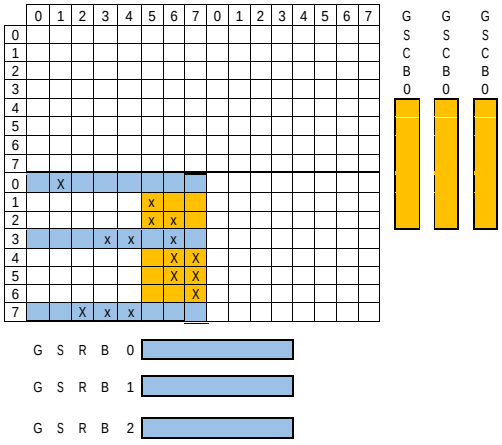

Figure.2. Global block-level redundancy scheme.

The advancement of embedded chip design and fabrication technology has led to rapid growth of the capacity and density of memories [10]. The yield improvement and testing issues have become the most critical challenges for memory manufacturing, as most of the chip area consists of memory elements as in figure 2. If we consider the case of repair in bit level, each and every cell of memory is being repaired [8]. But the time taken to repair the memory is high and the hard ware used to repair is also large. This is recorded in the Table 1.

Table.1. Observations on the Selection over Bit, Block and Word Level

	Bit	Block	Word
0th row	2 cells	2 blocks	Full word
1th row	1 cell	1 block	Full word
2th row	----------No fault----------		
3th row	2 cells	1 block	Full word
4th row	1 cell	1 block	Not repeated
5th row	5 cells	2 blocks	Not repeated

As in figure 3 the BISR flow chart is shown in Fig 9. Upon detection of fault in the spare memory during test by BIST, *erm_s* signal is set and particular flag of ARCAM module is activated [9]. BIST tests the main memory afterwards and if any fault is found, BIST is stopped temporarily and erm_m is activated. Subsequently entries are made in the FCR tables. When all the memory locations are not tested the BIRA will send *cnt* signal for resumption of main memory testing. After the end of testing by BIST and repair by BIRA [10], the contents of FCR are transferred to CAM. This is to facilitate address remapping procedure in Mission mode.

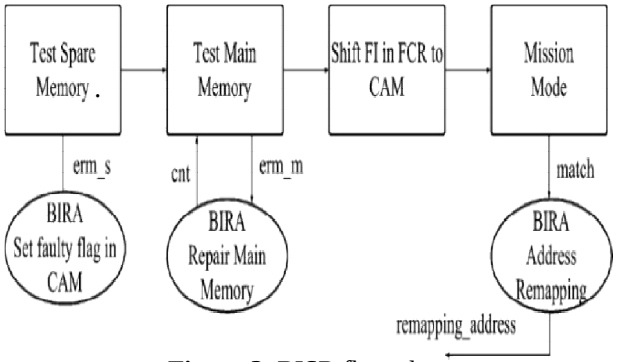

Figure.3. BISR flow chart

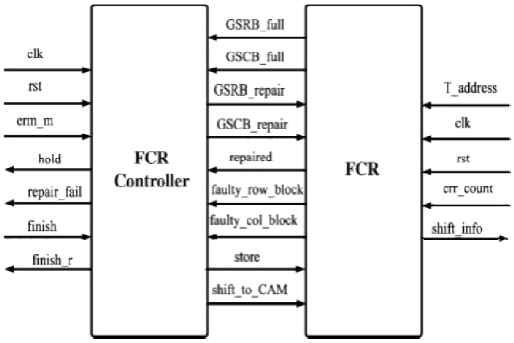

Figure.4. FCR Structure

The FCR and ARCAM details are elaborated in Figure 4 and 3 respectively. As shown in Fig in 10 the FCR structure contains the FCR controller and FCR. First the reset (*rst*) signal is given to FCR controller for one clock cycle to clear the contents of all the internal storage registers of FCR. Upon detection of faulty cell in spare memory (*erm_s = 1*), the respective faulty flag in ARCAM is marked. After BIST completes the spare memory testing, *err_count* signal is sent by ARCAM to the FCR for updating of counters to indicate the actual good available spare elements.

Thefaultaddressesare retrieved by processing a one-to-one mapping. Using this method, the BISR operates on all the fault location in the address memory, which is an exhaustive search operation.

4. RESULTS AND ANALYSIS

As shown in figure 5 the fault diagnosis in such case takes a larger time for reading and large address memory locations for storage. This overhead leads to low operation efficiency of memory application and result in high power consumption. To overcome these issues, a redundant fault addressing logic is suggested

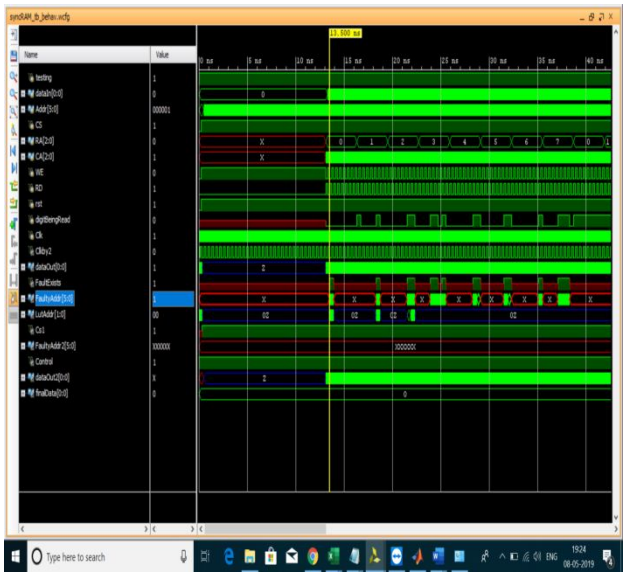

Figure.5. Simulation results

5. CONCLUSION

In this paper fault tolerance is proposed for embedded memories using global block based spares. The global spares and the memory are bifurcated into blocks. The replacement is designed at block level instead of full row or column level as in traditional methods. The global row blocks or global column blocks can be utilized to take care of the defective cells spread anywhere in the memory array. This global attribute is particularly useful for faults spread in a particular region in the memory array. The local based spare blocks cannot address this problem. For redundancy analysis, EMSP algorithm is proposed. As per the results shown in table 1, the area overhead for the implementation is very less. Making optimum use of spares the reliability, percentage repair rate and production net throughput can be enhanced considerably

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