ISSN No. 2278-3091
Volume 2, No.3, May - June 2013
International Journal of Advanced Trends in Computer Science and Engineering
Available Online at http://warse.org/pdfs/2013/ijatcse03232013.pdf

Study and Analysis of Low Voltage Low Power Pipelined ADC

Poonam[1], Manoj Duhan[2], Himanshi Saini[3]
[1]Student, DCRUST, Murthal, India, ghanghas.poonam20@gmail.com
[2]Professor, DCRUST, Murthal, India, duhan_manoj@rediffmail.com
[3]Assistant Professor, DCRUST, Murthal, India, himanshi.4887@gmail.com

ABSTRACT

This paper is concerned with improving the resolution of analog to digital converters (ADCs). The design of analog-to-digital converters is one of the most critical and challenging aspects in the development of new and more powerful electronic systems. The fast advancement of CMOS technology and more signal-processing functions is implemented for a lower cost, lower power consumption, and higher yield. In this Paper design of 3 bit Pipeline ADC using 1 micrometer CMOS technology and the schematic of the various circuits drawn in Tanner SEdit and the simulation waveforms obtained using Tanner WEdit have been included.

Key words: ADC (Analog-to-Digital Converter), CMOS (Complementary metal oxide semiconductor), Pipelined.

1. INTRODUCTION

Reduction of the power dissipation associated with high speed sampling and quantization is a major problem in many applications in personal communication devices such as wireless LAN transceivers including portable video devices such as camcorders. An ADC is a device that converts the input continuous physical quantity to a digital number that represents the quantity's amplitude. A small amount of error is also introduced as the conversion involves quantization of the input. The inverse operation is performed by a digital-to-analog converter (DAC). ADC performs the conversion periodically instead of doing a single conversion. The result is a sequence of digital values that have converted a continuous-time and continuous-amplitude analog signal to a discrete-time and discrete-amplitude digital signal. This level of power consumption may not be suitable for battery-powered portable applications and further power reduction is essential for power-optimized A/D interfaces [4].

Low voltage operation is another important key factor in these portable A/D interface environments. With the trend that A/D interfaces are incorporated as a cell in complex mixed-signal, the use of the same supply voltage for both analog and digital circuits can give advantages in reducing the overall system cost by eliminating the need of generating multiple supply voltages. Therefore, a new generation of A/D converters that can operate at supply voltage below 5 V is desired in order to be compatible with low-voltage systems.

CMOS technology is becoming increasingly attractive with recent improvements on higher speed and higher integration capability of the scaled technologies, as a cost effective solution for many applications once reserved for bipolar or other fast technologies [1]. This trend is expected to continue with scaled sub-micron CMOS technologies.

Among many types of CMOS A/D converter architectures, a pipeline architecture can achieve good high input frequency dynamic performances and as a high throughput as the flash ADC due to a S/H circuit in each stage of the pipeline for concurrent processing . In this dissertation, both fundamental and practical limitations to the power dissipation in CMOS A/D converters are examined, and techniques to allow low power and low voltage operation of the pipeline architecture are described. To verify the effectiveness of the techniques, a 3 bit pipeline A/D converter is designed using 0.18 mm CMOS technology

2. PIPELINED ARCHITECTURE:

Pipeline ADC is a popular architecture for data conversion schemes which require a compromise between speed and accuracy [5].

A pipeline ADC also named as sub ranging quantizer which uses two or more steps of sub ranging. In the first step, a coarse conversion is done. In the second step, with the help of DAC the difference to the input signal is determined. This difference is converted finer, and the results are combined in a last step.

This is a refinement of the successive-approximation ADC in which the feedback reference signal consists of the interim conversion of a whole range of bits rather than just the next-most-significant bit. Pipelined ADC is fast, has a high resolution, and only requires a small die size with the combination of the merits of the successive approximation and flash ADCs [2]. Although the pipeline architecture is inherently not as fast as a flash scheme, its serial nature results in a linear scaling of power and area with resolution opposed to the exponential scaling which occurs in a flash, resulting in the pipeline architecture being a more attractive solution around and above the 9 bit level.

Pipeline architectures simplify the ADC design and provide various advantages as:

- Optimize correction for overlapping errors with the help of extra bits per stage.

- Separate sample-and-hold amplifiers for each stage release each previous sample-and-hold to process the next incoming sample which enables conversion of multiple samples simultaneously in different stages of the pipeline.
- Consumption of low power.
- Higher-speed ADCs have less effort and less design time and less cost.
- Fewer comparators to become metastable which virtually eliminates sparkle codes [3].

But several difficulties are also imposed by pipeline ADCs:

- Reference circuitry and biasing schemes is complex.
- The number of stages through which the input signal must pass produce pipeline latency.
- For synchronization of all outputs critical launch timing is needed.
- Sensitivity to process imperfections that cause nonlinearities in offset, gain and other parameters.
- Compared with other architectures have greater sensitivity to board layout.

Figure 1 shows a block diagram of a general pipeline with k stages. The output of each stage is digitally corrected to obtain an accurate digital output.

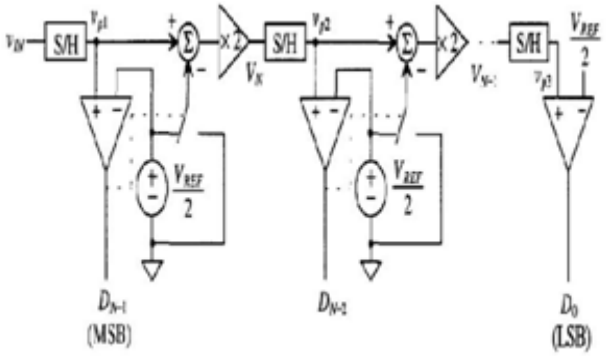

Figure 1: Block diagram of pipelined ADC

3. RESULTS

The simulations results of sine wave in 3 bit pipeline architecture of ADC designed with 1µm CMOS technology and 2.5V peak to peak rail voltage is shown as:

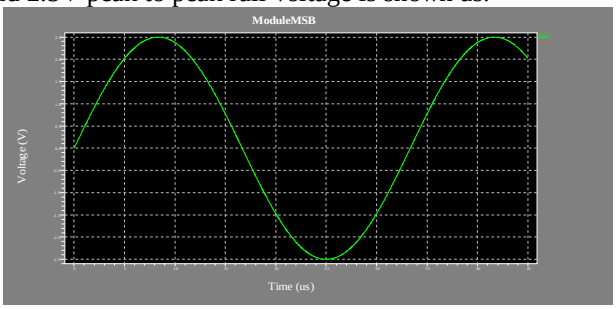

Figure 2: Input voltage signal of a 3-bit pipelined ADC

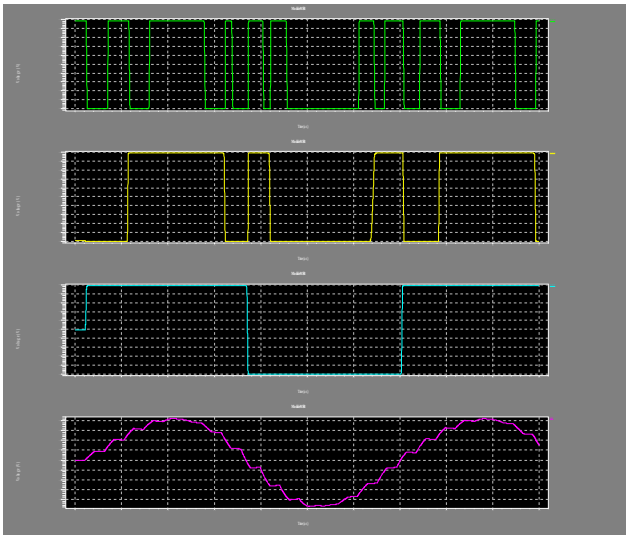

Figure 3 : Output voltage signal of 3 bit pipeline with sample and hold signal of input voltage

The Figure shows the transient analysis of 3 bit pipeline ADC. Sine wave is the input pulse signal applied with amplitude 2.5V and the output taken is D0, D1, D2 as shown in Figure 3. When input is applied to the circuit then it sampled by sampling pulses where we want to output. Then output is find across D0, D1, D2.First bit of the signal is find across D0, and second from D1, and third across D2 in a continue manner. For example if sampling pulses sample the signal at 2V then out from D0 is 0 and output from D1 is 1 and output from D2 is 0.Erroe in the wave form due to non ideal characteristics is the offset of the comparator. When the comparator computes the difference of between the two input signals, an internal offset voltage is added to this difference. Thus, when the two inputs are close together, the comparator may make a wrong decision and due to KT/C noise in sample and hold circuit.

4. CONCLUSION

This Paper presents a detailed study of design analysis of the pipeline architecture of ADC with 3 bit of resolution using 1µm CMOS technology.

Initially our work describes the study of design of low voltage low power pipeline architecture of ADC using individual blocks of comparator, sample and hold circuit, two stage op amp. The two stage Op-Aamp was designed for a gain of 80 dB and phase margin and unity gain bandwidth of 400MHz at a load capacitance 3pF. The sample and hold circuit designed using this Op-Amp. Noise analysis should be performed to get the required capacitor values so that the SFDR requirements could be met. The design of the comparator with high sampling frequency and analog bandwidth and it doesn't require high gains but works on the principle of positive feedback the values of Vref=0V. Considerable improvement in the parameters is observed when it is compared with the other architecture of ADC. A comparison among the pipeline ADC is done using the simulated results. The simulation waveforms of all the above

mention circuits are done using tanner simulation tool WEdit. In comparison with reported ADC, the pipelining ADC achieves high sampling frequency with relatively low power consumption. This Paper provides a considerable insight into the overall operation and advantages of pipeline architecture of ADC.

In this project the prototype ADC was built using two stage amplifiers in order to simultaneously achieve high gain and high swing. Using this two stage amplifier architecture is a big penalty in terms of speed and power dissipation. It would be desirable to use an amplifier with different Peak to Peak rail voltage to improve the speed and save power. Furthermore, these amplifiers would have less output swing than the two stage amplifier.

REFERENCES

1. P.E. Allen and D.R Holberg," CMOS Analog Circuit Design", Secon Edition, Oxford University Press, 2002.
2. 2 JohnA. McNeill, *Member, IEEE,* Christopher David, *StudentMember, IEEE,* Michael Coln, *Member, IEEE,*and Rosa Croughwell, *Member, IEEE,* "Split ADC" Calibration for All-Digital Correction of Time-Interleaved ADC Errors" , IEEE *TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS*, VOL. 56, NO. 5, MAY 2009.
3. 3 Junhua Shen and Peter R. Kinget, *Senior Member, IEEE,* "A 0.5-V 8-bit 10-Ms/s Pipelined ADC in 90-nm CMOS", IEEE *JOURNAL OF SOLID-STATE CIRCUITS*, VOL. 43, NO. 4, APRIL 2008.
4. 4 Lukas Dörrer, Franz Kuttner, Patrizia Greco, Patrick Torta, and Thomas Hartig, "A 3-mW 74-dB SNR 2-MHz Continuous-Time Delta-Sigma ADC with a Tracking ADC Quantizer in 0.13-_m CMOS", *IEEE JOURNAL OF SOLID-STATE CIRCUITS*, VOL. 40, NO. 12, DECEMBER 2005.
5. 5 Chun-Ying Chen, Michael Q. Le, *Member, IEEE,* and Kwang Young Kim , "A Low Power 6-bit Flash ADC With Reference Voltage and Common-Mode Calibration" , *IEEE JOURNAL OF SOLID-STATE CIRCUITS*, VOL. 44, NO. 4, APRIL 2009.
6. Ms. Rita, M. Shende, P. R. Gumble, ''Low Power High Speed 4 Bit Resolution Pipeline ADC Design in Submicron CMOS Technology'', International Journal of Advanced Research in Computer Science and Software Engineering , Volume 3, Issue 1, January 2013 , *Page | 189*
7. Jintae Kim, *Member, IEEE,* Sotirios Limotyrakis and Chih-Kong Ken Yang,"Multilevel Power Optimization of Pipelined A/D Converters" IEEE transactions on VLSI systems, vol. 19, no. 5, May 2011.