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Power Electronics Control and Communication for Grid Converter Applied to DPGS.

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Abstract—Distributed Power Generation Systems (DPGS) are changing the face of electric distribution and transmission. The objective of this paper is with help of Power electronic controller we can able to implement complex control algorithms combined with internal high speed communication interfaces. Thus it is possible to monitor, store and transfer a large number of internal variables that can be sent on-line to local or remote hosts in order to take new set points of different generation units. A floating-point Digital Signal Processor (DSP) and Field-Programmable Gate Array (FPGA) FPGAs provide higher performances in repetitive and massive computations than fixed-point DSPs, obtaining reduced execution times.

I. INTRODUCTION

Current Distributed Power Generation Systems have to execute complex control algorithms based on power unit internal and grid variables, which must be measured in real time, it is necessary to develop electronic controllers with high computational power in addition to both internal and external high speed communication capabilities.Nowadays, the control electronics of power converters, both in industrial and researching applications are built from: 1) on chip solutions based on fixed-point, 2) on-chip solutions based on Field-Programs, and 3) systems which include a floating-point, where the more complex control algorithms are executed.On-chip solutions include in a unique chip the control algorithms and the interface modules with the power converter, such as, PWM generators, encoder readings, activation of contactors, etc. Therefore, the controller electronic is cheaper, more robust and compact, the fault rate in the assembling process is considerably reduced, and the data transfers between processors are eliminated.The control and communication electronic solution has numerous applications in DPGS. The whole system can be divided into: 1. The Power Electronic System.2.The Control Electronic System; and 3.The High Speed Communication Interfaces.

In the last few years, the trend to use concurrent hardware for control purposes is increasing and FPGAs (Field-Programmable Gate Arrays) are becoming more popular since they provide higher performances in repetitive and massive computations. A sophisticated programming, complex algorithms running in floating-point DSPs can be often executed in FPGAs with shorter execution times.

II. POWER ELECTRONIC CONTROL ALGORITHMS

Fig. 1. shows the block diagram of the control system of the back-to-back NPC converter used for variable-speed wind turbines. The system is mainly divided into the line-side converter and the generator-side converter.The line-side converter (VSC1) is vector-controlled, using direct vector control and synchronous current control in the inner loops.

The grid power is controlled with a DC-bus voltage control. A line-side converter guarantees low AC current harmonic distortion and a controllable power factor.

- The *inner control structure* controls the active and reactive powers in a decoupled way. It is composed of a DC-bus voltage loop and some output AC current control loops.
- The *outer control structure* is strongly Application dependent: it depends on the generation system, and it should be capable to operate in either stand-alone mode or following the Transmission System Operator's guidelines.

The most important blocks of the VSC1 controlto balance the ripple in the NP voltage, the technique described in [9] and based on two modulation signals is used to compensate it. Regarding to the grid synchronization algorithm, in Fig. 2.It is formed by a synchronous reference frame phase locked loop (PLL) [10] and a delay signal cancellation algorithm (DSC) (Fig. 3 [11]) for separating on-line the positive and the negative sequences. This algorithm will be named as DSC-SRF-PLL.The DC-bus and the current controller are configured as a structure of cascade loops.The first one, that is the outer loop, is a conventional proportional + integral controller [13], whereas the inner current loop has the configuration indicated in Fig. 4.The proposed controller is based in three PI controllers connected in cascade, whose equations are shown in (1), and a state observer, that includes a Smith Predictor to compensatethe computational delay.The controller expressions areobtained from the equivalent discrete model of the continuous time LCL-filter model expressed in the *dq0*-frames and supposing dead-beat response for each LCL-filter model expressions.

The symbol ^ over voltages and currents represents estimated values. This symbol over converter parameters means the nominal or measured values at the starting up moment of the converter.

- $K_{p2} = k_{p2} \cdot \left(\frac{\hat{L}_2}{T_S} + \frac{\hat{R}_2 + R_{2a}}{2} \right)$, $K_{pc} = k_{pc} \cdot \frac{\hat{C}_o}{T_S}$ and $K_{p1} = k_{p1} \cdot \left(\frac{\hat{L}_1}{T_S} + \frac{\hat{R}_1 + R_{1a}}{2} \right)$.

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$$\vec{u}^*(k) = K_{p1}\cdot\left(\vec{i}_1^*(k) - \hat{\vec{i}}_1(k)\right) + \frac{T_S}{T_{i1}}\sum_{n=0}^{n=k-1}\left(\vec{i}_1^*(n) - \hat{\vec{i}}_1(n)\right) + j\omega_1\hat{L}_1\frac{\vec{i}_1^*(k)+\hat{\vec{i}}_1(k)}{2} + \hat{\vec{u}}_c(k)$$

$$\vec{i}_1^*(k) = K_{pc}\cdot\left(\vec{u}_c^*(k) - \hat{\vec{u}}_c(k)\right) + j\omega_1\hat{C}_o\frac{\vec{u}_c^*(k)+\hat{\vec{u}}_c(k)}{2} + \vec{i}_2^*(k) + \vec{i}_{1smith}(k) \qquad (1)$$

$$\vec{u}_c^*(k) = K_{p2}\cdot\left(\vec{i}_2^*(k) - \vec{i}_2(k)\right) + \frac{T_S}{T_{i2}}\sum_{n=0}^{n=k-1}\left(\vec{i}_2^*(n) - \vec{i}_2(n)\right) + j\omega_1\hat{L}_2\frac{\vec{i}_2^*(k)+\vec{i}_2(k)}{2} + \vec{e}_g(k)$$

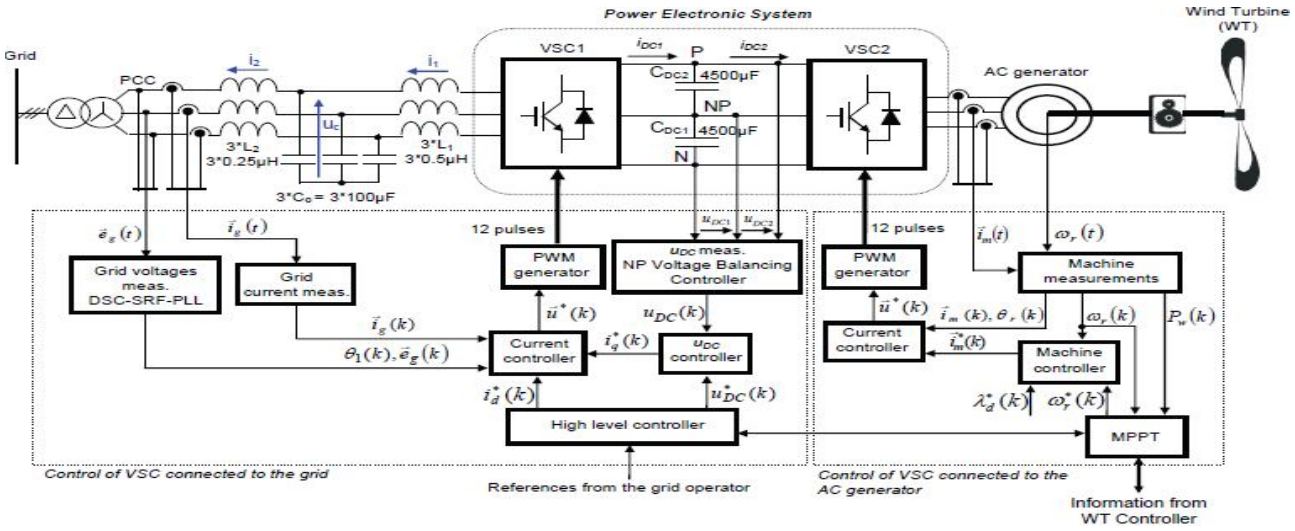

Fig 1.Block diagram of the Power Electronic Control algorithms.

- $T_{i2} = \dfrac{T_S K_{p2}}{\dfrac{\hat{L}_2}{\hat{R}_2 + R_{2a}} + \dfrac{T_S}{2}}$ and $T_{i1} = \dfrac{T_S K_{p1}}{\dfrac{\hat{L}_1}{\hat{R}_1 + R_{1a}} + \dfrac{T_S}{2}}$
- $R_{1a}$and $R_{2a}$are the active resistances. These are connected in series with R_1 and R_2, respectively, and theyreduce the effect of the LCL-filter oscillation frequency.
- $i_{1smith}(k)$ is the Smith Predictor (SP) output current, which is used to compensate the computational delay [15].
- The dead-beat gains are modified by the k_{p1},k_{pc}andk_{p2} factors. The selection of these factors is based on the improvement of the system stability.

The resultant control algorithm needs the information of i_1,i_2, $u_c$ande_g. Fig. 4. shows two possible alternatives of working, depending of the feed-backed variables. With both possibilities, the controller works correctly, only the transient response changes smoothly.

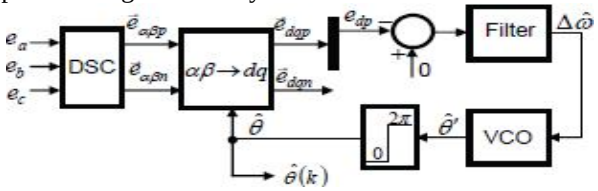

Fig 2. DSC-SRF-SPLL

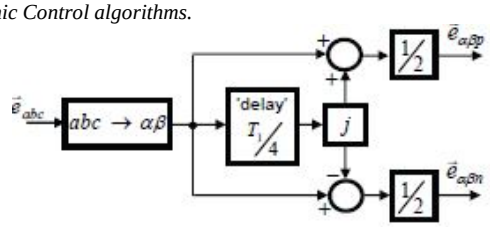

Fig 3.DSC (Delay Signal Cancellation) [19].

The generator-side converter (VSC2) controls thegenerator speed by a conventional indirect vector control withtorque control and synchronous current control as inner loops.The machine flux is controlled in open loop, setting it to itsrated value for a fast transient response. The speed reference is obtained from the block "Maximum Power Point Tracker(MPPT)", which adjusts the rotational speed to maximize the generated turbine power from the information about generatorspeed, generator power and wind speed [16].In the case of the wind turbines, the outer loop "High levelcontroller", which manages the VSC1 and VSC2 control loops,should guarantee that the injected energy keeps the gridvoltage characteristics between the allowed boundaries.

The distributed generation unit controls the gridactively, and can verify the standards of connection to the grideven under grid disturbances. Mainly, it is divided into tworegulations:

- The first regulation considers frequency-power. The grid frequency is an estimator of the generation-consumption power balance. When an increase in the grid frequency happens, the generator should decrease the injected power to balance the power contribution of the different generators.

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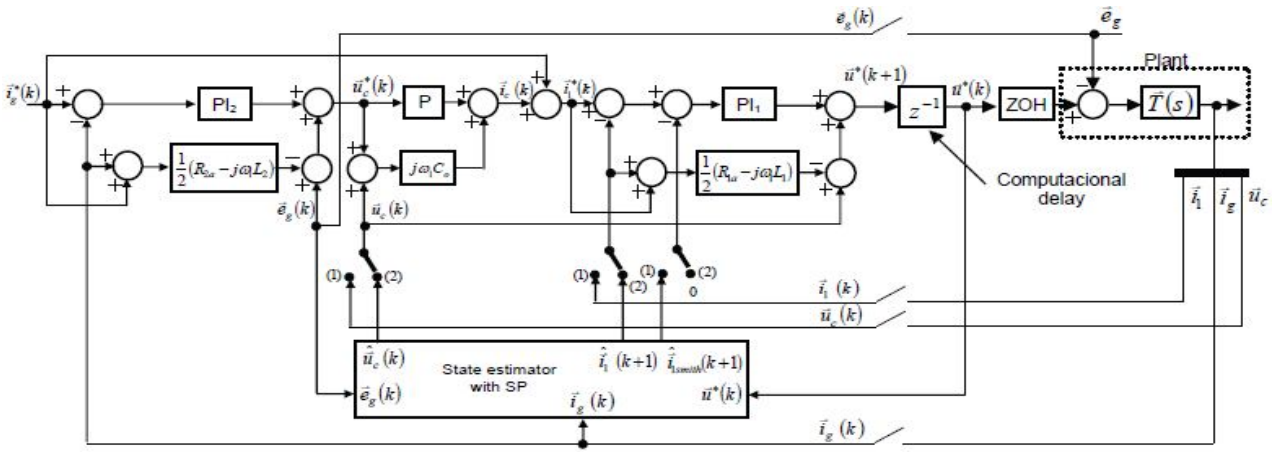

Fig.4. Block diagram of the proposed current controller for the converter connected to the grid through an LCL-filter.

- Simultaneously, a second regulation law controls the grid voltage by the injection of reactive power. When a low-grid voltage situation is detected, the generator provides reactive power (with a capacitive behavior); on the contrary, in high-grid voltage situations, the generator consumes grid reactive power, at which time it behaves as an inductor.

III. PROPOSED CONTROL ELECTRONIC SYSTEM

Fig. 5 proposes a control structure suitable for the application shown in Fig.1. It is divided into two parts: 1) the processor module; and 2) the coprocessor, which is divided into two different subsystems: (a) the co processing module with the FPGA and (b) the coprocessor power system interface, which consists of the data acquisition system, the optical interface with IGBTs (PWM and FAULT signals), the relay drivers, the CAN communication, and Compact Flash to store the boot program and the encoder drivers.

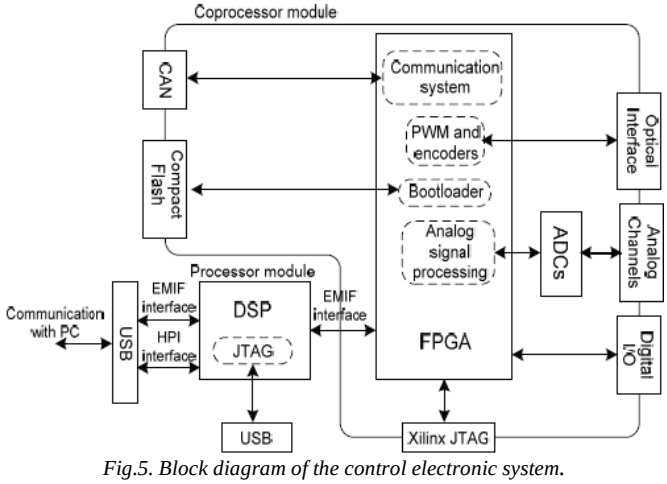

Fig.5. Block diagram of the control electronic system.

A. Task distribution between the two processing devices

The control electronic system is composed of floating-point DSP and a FPGA. In order to distribute tasks between these two devices, the main characteristics of DSPs and FPGAs have been taken into account with following considerations based on the task type:

1. Some tasks are constrained or linked by data dependences, so their location should be in the same device to avoid high data exchange rates between devices.
2. Since the selected DSP has limited integrated periphery,some tasks, like encoder reading or PWM generation, should be implemented in the FPGA.
3. Tasks with high computational load may not be implemented by the DSP in real-time, so they are processed in the FPGA.
4. A very repetitive task that rarely changes may be programmed in the FPGA, independently on their computational complexity.
5. Tasks with low or low-medium computational load,which are often modified by the programmer, are executed in the DSP. Such tasks are mainly control algorithms.
6. Non-critical tasks, such as representation, are notconstrained, so they can be placed in the DSP due to its ease of programming.

TABLE I. DISTRIBUTION OF THE TASKS BETWEEN THE TWO PROCESSORS.

DSP
For the line-side converter:
• Current vectorial controller with state estimator ([22]).
• Transformation abc→dq, and vice versa.
• DC-bus voltage controller ([21]).
• FFT of the grid voltages to identify the harmonic parameters.
• Synchronization with the grid ([20]).
• Sampling period: 200µs.
For the generator-side converter:
• Vectorial controller.
• Tracking of the maximum power point ([24]).
• Sampling period: 200µs
FPGA
• Communication with DSP.
• PWM generator (carrier frequency 2.5kHz).
• Control of the peripherals.
• Reading of generator encoders.
• Synchronization of the whole system.

B. DSP Programming

The development tool used for the DSP is Code Composer Studio v.3.3 [5], using C as programming language and the real-time operating system DSPBIOS by TI [18].

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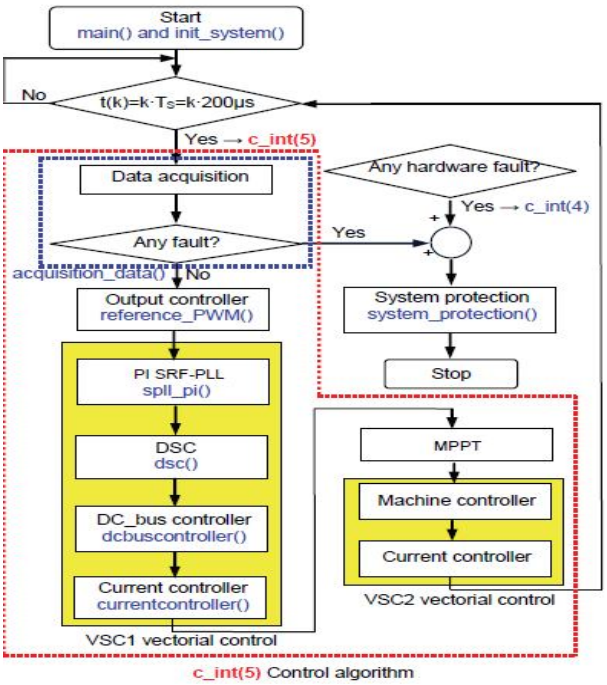

Fig. 6control algorithms flowchart of the back-to-back converter executed by the DSP.

C. USB Communication

The USB interface is implemented with the Cypress CY7C68001 EZ-USB SX2™ USB device [15]. It operates at two over three rates defined in [2]: 1) Full-speed, with a signalling bit rate of 12Mbits/s; and 2) High-speed, with a signaling bit rate of 480Mbits/s. The SX2 implements most of the requirements of the USB specification (Chapter 9 in [2]), and the remaining specifications are programmed in the DSP.The objective of using a USB interface in this work is toprovide a high-speed and high-bandwidth communication channel between the processors shown in Fig. 8. The critical elements in the chosen electronic structure are: 1) the DSP CPU occupation and 2) the selected communication channel occupation.

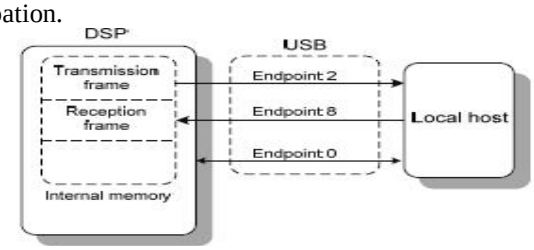

Fig. 7. USB channel composition

To reduce the DSP CPU occupation time, the data movement is achieved using the DSP EDMA (Enhanced Direct Memory Access Controller) [5] module.the DSP CPU intensively uses the EMIF interface during the controlexecuting algorithm, receiving the acquired data, sendingPWM references, etc. Therefore, to avoid possible conflict, the USB communication only uses the EMIF interface in the free slots of the control algorithm execution.

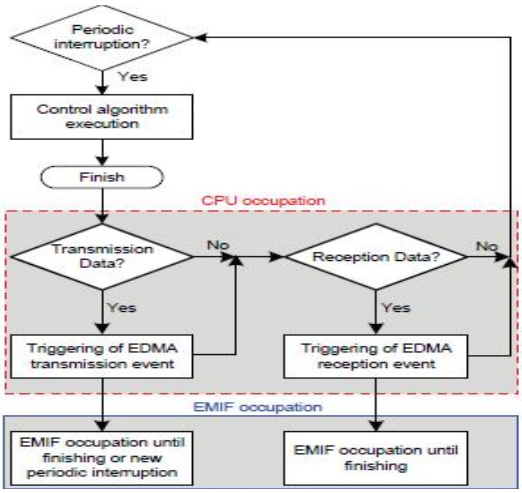

Fig8. DSP operations in the data transmission and reception processes of the USB interface.

The DSP operations in the transmission and reception processes and the different elements of DSP involved in each step. In every sampling period, the Power Electronic Controller acquires a set of variables essential to execute the control algorithms. These variables are stored in floating-pointformat in the DSP internal memory and will be sent by the USB interface to the local host later. When the control algorithm execution has finished, the CPU checks if there exist data to be transmitted. If affirmative, the CPU triggers the EDMA transmission event. Nevertheless, if there are no data to be transmitted, or after triggering the transmission event, the CPU checks a USB flag to verify if any data is pending for the DSP. In that case, the CPU triggers the EDMA event to receive data. Afterwards, the CPU becomes idle, waiting for a new periodic interruption to begin the control algorithm execution, whereas the EMIF interface carries out the transmission or reception of variables.

TABLE II. CPU OCCUPATION WITH THE USB COMMUNICATION.

Sampling Time	Frame Size	
	128 Bytes	64 Bytes
1s	<0.01%	<0.01%
200µs	0.04%	0.04%
10µs	2.45%	1.35%

The conclusion obtained from Table II and Fig. 9 is that the communication proposed in this work between the Power Electronic Control and Local Host based on a USB interface is a fundamental tool for any modern generation power unit since it permits the transfer, monitoring and storage of a large number of internal variables with a low CPU occupation ratio.

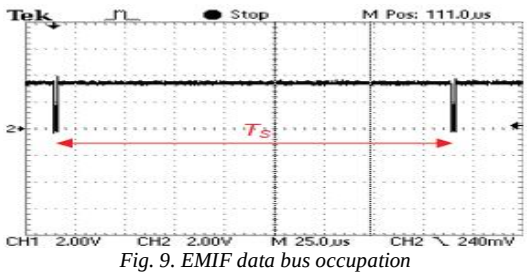

Fig. 9. EMIF data bus occupation

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D. Task scheduling analysis

In order to determine the capabilities of the processing systems, this subsection analyzes the task scheduling. The tasks are scheduled using a pre-emptive operating system (DSP-BIOS [18]). As the deadline for each one of them is equal to the minimum repetition time, the RMS (Rate Monotonic Scheduling) algorithm is the best option for task scheduling. The list of tasks, according to previous sections, is:

• Control task, with a CPU utilization factor of 15.773%.
• USB communication task, with a CPU utilization factor of 3%.
• CAN-bus task, with a CPU utilization factor of 2.5%.

So, the total CPU utilization factor (U) is 21.273%. The guaranteed utilization factor U is:

$$U < n(2^{1/n} - 1) \cdot 100 = 78 \qquad (2)$$

where*n* is the task number (3 in this case). It shows that the set of tasks can be executed without problem. As the actual value of *U* is lower than the limit value of 78%, the control task can assume more complex algorithms.

V. FPGA IMPLEMENTATION

The FPGA device can be considered as the master of the Power Electronic Control system. It is connected to the DSP through the EMIF interface and to the Power Electronic converter through the different modules implemented in the FPGA, such as the acquisition block, PWM generator, etc.

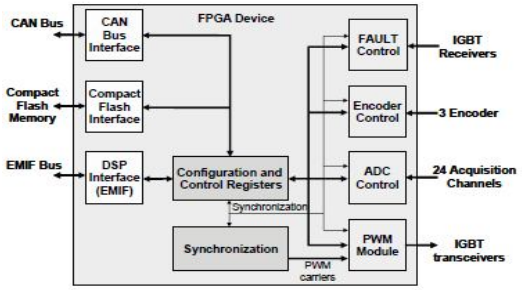

Fig. 10. Block diagram of the design implemented in the FPGA device.

A. DSP-FPGA synchronization

The synchronization module is in charge of the generation of a periodic pulse (SYNC) to determine the sampling period *TS*=200µs. This SYNC pulse is used to periodically interrupt the DSP so both devices can synchronize their operation every 200µs.After generating the SYNC signal at instant *k*, the FPGA acquires samples from the ADCs and encoders, while the DSP remains stalled until the acquired data are available in the FPGA. Then the FPGA transmits these data to the DSP, and the DSP transmits the new references to the FPGA PWMgenerator. These references are obtained by the algorithms computed at the instant *k*-1. With the acquisition data at instant *k* and the references applied at *k*, the new references to be applied at the instant *k*+1 are computed, shown in fig. 11.

Finally, in Fig. 12 the diagram block of the implementation of the synchronization module is shown. It is based on two 16- bit counters, used to generate both NPC converter carriers, as well as two comparison blocks in charge of generating the SYNC signal and controlling the up/down line of the counters.

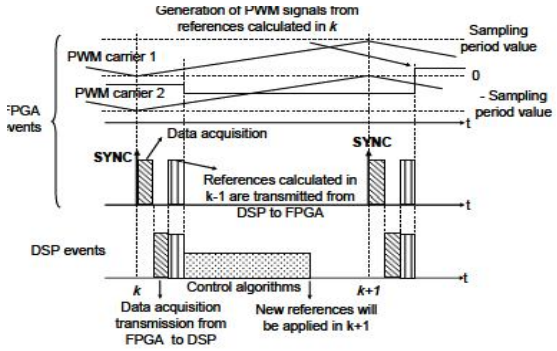

Fig. 11.Timing of the synchronization between the DSP and FPGA.

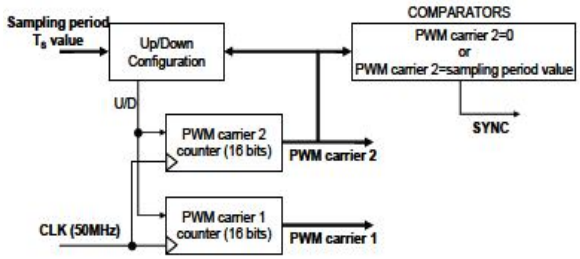

Fig.12.Block diagram of the implementation of the synchronization module

B. Configuration and Control Registers

The FPGA is managed and configured by the DSP, which uses an EMIF interface to transfer and receive data to and from the FPGA.

• Global Control Register. This enables the global system, the acquisition stage, the PWM generators and the control block in charge of monitoring the minimum width of modulation pulses as well as it configures the type of PWM and the method used to read the encoders.
• Registers for minimum width in pulses and dead-timeelimination. They allow the configuration of the modulation pulse minimum width and the dead-times of the signals that drive the IGBTs.
• Registers for IGBT PWM reference (6 per converter). In these registers the modulation signals are written which are the results of the VSC1 and VSC2 controllers implemented in the DSP.
• IGBT faults. The current state of the IGBTS of both converters are continuously analyzed and stored in a register from which the DSP can read information about the system. This register is also used for the generation of interruption 4.
• Encoder registers. There are six registers to manage up to three encoders with three common signals: two pulsechannels and an index signal. They contain the number of pulses received from every encoder in the last controlperiod in 32 bit format with a sign (two 16-bit registers per encoder).
• Acquisition faults and data registers. The system has 24registers available where the DSP can read the last samples acquired by the corresponding 24 acquisition channels.

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Furthermore, it is possible to configure a minimum and maximum value for each channel so that a fault is generated when the acquired sample is outside the minimum and maximum values. In this way, an acquisition fault register is composed by a fault bit for every channel.

• USB control. A data register is used to control the USBtransfers.

• Interruption masks. The system has three interruption mask registers: two are used for acquisition faults, whereas the other is dedicated to IGBT faults.

C. PWM Module

This block is dedicated to generate the PWM control signals for the IGBTs based on the techniques indicated in Table V. Bits 8, 9 and 10 correspond to the FPGA Global Control Register.

TABLE III: DIFFERENT IMPLEMENTED PWM TECHNIQUES.

Bit 10	Bit 9	Bit 8	Modulation type
0	0	0	Scalar PWM for VSC1 and VSC2
0	0	1	Scalar PWM with zero sequence for VSC1 and VSC2
0	1	0	Scalar PWM with zero sequence and two modulation signals for VSC1 and VSC2
0	1	1	Scalar PWM without zero sequence and two modulation signals for VSC1 and VSC2
1	0	0	Space Vector PWM for VSC1 and VSC2

Fig. 13 describes the block diagram of this module for scalar PWM. It is based on two comparators, which generate two basic control signals (*Sx2i*and *Sx1i* in Fig. 14) by comparing the PWM carriers from the synchronization module and the modulation commands from the register block written by the DSP.The "Pulse Width Checking" and "Control Signal Dead-time Generation" blocks are common both for scalar PWM and for space vector PWM.

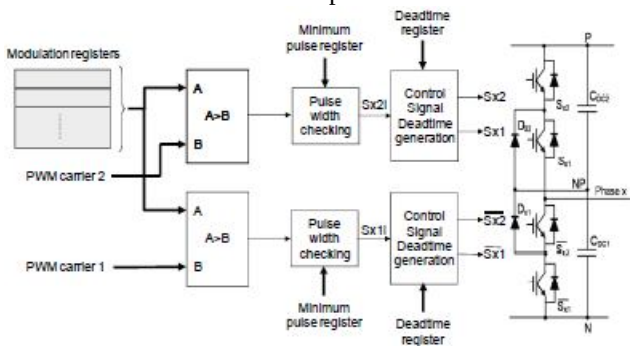

Fig. 13. Block diagram of the PWM generation module.

D. Acquisition Module

The acquisition system provides 12-bit samples at frequency fSof 5kHz, synchronized with the signal SYNC. The block diagram of the acquisition module can be observed in Fig. 14. The captured data are stored in a dual-port memory implemented in the FPGA, which is directly accessed by the DSP.these data are used to implement the control algorithms. The use of a dual-port memory allows having a dedicated port for the connection with the ADCs, while the other port is available for connection with the DSP.

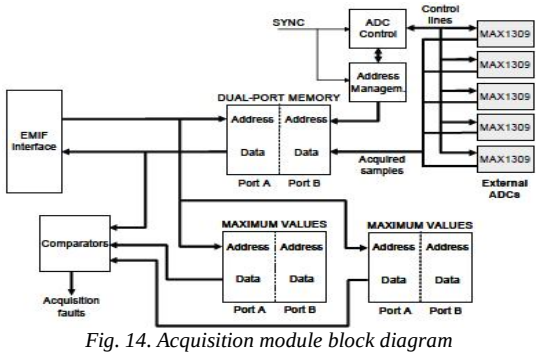

Fig. 14. Acquisition module block diagram

Fig. 15 shows the magnitude and phase of the developed filter, taking quantification effects into account according to the representation in Table IV. The resulting quantification error is below 1%.

TABLE VI.FIXED-POINT REPRESENTATION OF FILTER PERAMETERS

Parameter	Integer bits . Fractional bits
Input	1.11
Output	1.15
Coefficients	2.14
Product	2.26
Accumulator	4.26
State	1.15

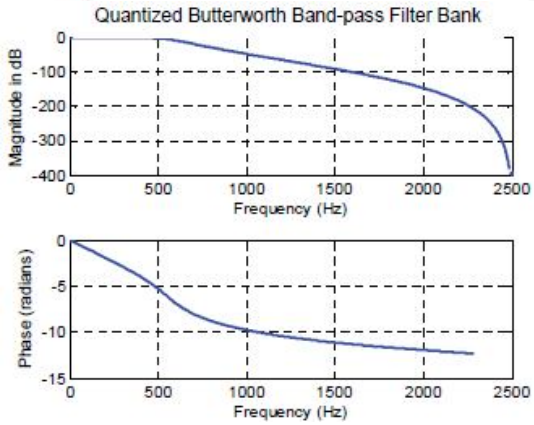

Fig. 15.Magnitude and phase of the developed filter.

Fig. 16 shows the simulated feedback waveforms of the DC-bus controller in the process ofsignal acquisition both with and without the filter. With the filter, the noise is reduced considerably and, therefore, the grid current THD (Total Harmonic Distortion) is reduced.

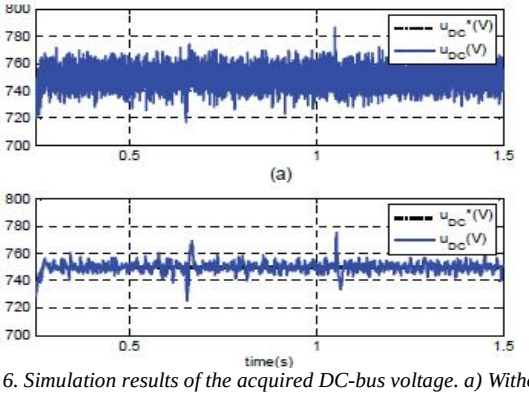

Fig. 16. Simulation results of the acquired DC-bus voltage. a) Without filter. b) With filter.

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E. Encoder Module

This module manages three encoders, each one of them with two pulse channels (CHA and CHB) and an index signal (CHI). The encoders are coupled to the generator and the wind turbine. The speed $\omega_m$is the following (2), shown in rpm (revolutions per minute):

$$\omega_m = \frac{60}{m \cdot N \cdot T_{CLK}} \qquad (3)$$

Where *m* is the number of CLK periods counted between two consecutive rising edges in Channel A of the encoder; *N* is the number of periods per revolution given by the encoder in a channel; and *TCLK* is the main CLK period of the FPGA design.

F. Fault Modules

Faults can be generated in the system by two different sources. Firstly, whenever an acquired sample is not in the interval defined by the corresponding minimum and maximum values, a fault is generated. Secondly, the fault signals generated by the IGBT are continuously monitored to detect any overcurrent and overvoltage situations.In order to avoid false faults resulting from glitches inIGBTs or acquisition modules due to noisy signal measurements, a low-pass digital filter has been implemented for every fault signal. These filters can be individually adjusted to improve the performance of the global system and to avoid unnecessary emergency stops.

G. CAN bus, Compact Flash and EMIF Interfaces

Fig. 17 shows the block diagram of the EMIF interface [5] implemented in the FPGA, where the address is decoded in writing accesses to enable the corresponding register where the input data is stored. In the reading accesses, a multiplexer is in charge of selecting the desired register according to the address bus in order to transfer its content to the data bus.

The interfacing of the different peripherals is one of the applications of the FPGA in this work. The timing diagrams of both CAN bus and Compact Flash memory are different than the timing diagrams of the DSP. In the case of CAN bus, a finite state machine is required to control and generate, according to the timing diagram, the suitable CAN signal.

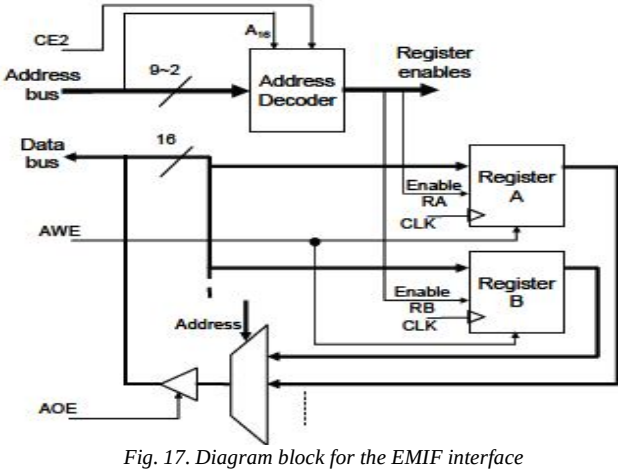

Fig. 17. Diagram block for the EMIF interface

H. Device Utilization

The FPGA design has been developed using VHDL. It has been implemented in a Xilinx XC3S500E FPGA [6]. The design is proposed for operation with a main frequency of 50MHz. Table V shows the resource consumption achieved.

TABLE V: DEVICE UTILIZATION FOR A XILINX XC3S500E FPGA.

Resource	Slices	RAMB16	DCM
Number	3180	3	1
Percentage	68%	15%	25%

VI. EXPERIMENTAL RESULTS

To carry out the experimental tests described here, theconverter has been connected to a real grid with a nominal voltage of 400V in 24.5 w a research laboratory under the following conditions: 1) non-null grid impedance; 2) mean THD in the phase neutral voltages of 19.5 %; and 3) mean percent imbalance of 3.5% .Fig. 18 displays the data stored in the local host during the converter operation. It shows the grid currents and voltages when VSC2 is consuming approximately 12kW and the reactive power reference of VSC1 is $Q^* = 0VAr$ (see Fig. 18.a), $Q^* = 8kVAr$ (see Fig. 18.c), and $Q^* = -8kVAr$ (see Fig. 18.d). In Fig. 18 the angle between the voltage and the current is 180º because the converter is consuming active power fromthe utility grid. The fundamental harmonic peak value is 24.5 w, and the value of the other harmonics is negligible. The nextmain group of current harmonics is placed around twice the switching frequency due to the behavior of three-level converters. For the two other experiments, the harmonics are very similar: only the fundamental harmonic amplitude increases approximately 5A.Other data stored in the local host during the converter operation are displayed in Fig. 19. Concretely, Fig. 19.a shows the temporal evolution of the DC-bus voltage under the different references of VSC1 reactive power indicated in Fig. 18, and also, different operation points of the AC machines, such as start, nominal-speed and stop. Initially, an auxiliary rectifier precharges the DC-bus capacitors up to the natural DC-bus voltage ($\sqrt{2}U_{base}$); and from this point, the VSC1 controller begins to work. In the first step the DC-bus reaches the u^*_{DC}through a process called 'soft-start', which consists of applying a slope reference of value $(u^*_{DC} - \sqrt{2}U_{base})V/s$. Then the DC-bus controller with its feed-forward action begins to operate normally. In spite of the different references applied with active and reactive power, u_{DC}does track to u^*_{DC}without observable errors, which verifies the correct operation of the DC-bus controller. Otherwise, Fig. 19.b represents the ripple in the neutral point of the converter. As was previously indicated, to reduce this ripple, the algorithm proposed in [9] is applied in this work. As is observed in Fig.19 the ripple is practically reduced to zero. The most critical points are the start and stop of the machine because in these situations the machine demands high unbalanced currents.

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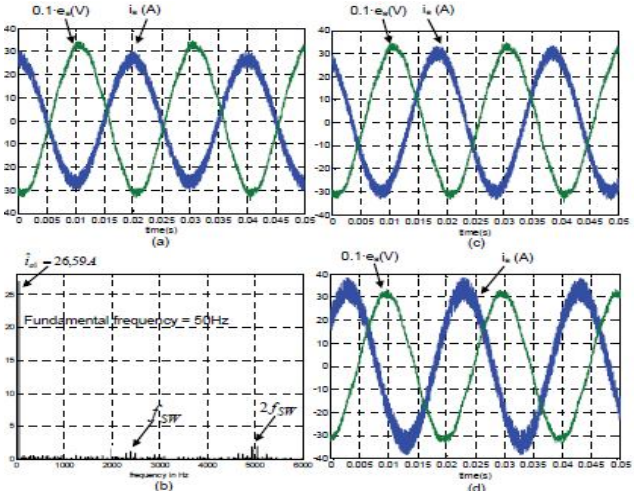

Fig. 18.Experimental converter waveforms. a) Phase voltage divided by 10 and phase current for Q = 0VAr . B) Phase current harmonic spectrum for the previous condition. c) Phase voltage divided by 10 and phase current for Q* = 8kVAr . d) Phase voltage divided by 10 and phase current for Q* = −8kVAr .*

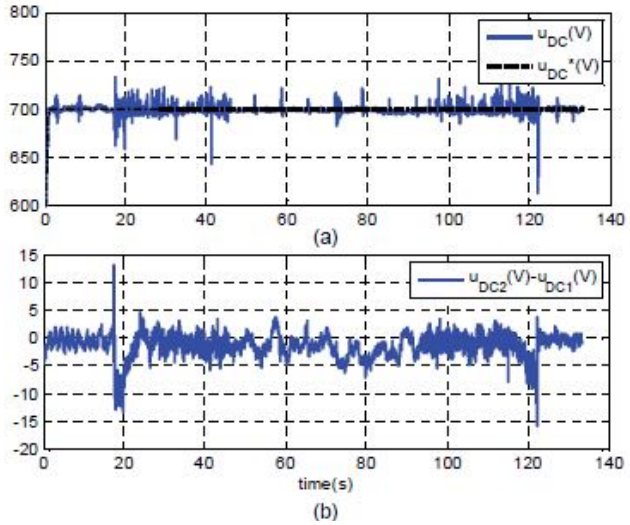

Fig. 19. Experimental waveforms of *uD*

VII. CONCLUSIONS

In this paper, two processors used (a floating-point DSP and a FPGA) allow the parallel implementation of algorithms, thereby increasing theprocessing rate. It is necessary to achieve an optimal taskdistribution to improve the control electronic systemperformance. The high-speed communication interfaces give to the system the capability to develop complex control algorithms based on a large amount of information obtained in real time from the grid and the generation unit. The proposed control electronic structure has been shown as well as the distribution of tasks between the two processors chosen, the DSP programming, the configuration of USB communicationand the FPGA programming. In an industrysome complex control algorithm can be migrated into the FPGA. Furthermore, a software processor core can be embedded in the FPGA to perform tasks implemented in the DSP

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