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Modified multilevel inverter with Minimum no of switches

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Abstract—**This paper presents a modified multilevel inverter. In introduction part the conventional multilevel inverter & switching techniques are explained. In second part switching signals of proposed work is explained. This paper provides a new multi level inverter with minimum number of switches. In the last simulation results are provided.**

*KEY WORDS-***Asymmetrical multilevel Inverter, Bidirectional switch, cascade multilevel inverter(CMLI),Total harmonic distortion**

Introduction

Power electronic inverters are becoming popular for various industrial drives applications. In recent years, inverters have even become a necessity for many implementations such as motor controlling and power systems.The concept of utilizing multiple small voltage levels to perform power conversion was patented by an MIT researcher over twenty years ago.

The multi-level inverter system is very promising in AC drives, when both reduced harmonic contents and high power are required.Multilevel inverters have been mainly used in medium or high power system applications, such as static reactive power compensation and adjustable-speed drives.A multilevel inverter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel inverter system for a high power application

The concept of multilevel inverters was first introduced in 1975. The term multilevel began with the three-level inverter. Subsequently, several multilevel inverter topologies have been developed.Up to now, several topologies of multi-level inverter system have been introduced. The main topologies used to generate a high voltage waveform using low voltage devices are the series H-bridge design, diode clamped inverter system and flying capacitor inverter system. Each of these topologies has a different mechanism for providing the voltage level.

Comparing with the other components, for instance, DC link capacitors having the same capacity per unit, diode clamped inverter has the least number of capacitors among the multi-level inverter system topologies but it requires additional clamping diodes[4].The flying-capacitor topology followed diode-clamped after few years. Instead of series connected capacitors, this topology uses floating capacitors to clamp the voltage levels.[10] H-bridge inverters have isolation transformers to isolate the voltage source but they do not need either clamping diode or flying capacitor inverters. Also, some soft-switching methods can be implemented for different multilevel inverters to reduce the switching losses and to increase efficiency. Recently, several multilevel inverter topologies have been developed.

The disadvantages of multilevel configurations over the two-level inverter configuration are the increase in the number of power devices required and the circuit complexity, which necessitates complex control schemes that add to the cost and reduces the reliability of the converter. This may lead the overall system to be more complex. Therefore , in practical implementation, reducing the number of switches and gate driver circuits is very important.

New topologies of symmetrical and asymmetrical multilevel inverters been investigated in this Paper. Which is generally for high number of steps associated with a low number of switches and gate driver circuits for switches and for generating all levels at the output? Finally, simulation results verify the validity of the proposed multilevel inverter.

CASCADED H-BRIDGES INVERTER:

A single-phase structure of an m-level cascaded inverter is illustrated in Figure 2.2. Each separate dc source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the dc source to the ac output by different combinations of the four switches, S_1, S_2, S_3, and S_4. To obtain $+V_{dc}$, switches S_1 and S_4 are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S_2 and S_3. By turning on S_1 and S_2 or S_3 and S_4, the

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output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate dc sources. An example phase voltage waveform for an 11-level cascaded H-bridge inverter with 5 SDCSs and 5 full bridges is shown in Figure 31.2. The phase voltage $v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5}$.

For a stepped waveform such as the one depicted in Figure 31.2 with s steps, the Fourier Transform for this waveform follows

$$V(\omega t) = \frac{4V_{dc}}{\pi}\sum_{n}\left[\cos(n\theta_1) + \cos(n\theta_s)\right]\frac{\sin(n\omega t)}{n}$$

where n=1,2,3....

The magnitudes of the Fourier coefficients when normalized witth with respect to V_{dc} are as follows:

$$H(n) = \frac{4}{\pi n}\left[\cos(n\theta_1) + \cos(n\theta_2) + \ldots + \cos(n\theta_s)\right]$$

where $n = 1, 3, 5, 7, \ldots$

The conducting angles, θ_1, θ_2, ..., θ_s, can be chosen such that the voltage total harmonic distortion is a minimum. Generally, these angles are chosen so that predominant lower frequency harmonics, 5th, 7th, 11th, and 13th, harmonics are eliminated. More detail on harmonic elimination techniques will be presented in the next section.

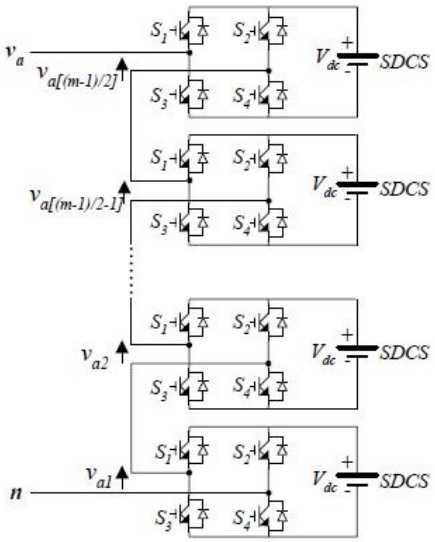


Fig 2.2 Single-phase structure of a multilevel cascaded H-bridges inverter

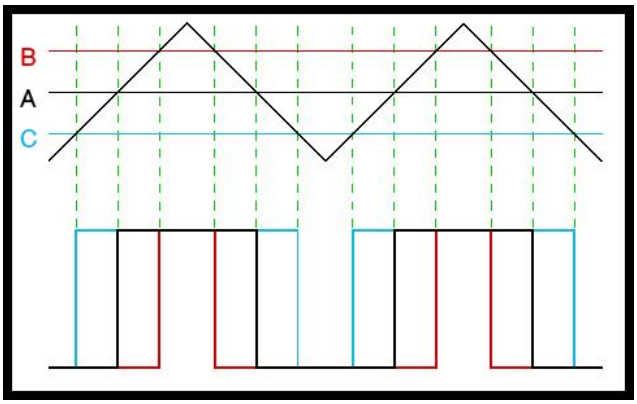
Multilevel cascaded inverters have been proposed for such applications as static var generation, an interface with renewable energy sources, and for battery-based applications. Three-phase cascaded inverters can be connected in wye, as shown in Figure, or in delta. Peng has demonstrated a prototype multilevel cascaded static vaR generator connected in parallel with the electrical system that could supply or draw reactive current from an electrical system.

The inverter could be controlled to either regulate the power factor of the current drawn from the source or the bus voltage of the electrical system where the inverter was connected. Peng [20] and Joos [24] have also shown that a cascade inverter can be directly connected in series with the electrical system for static var compensation. Cascaded inverters are ideal for connecting renewable energy sources with an ac grid, because of the need for separate dc sources, which is the case in applications such as photovoltaic's or fuel cells.

Cascaded inverters have also been proposed for use as the main traction drive in electric vehicles, where several batteries or ultra capacitors are well suited to serve as SDCSs. The cascaded inverter could also serve as a rectifier/charger for the batteries of an electric vehicle while the vehicle was connected to an ac supply as shown in Figure. Additionally, the cascade inverter can act as a rectifier in a vehicle that uses regenerative braking.

PULSE WIDTH MODULATION (PWM)

So, how do we generate a PWM waveform? It's actually very easy, there are circuits available in the TEC site. First you generate a triangle waveform as shown in the diagram below. You compare this with a d.c voltage, which you adjust to control the ratio of on to off time that you require. When the triangle is above the 'demand' voltage, the output goes high. When the triangle is below the demand voltage, the



MODELING PROPOSED MULTILEVEL TOPOLOGIES

In all well-known multilevel inverter topologies, the required number of power devices depends on the output voltage level. However, increasing the number of power semiconductor switches also increases the inverter circuit size,

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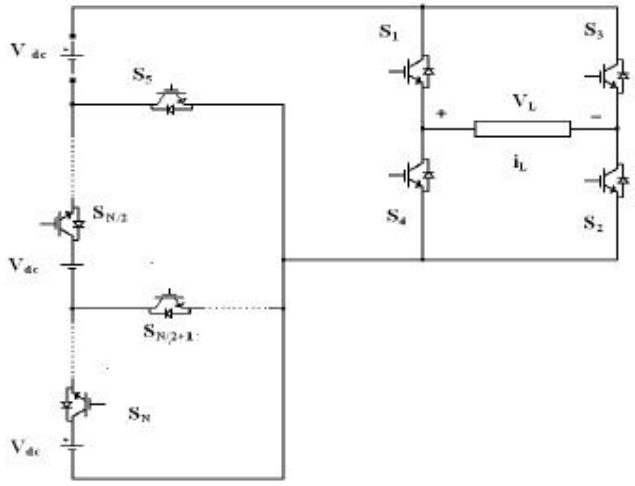
cost, and installation area and control complexity. To provide a large number of output levels without increasing the number of bridges, a new power circuit topology and a suitable method to determine the dc voltage sources level for symmetrical and asymmetrical multilevel inverter are proposed in this thesis.

Fig. 5.5 shows the proposed basic unit for a symmetrical multilevel inverter. The output for 7-level topology is shown in Fig



To increase the number of levels one power supply shall be added with two switches only. This proposed method is different from the method in [19] since it does not have any bidirectional switch and different from the method in [10] since it has less number of switches.

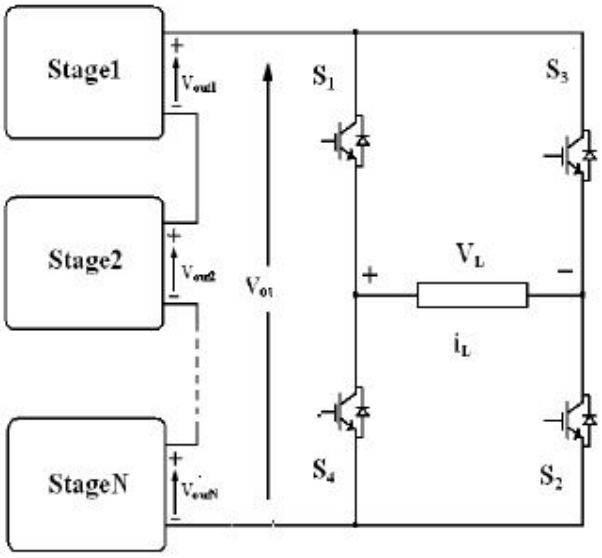
The effective number of output voltage steps (Nstep) in symmetric multilevel inverter is:

$$N_{Step} = 2n + 1 \quad (8)$$

Where n represents the number of dc voltage sources and the maximum output voltage (Vomax) of this n cascaded multilevel inverter is:

$V_{omax} = n \times V_{dc}$

Vo can be increased by connecting the N basic circuit given in Fig 5.5 in series as shown in Fig



7-LEVEL INVERTER TOPOLOGY

The figure below shows the arrangement for the 7-level inverter this topology is called as the symmetrical configuration of the switches with this arrangement we get the seven level with just 8 switches but the same level from conventional configuration requires 12 switches. The working of this circuit is clearly explained in the next chapter with the look up table which gives the switching states for all the levels.

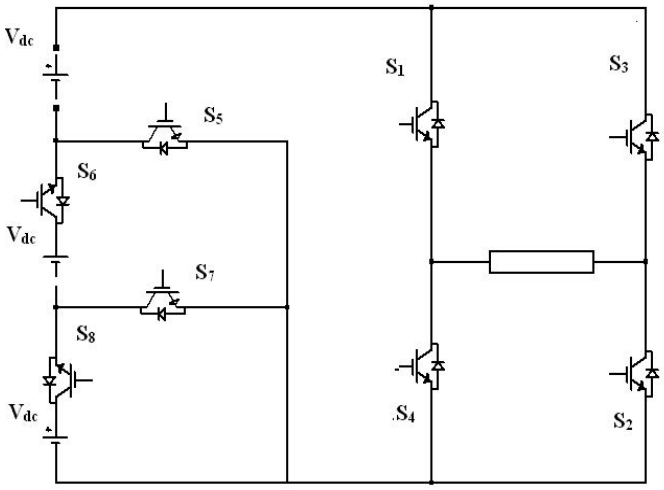


Fig 5.7 7-level configuration circuit

SUMMARY

This chapter discusses about the modeling of conventional topology which is a cascaded h-bridge multilevel inverter due to its advantages over other conventional topologies and develops a new topology with reduced number of switches than in h-bridge inverter for the same level. In the

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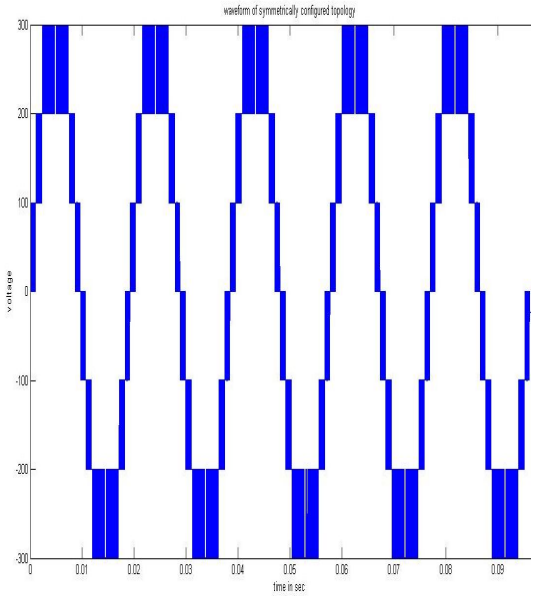
proposed symmetrical also discussed the matlab circuit and waveforms

RESULTS



ADVANTAGES:

1. The number of switches are reduced.
2. Switching Losses reduced.
3. Installation Area is reduced.
4. Cost of the cicuit is also reduced.

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