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MULTI-LEVEL CONVERTER WITH OPTIMAL NUMBER OF POWER ELECTRONIC DEVICES

P.Dharani[1], M. Vijayakumar[2]
[1]dharanipolumati@gmail.com, [2] vijay555.m@gmail.com

Abstract—In this paper, a new topology for cascaded multilevel converter based on sub multilevel converter units and full-bridge converters is proposed. The proposed topology significantly reduces the number of dc voltage sources, switches, IGBTs, and power diodes as the number of output voltage levels increases. Also, an algorithm to determine dc voltage sources magnitudes is proposed. To synthesize maximum levels at the output voltage, the proposed topology is optimized for various objectives, such as the minimization of the number of switches, gate driver circuits and capacitors, and blocking voltage on switches. The analytical analyses of the power losses of the proposed converter are also presented. The operation and performance of the proposed multilevel converter have been evaluated with the experimental results of a single-phase 125-level prototype converter.

Key words —**Bidirectional switch, cascaded multilevel converter, full-bridge converter, multilevel converter, submultilevel converter.**

INTRODUCTION

The basic concept of a multilevel converter is to use a series of power semiconductor switches that properly connected to several lower dc voltage sources to synthesize a near sinusoidal staircase voltage waveform. The small output voltage step results in high quality output voltage, reduction of voltage stresses on power switching devices, lower switching losses and higher efficiency.

The different basic multilevel converter topologies are the neutral point clamped (NCP) or diode clamped, the flying capacitor (FC) or capacitor clamped and the cascaded h-bridge (CHB). The main drawbacks of (NCP) topology are their unequal voltage sharing among series connected capacitors that result in dc-link capacitor unbalancing and requiring a great number of clamping diodes for higher level. The multilevel converter uses flying capacitor as clamping devices. These topologies have several attractive properties in comparison with the NPC converter, but these converters require an excessive number of storage capacitors for higher voltage steps. The CHB topologies are proper option for high level applications from point of view of modularity and simplicity of control. But, in this topology, a large number of isolated dc voltage sources are required to supply each conversion cell. It increases the converter cost and complexity.

This paper proposes a new modular and simple topology for cascaded multilevel converter that produces a high number of levels with the application of a low number of power electronic components. Then, a procedure for calculating the values of required dc voltage sources is also proposed. In addition, the structure of the proposed topology is optimized for various aims.

1.1 BASIC TOPOLOGY

The basic unit for multilevel converters, which is recommended, is illustrated in Fig. 1(a). This consists of a capacitor (with voltage equal to V_{dc}) with four bidirectional switches. The typical output waveform of V_o is shown in Fig. 3.1(b). It is noted that three values can be achieved for V_o.

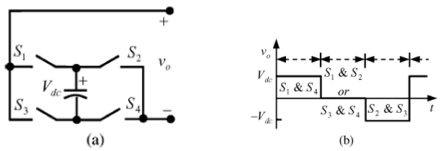

Fig 1(a) Basic unit (b) Typical output waveform of *Vo*

The proposed unit requires bidirectional switches with the capability of blocking voltage and conducting current in both directions. Several arrangements can be used to create such a bidirectional switch.Fig.3.2 presents a number of these connections. To simplify the scheme of the converter, it is interesting to consider the advantages and disadvantages of each structure.

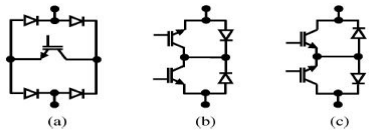

Fig 2 various methods for arranging bidirectional switches

The switch shown in Fig. 3.2(a) is easy to control, but its ON-state voltage drop is high. It is equal to the sum of voltage drops of two diodes and one insulated gate bipolar transistor (IGBT). The switch shown in Fig. 3.2(b) decreases the ON-state voltage drop, but needs two IGBTs. One possible disadvantage is that each IGBT requires an isolated gate driver circuit, configuration. The conduction losses are identical to the configuration shown in Fig. 3.2(b). The advantage of this configuration over the previous one is that each bidirectional switch requires a gate driver circuit. Therefore, we will use this configuration in the proposed multilevel converter.

The basic unit shown in Fig. 3.1(a) can be extended as shown in Fig. 3.3(a). The basic units in series can increase the possible values of V_o. If m capacitors are used in the extended unit shown in Fig. 3.3(a), then the number of output voltage steps (N_{step}) and switches (N_{switch}) are, respectively, given by the following equations:

$$N_{step-} m(m+1)+1 \qquad N_{switch} = 2(m+1)$$

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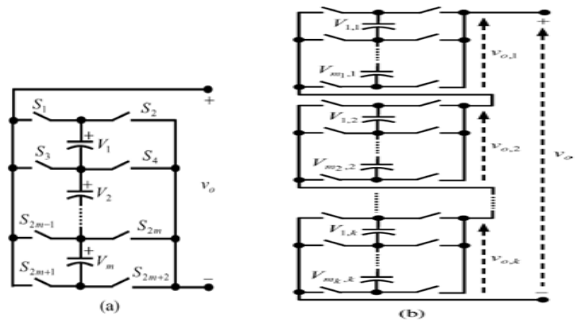


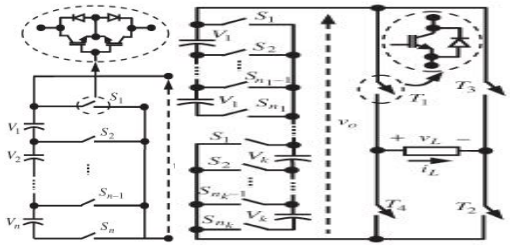
Fig 3.Extend unit(a) Extended basic unit (b) *k* basic units connected in series

Now, consider that k basic units of Fig. 3.(a), as shown in Fig. 3.(b), are used in series where the structure of the first unit, second unit,..., and the k_{th} unit have $m_1, m_2, ..., m_k$ capacitors, respectively. It is important to note that two switches of each unit turn on in different modes of converter operation.

In this case, the number of output voltage steps and switches are, respectively, given by the following equations:

$$N_{step} = \prod_{i=1}^{k} [m_i(m_i + 1) + 1] \qquad N_{switch} = \sum_{i=1}^{k} [2(m_i + 1)]$$

MODELLING OF MULTILEVEL CONVERTER



(a) **(b)**

Fig 4 Modeling of (a) Basic unit (b) Multilevel Converter

The basic unit of the sub multilevel converter, presented is illustrated in Fig.4 (a). It consists of several capacitors (with dc voltages) and bidirectional switches. If *n* capacitors are used, *n* + 1 different values can be obtained for v_o, by *n* + 1 bidirectional switches. The output voltage of this sub multilevel converter has zero or positive values. The proper configuration of bidirectional switches is arranged by a common emitter connection of two IGBTs, which each one of IGBTs has an anti parallel diode. Because the emitters of two IGBTs are common, the base voltage of each IGBT can be measured versus its common emitter. Therefore, a bidirectional switch requires a gate driver circuit in this configuration. This configuration of bidirectional switch is used in this paper, to make it comparable with one presented.

The cascaded connection of these sub multilevel converter increase the possible value of v_o, effectively. But, it can only generate the positive output voltages. To generate both positive and negative voltages, a full-bridge converter is connected to the output terminal of the cascaded connection of sub multilevel converters. But, the unidirectional switches in the full-bridge converter and some bidirectional switches, such as S_1, must operate at the high output voltage and need higher voltage blocking.

As a result, the cost and losses will be increased and its industrial applications will be limited. Fig.6.1 (b) shows *k* sub multilevel converters in series, where the structure of the first till k^{th} sub multilevel converters has $n_1, n_2, \ldots, n_k$ bidirectional switches, respectively. In this case, only one switch of each sub multilevel converter turns on in different operation modes of the converter. The number of output voltage levels (N_{level}) and IGBTs (N_{IGBT}) are given by the following equations, respectively:

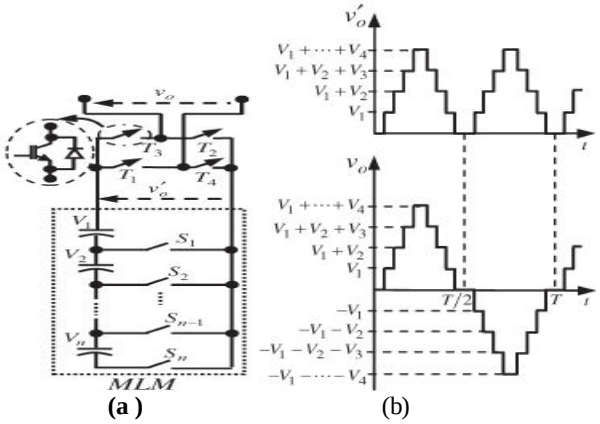
$$N_{level} = 2\left(\prod_{i=1}^{k} m_i\right) - 1 = 2(n_1 \times n_2 \times \ldots\ldots \times n_i) - 1$$

$$N_{IGBT} = 2\left(\prod_{i=1}^{k} n_i\right) + 4 = 2(n_1 + n_2 + \ldots\ldots + n_k)$$

The maximum value of the output voltage (V_{omax}) can be obtained, as follows:

$$V_{0max} = \sum_{i=1}^{k} (n_i - 1)V_i$$

PROPOSED TOPOLOGY:



(a) (b)

Fig 5(a) Proposed sub multilevel topology (b) typical output waveform of v_o.

Fig.(a) shows the proposed topology for a sub multilevel converter, hereafter called multilevel module (MLM), which is used for the implementation of the proposed multilevel converter topology. It consists of *n* dc voltage sources and *n* bidirectional switches. A MLM produces a staircase voltage waveform with positive polarity. It is connected to a single phase full-bridge converter, which particularly alternates the input voltage polarity and provides positive or negative staircase waveform at the output. The full-bridge converter has four unidirectional switches, which consists of an IGBT and an anti parallel fast recovery diode. The typical output waveforms of and v_o are shown in n Fig (b). It is noticeable that only one switch turns on in different operation modes of the MLM and also, both switches T_1 and T_4 (or T_2 and T_3) cannot be simultaneously turned on because of a short circuit occurrence across dc voltage sources and then the voltage v_o would be produced. Summarizes the values of the output voltage of a MLM and corresponding full-bridge converter for different state of switches $S_1, S_2 \ldots S_n, T_1 \ldots T_4$. State conditions 1 and 0 means that the switch is on and off, respectively. For simplicity, the on state voltage drops of switches have been neglected. As it can be seen, $2n + 1$ different value can be obtained for v_o.

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The proposed multilevel converter topology, which is based on the combination of MLMs and full-bridges converters, is shown in Fig. The structure of the first till k^{th} MLM has n_1, n_2. . . n_k bidirectional switches, respectively. Each MLM can generate a stepped voltage waveform with positive polarity. The full-bridge converters provide positive and negative stepped voltage waveforms in their output.

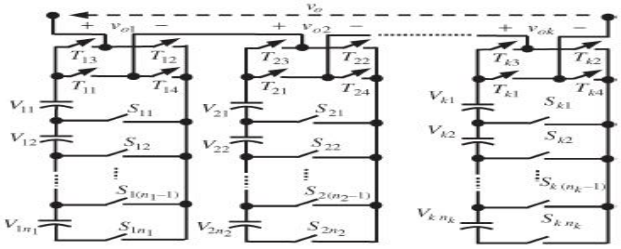

Fig (6) Proposed multilevel converter topology.

The different output voltage levels can be determined by the combination of switching states of MLMs. It is obvious that only one switch of each MLM turns on in different operation modes of the converter without considering the zero voltage state of MLMs. If the proper values for dc voltage sources are selected, then, the output voltage of the converter will be obtained between -and + . the output voltage of the proposed topology for different switching states. It is noticeable that there are two switching states for producing the zero voltage level

It should be noted that the capacitors can be replaced with the dc voltage sources in the proposed topology. When ac voltage is already available, then, multiple dc sources can be generated using isolated transformers and rectifiers, too.

If the voltage sources are changed during the converter operation, the voltage balancing should be done. For example, the output voltages of fuel cells are variable. Therefore, if they are used at dc-link, the quality of output voltage of the converter will be reduced. The hardware proposed method to dc-link balancing is shown in fig The capacitor voltages are controlled with the DC/DC converters.

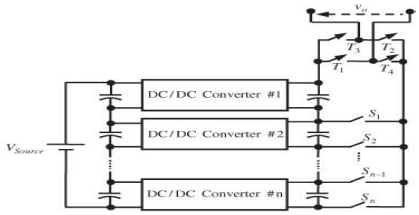

Fig (7) . DC-link voltage balancing

If the dc voltage sources are considered to be equal in MLMs, the structure of the proposed topology will be symmetrical. In the asymmetrical structure of the proposed topology, similar to the asymmetrical cascaded multilevel converter, there is only one switching state for each output voltage level (except the zero level) to produce unequal values for v_o.

In this paper, to reduce the number of components, the asymmetrical structure has been studied. It is noticeable that the asymmetrical structure has circulating energy problems. Therefore, if diode-based rectifiers are used for dc voltage sources, their dc-link voltages can increase their values dangerously.

Considering the first dc voltage source (V_{11}) as the base value of the per-unit system, i.e.,

$$V_{base}=V_{11}=V_{dc}$$

Then, the normalized values of the dc voltage sources for producing all levels (odd and even) in the output must be chosen using the following algorithm.

For module 1

$$V_{11}=V_{dc} \qquad V_{1i}=V_{11}=V_{dc} \quad i=2,\ldots\ldots n_1$$

For module 2

$$V_{21}=V_{11}+2\sum_{i=1}^{\kappa}V_i=(2n_1+1)V_i$$

$$V_{2i}=V_{21}(2n_1+1)V_{dc} \quad i=2,\ldots\ldots n_2$$

For module 3

$$V_{31}=V_{11}+2\sum_{i=1}^{n_1}V_{1i}+2\sum_{i=1}^{n_2}V_{2i}=(2n_1+1)(2n_2+1)V_{dc}$$

$$V_{3i}=V_{31}=(2n_1+1)(2n_2+1)\,V_{dc} \qquad i=2,\ldots\ldots n_3$$

In general, for the *m*th module

$$V_{m1}=V_{11}=\sum_{i=1}^{m-1}\sum_{j=1}^{n_i}V_{ij}=\prod_{i=1}^{m-1}[2(n_i+1)]\,V_{dc}$$

$$V_{mi}=V_{m1}=\prod_{i=1}^{m-1}2(n_i+1)V_{dc} \qquad i=2,\ldots\ldots n_m$$

By using the proposed algorithm, the maximum value of the output voltage (V_{omax}) is obtained, as follows:

$$V_{0max}=\sum_{i=1}^{\kappa}\sum_{j=1}^{\kappa}V_{ij}=\sum_{i=1}^{\kappa}(n_i\times V_{11})$$

The number of output voltage levels can be determined by the following equation

$$N_{level}=\prod_{i=1}^{\kappa}(2n_i+1)$$

$$=(2n_1+1)\times(2n_2+1)\times\ldots\ldots\times(2n_k+1)$$

$$=(2n_1+1)\times(2n_2+1)\times\ldots\ldots\times(2n_k+1)$$

Considering the selected common emitter configuration for bidirectional switches, the number of power IGBTs in the proposed topology can be obtained as follows:

$$N_{IGBT}=2(n_1+n_2+\ldots\ldots\ldots n_k)+4k$$

It is important to note that the number of IGBTs and main diodes are the same.

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OPTIMAL STRUCTURES:

.Maximum Number of Voltage Levels with Constant Number of IGBTs:

The desirable object in a multilevel converter is maximizing the number of levels using the minimum number of IGBTs. The question concerning the proposed structure is that for the constant number of IGBTs, which topology can provide a maximum number of output voltage levels?

The product of numbers, whose summation is constant, will be maximum, when all are equal.

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$$n_1 = n_2 = \ldots\ldots = n_k = n$$

$$k = \frac{N_{IGBT}}{(2n+4)}$$

Now, the value of *n* must be determined. The maximum number of voltage levels will be determined

$$N_{level} = (2n+1)^k$$

$$N_{level} = [(2n+1)^{1/(2n+4)}]^{N_{IGBT}}$$

Fig. 8 shows the variation of (2*n* + 1)1/(2*n*+4) versus *n*. It is clear that the maximum number of voltage levels is obtained for *n* = 2. Thus, a structure consisting of two bidirectional switches (i.e., two dc voltage sources) in each MLM can provide the maximum voltage levels for v_o with using minimum numbers of IGBTs.

It is necessary to notice that the number of components is an integer. Thus, if an integer number is not obtained, the nearest integer number should be selected.

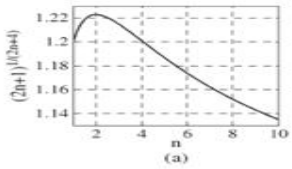

Fig (8) Variation of (2*n* + 1)1/(2*n*+4) versus *n*,

4.2.2. Maximum Number of Voltage Levels with Constant Number of Capacitors:

Suppose the number of capacitors (dc voltage sources) is constant and equal to ($N_{capacitor}$), the question in this section is which topology provides the maximum number of voltage levels?

Suppose the proposed topology consists of a series of k MLMs and each of them consists of n_i capacitors (i = 1, 2, . . . , k). Thus

$$N_{capacitor} = \sum_{i=1}^{k} n_i = n_1 + n_2 + \ldots\ldots\ldots n_k$$

Considering (4.1), the number of capacitors can be written as follows Using (4.3), the maximum number of voltage levels can be determined

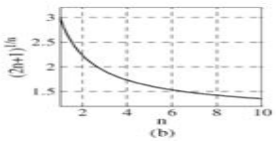

Fig (9) (2*n* + 1)1/*n* versus *n*

Fig. 9 shows the variation of (2n + 1)1/n versus n. It is clear that the maximum number of voltage levels is obtained for n = 1.

Thus, a structure consisting of MLMs with one capacitor (dc voltage source) can provide maximum voltage levels for v_o with minimum numbers of capacitors. It is necessary to note that the proposed topology is converted in this case to the conventional cascaded multilevel converter.

4.2.3. Minimum Number of IGBTs with Constant Number of Voltage Levels:

In this section, the question is that if N_{level} is the number of voltage levels considered for the voltage v_o, which topology with a minimum number of IGBTs can produce it?

It can be proven that the maximum number of voltage levels may be obtained for equal bidirectional switches. Thus, if the number of switches in each MLM is assumed to be equal to n, then the total numbers of IGBTs (N_{IGBT}) can be obtained

$$N_{IGBT} = (2n+4)k = l\times$$

Since N_{level} is constant, N_{IGBT} will be minimized, when (2n + 4)/ ln (2n + 1) tends to be minimum. Fig. 4.4 shows that the minimum number of IGBTs to realize Nlevel values for the output voltage is possible for n = 2.

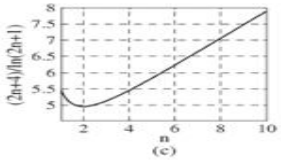

Fig (10) (2*n* +4)/ ln(2*n* + 1) versus *n*

. Minimum Number of Gate Driver Circuits with Constant Number of Voltage Levels:

In the proposed topology, each bidirectional switch is composed of two IGBTs and two anti-parallel diodes. Also, each unidirectional switch used in full-bridge converter is composed of an IGBT and an anti-parallel diode. Each bidirectional and unidirectional switch in the converter requires an isolated driver circuit. The isolation can be provided using either pulse transformers or optoisolators. The optoisolators can work in a wide range of input signal pulse widths, but a separate isolated power supply is required for each switching device.

The voltage and current ratings of switches in a multilevel converter play important role in the cost and realization of multilevel converters. In all topologies, currents of all switches are equal to the rated current of the load. But, this is not the case for the voltage. The objective is to determine the topology with the minimum blocking voltage, which can provide constant number of voltage levels v_o.

Suppose that the peak value of the blocking voltage of switches (V_{switch}) is represented by the following equation:

$$V_{switch,M} = V_{switch,M} + V_{switch,B}$$

$$= \sum_{i=1}^{k} V_{switch,m,j} + \sum_{i=1}^{k} V_{switch,b,j}$$

In this equation, Vswitch, M and Vswitch, B are the peak value of the blocking voltage of the bidirectional and unidirectional switches, respectively. Also, Vswitch, m, j and Vswitch, b, j represent the peak value of the blocking voltage of bidirectional switches in the j^{th} MLM and unidirectional switches in the j^{th} full-bridge converter, respectively. Therefore, (4.11) can be considered as a criterion to compare different topologies from the viewpoint of the maximum voltage on the switches. The lower value of the criterion indicates that a smaller voltage is applied to the terminal of the

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switches.

$$V_{switch,m,j} = P \times V_{j,\quad j}$$

LOSSES IN PROPOSED TOPOLOGY:

The total losses of switches are the conduction and switching losses. The blocking state losses have been neglected, because they are much smaller than the conduction losses.

Calculation of Conduction Losses:

The conduction losses are the losses that occur while the power device is in the on-state and conducting current. Therefore, power dissipation during the conduction is computed by multiplying the on-state voltage drop by the current that flows through device i.e.

$$p(t) = V_{on}(t).I(t)$$

Where, Von is the on-state saturation voltage and I is the power device current. The saturation voltage is a function of the junction temperature and the current flowing through the device. The saturation voltage of a bidirectional switch, shown in Fig., is the sum of saturation voltage of a diode, approximated by a linear function, and an IGBT, obtained from the manufacturers.

Therefore, we have

$$V_{on} = V_{on,IGBT} + V_{on,Diode}$$

At a particular temperature, the semiconductor specifications can be used to approximate semiconductor losses.

Calculation of Switching Losses:

The switching losses are the power dissipation during turn on and turn-off switching transitions. These losses are due to the imperfect switching of devices.

1) Turn-Off Losses: To calculate the turn-off losses, consider a bidirectional switch as shown in Fig. 11 Before turning off, this switch carries the output current *I*. At the end of this period, the output current is carried by *n* snubber circuits of the MLM and therefore, the voltage across this switch, is *IR/n*, since the snubber capacitor was initially discharged. Assuming that the device current changes linearly during turn-off period, the switching waveforms shown in Fig. 4.8 can be used.

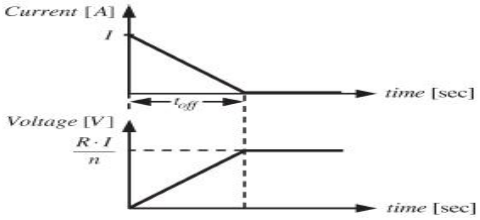


Fig (11). Current and voltage waveforms of device during turn-off period.

2) Turn-On Losses: Before the turn on, the output current is flowing through n snubber circuits in parallel and the snubber capacitor associated with this switch is charged to (V_{dc} +ΔV_C), where V_{dc} is the dc voltage of the MLM. Therefore, the switch voltage is the sum of the capacitor voltage (V_{dc} +ΔV_C) and the voltage drop across the snubber resistor, RI/n. At the end of the turn-on period, the sum of the load current (I) and the peak snubber discharge current (n (V_{dc} +ΔV_C)/R) flow through the switch. Assuming again that the device current changes is linear during turn-on period, and then the waveforms shown in Fig. 11 can be used. The energy losses are calculated in this switch during the turn-on period, as follows:

$$E_{on} = \left(V_{dc} + \Delta V_C + \frac{RI}{n}\right)\left(I + \frac{n(V_{dc} + \Delta V_C)}{R}\right)\frac{t_{on}}{6}$$

Where, ton is the rise time of the IGBT device and ΔVC is equal to Iτ/nC. C is the snubber capacitor and τ is the delay time considered among drive signals of IGBTs to provide the safe commutation of switches.

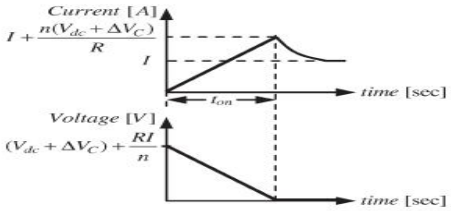


Fig (12) Current and voltage waveforms of device during turn-on period.

the total turn-on losses of the proposed topology are the sum of MLMs and H-bridges turn-on losses, i.e.

$$P_{on} = P_{on\,M} + P_{on\,H}$$

Now, the total switching losses can be calculated as follows:

$$P_{sw} = P_{on} + P_{off}$$

COMPARISON OF PROPOSED TOPOLOGY WITH PREVIOUS TOPOLOGY

To compare with existing topologies, the number of bidirectional switches of MLMs in the proposed topology and blocks in the topology presented in previous have been considered to be equal to two and three, respectively. Therefore, the maximum number of voltage levels will be produced. The proposed topology has an asymmetrical converter, then, the results are compared with the well-known asymmetrical cascaded multilevel converter. The most common type has dc voltage sources that scaled by the factor of three, hereafter called trinary configuration.

The trinary configuration provides the maximum number of voltage levels with constant number of IGBTs.

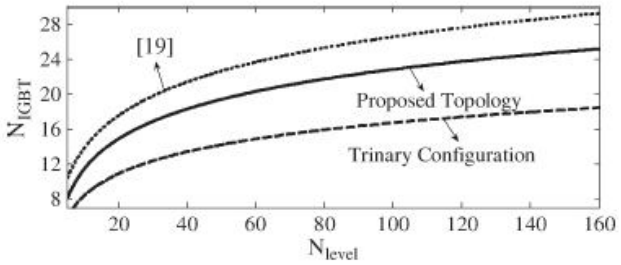
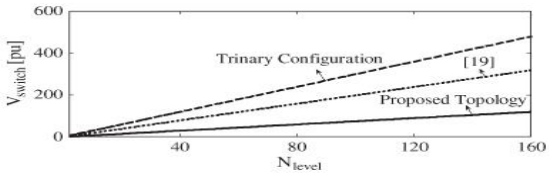


Fig (13) Required number of IGBTs to realize N_{level} voltages in different topologies



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Fig(14) Blocking voltages on bidirectional switches to realize N_{level}voltagelevels

The maximum blocking voltage of switches in the proposed topology, topology presented in previous and trinary configuration are shown in Fig.4.12 In the optimized proposed

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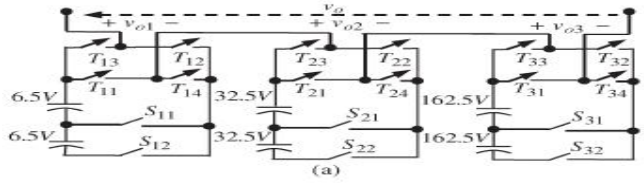
topology, the MLMs have two bidirectional switches. So, the maximum blocking voltage is related to S_{k2} and equal to $2 \times 5k-1$ (i.e., $N_{level}/2.5$). This figure shows that this voltage is less than the equivalent voltage of previous topology and has a minor difference with trinary configuration. The major demerit of these topologies is the increase of the stress with increasing the number of levels.

DESIGN OF MULTILEVEL CONVERTER BASED ON PROPOSED TOPOLOGY:

In this section, a typical single-phase multilevel converter with a minimum of 120 voltage levels and a peak value of 400V should be designed. The on-state voltage drops of the switches have been neglected. The optimal multilevel structure is presented in Fig. 4.16 for the minimum number of used switches. As shown in this figure, the number of IGBTs and capacitors are 24 and 6, respectively. In this design, the number of voltage levels is 125. The optimal structure based on the minimum number of capacitors is similar to Fig. 15



Fig(15) multilevel structure with minimum used switches

The structure of optimal multilevel with minimum used switches based on the recommended topology of previous is presented .

RESULTS

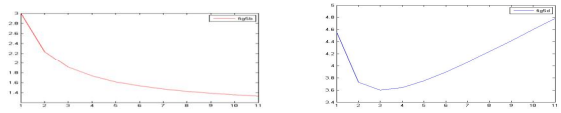


Fig 16.Minimum Number of IGBTs with Constant Number of Voltage Levels

Fig 17Minimum Number of Gate Driver Circuits with Constant Number of Voltage Levels

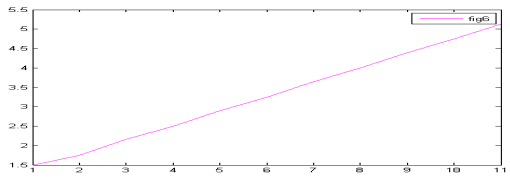


Fig 18Minimum Blocking Voltage of Switches with Constant Number of Voltage Levels

CONCLUSION AND FUTURE SCOPE

A new basic multilevel module (MLM) for the multilevel converter has been proposed. The proposed topology is a combination of MLMs and full-bridges converter. It extends the design flexibility and the possibilities to optimize the converter for various objectives. It has been shown that the structure, consisting of MLMs with two switches has the minimum number of switches for a given number of voltage levels. It has been shown that the proposed topology provides 125 levels on the output voltage with a peak of 400 V, using 24 IGBTs and the blocking voltage of 604.5 V on bidirectional switches. But, the other topology produces 161 voltage levels using 28 IGBTs and a blocking voltage of 1000 V. The operation and performance of the proposed topology has been experimentally verified on a single-phase 125-level multilevel converter prototype. The proposed topology can be a good solution for applications that require high power quality, or applications that have considerable numbers of dc voltage sources.

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