

Design of Efficient Hardware Utilization Fault Coverage Circuit



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Abstract—A new fault coverage test pattern generator using a linear feedback shift register (LFSR) called FC-LFSR can perform fault analysis and reduce the power of a circuit during test by generating three intermediate patterns between the random patterns by reducing the hardware utilization. The goal of having intermediate patterns is to reduce the transitional activities of Primary Inputs (PI) which eventually reduces the switching activities inside the Circuit under Test (CUT) and hence power consumption is also reduced without any penalty in the hardware resources. The experimental results for c17 benchmark, with and without fault confirm the fault coverage of the circuit being tested.

Keywords- LFSR, Optimization, Low Power, Test Pattern Generation, BIST

I. INTRODUCTION

The main challenging areas in VLSI are performance, cost, power dissipation is due to switching i.e. the power consumed testing, due to short circuit current flow and charging of load area, reliability and power. The demand for portable computing devices and communications system are increasing rapidly. The applications require low power dissipation VLSI circuits. The power dissipation during test mode is 200% more than in normal mode. Hence the important aspect to optimize power during testing [1].

Power dissipation is a challenging problem for today's System-on-Chips (SoCs) design and test. The power dissipation in CMOS technology is either static or dynamic. Static power dissipation is primarily due to the leakage currents and contribution to the total power dissipation is very small. The dominant factor in the power dissipation is the dynamic power which is consumed when the circuit nodes switch from 0 to 1. During switching, the power is consumed due to the short circuit current flow and the charging of load capacitances is given by equation:

$$P = 0.5V_{DD}^2 E (sw) C_L F_{CLK} \quad (1)$$

Where V_{DD} is supply voltage, $E (sw)$ is the average number of output transitions per $1/F_{CLK}$, F_{CLK} is the clock

frequency and C_L is the physical capacitance at the output of the gate. Dynamic power dissipation contributed to total power dissipation. From the equation dynamic power depends on three parameters: supply voltage, clock frequency and switching activity. To reduce the dynamic

power dissipation by using first two parameters only at the expense of circuit performance. But power reduction using the switching activity doesn't degrade the performance of the circuit. Power dissipation during testing is one of most important issue.

Latest advances in semiconductor technology have led to transistor scaling of transistor dimensions, allowing a large number of devices to be fabricated on a single chip. The high integration has made power consumption. In addition, the ever increasing utilization of portable computing devices and communication systems requires low power dissipation in VLSI circuits [1].

The power dissipation of a system in test mode is more than in normal mode. Low correlation between consecutive test vectors (e.g. among pseudorandom patterns) increases switching activity and eventually power dissipation in the circuit. The same happens when applying low correlated patterns to scan chains. Increasing switching activity in scan chain results in increasing power consumption in scan chain and combinational block. The extra power (average or peak) can cause problems such as instantaneous power surge causes circuit damage, formation of hot spots, difficulty in performance verification and reduction of the product yield and lifetime [2].

Large and complex chips require a huge amount of test data and dissipate a significant amount of power during test, which greatly increases the system cost. There are many test parameters should be improved in order to reduce the test cost. Parameters include the test power, test length (test application time), test fault coverage, and test hardware area overhead

Automatic test equipment (ATE) is the instrumentation used in external testing to apply test patterns to the CUT, to analyze the responses from the CUT, and to mark the CUT as good or bad according to the analyzed responses. External testing using ATE has a serious disadvantage, since the ATE (control unit and memory) is extremely expensive and cost is expected to grow in the future as the number of chip pins increases. As the complexity of modern chips increases, external testing with ATE becomes extremely expensive. Instead, Built-In Self-Test (BIST) is becoming more common in the testing of digital VLSI circuits since overcomes the problems of external testing using ATE. BIST test patterns are not generated externally as in case of ATE.

BIST perform self-testing and reducing dependence on an external ATE. BIST is a Design-for-Testability (DFT) technique makes the electrical testing of a chip easier, faster,

more efficient and less costly. The important to choose the proper LFSR architecture for achieving appropriate fault coverage and consume less power. Every architecture consumes different power for same polynomial.

Applications of LFSR: Pattern generator, Low power testing, Data compression, and Pseudo Random Bit Sequences (PRBS).

II. LOW POWER TESTING SCHEMES

Various authors reported on techniques to cope with power problems during testing. Existing low-power testing scheme is divided into the following two categories.

- (A) Low - Power Testing Techniques for External Testing
- (B) Low - Power Testing Techniques for Internal Testing

A. Low-Power Testing Techniques for External Testing

The category contains various techniques adopted to reduce the power consumption during external testing by ATE and depends on the number of transitions in test data set. Reference [3] proposed a heuristic method to generate test sequences which create worst-case power droop by accumulating the high- and low-frequency effects using a dynamically constrained version of the classical D-algorithm for test generation. A novel scan chain division algorithm [4] analyzes the signal dependencies and creates the circuit partitions such that both shift and capture power can be reduced when using the existing ATPG flows. Reference [5] presents a low capture power ATPG and a power-aware test compaction method. This ATPG lowers the growth of test pattern count compared to the detection number . The peak power becomes smaller as the detection number increases. The test compaction algorithm further reduces the number of test patterns as well as the average capture power.

The idea is to identify an input control pattern such that, by applying that pattern to the primary inputs of the circuit during the scan operation, the switching activity in the combinational part can be minimized or even eliminated. The basic idea of input control technique with existing vector- or latch-ordering techniques that reduces the power consumption has been covered in [6]. In the same area, [7] presented a technique of gating partial set of scan cells. The subset of scan cells is selected to give maximum reduction in test power within a given area constraint. An alternate formulation of the problem is to treat maximum permitted test power and area overhead as constraints and achieve a test power that is within these limits using the fewest number of gated scan cells, thereby leading to least impact in area overhead. The area overhead is predictable and closely corresponds to the average power reduction.

The researches have widely explored the test vector reordering techniques to reduce the switching power. Hamming distance based reordering is described in survey paper [6].

Sankaralingam et al. Vector compaction and data compression based on a static compaction technique to minimize the scan vector power dissipation. Carefully selecting the merging order of test cube pairs during static compaction reduces both average and peak power for the final test set. The technique is more effective than conventional static compaction techniques that randomly merge test cubes. Chandra and Chakrabarty propose a

novel technique using test data compression for testing that reduces both test data volume and scan power dissipation [6].

B. Low-Power Testing Techniques for Internal Testing

Various authors reported on techniques to cope with power problems during BIST. Several techniques have been reported to address the low power BIST. The technique proposed in [8] consists of a distributed BIST control scheme that simplifies BIST architecture for complex ICs, especially during higher levels of test activity. The approach can schedule the execution of every BIST element to keep the power dissipation under specified limits. The technique reduces average power and avoids temperature-related problems but increase in test time. A BIST strategy called dual-speed LFSR is proposed in [9] to reduce the circuit's overall switching activities. The technique uses two different-speed LFSRs to control those inputs that have elevated transition densities. The low power test pattern generator presented in [10] is based on cellular automata, reduces the test power in combinational circuits while attaining high fault coverage. Test time and area overhead remain unaffected. Another low-power test pattern generator based on a modified LFSR is proposed in [11]. The scheme reduces the power in CUT in general and clock tree in particular.

Gizopoulos et al. consider the problem of low-power BIST for data path architecture built around multiplier-accumulator pairs. The method proposes two alternative architectures depend on low energy or low power dissipation. The authors based on both modified binary counters, operating as Gray counters, generate only one transition at a time. These architectures can achieve important energy and average power savings compared to conventional pseudorandom BIST [6]. The drawback of these techniques is circuit-dependent, implying that non-detecting subsequences must be determined for each circuit test sequence. Other authors propose two other low-power approaches for scan-based BIST. Zhang, Roy, and Bhawmik propose modifying the LFSR by adding weight sets to tune the pseudorandom vector's signal probabilities and thereby decrease energy consumption and increase fault coverage[6].

A low-power random pattern generation technique to reduce signal activities in the scan chain is proposed in [12]. In this technique, an LFSR generates equally probable random patterns. The technique generates random but highly correlated neighboring bits in the scan chain, reducing the number of transitions and, thus, the average power. Girard et al. address the problem of energy minimization during test application for BIST enabled circuits. The main constraint is reducing energy consumption without modifying the stuck-at fault coverage. In this work, the authors first analyze the impact of an LFSR's polynomial and seed selection on the circuit's switching activity during test application. They determine that the polynomial selection does not influence energy consumption; the LFSR's seed selection is a more important parameter. Therefore, the authors propose a method based on a simulated- annealing algorithm to select

an LFSR's seed and provide the lowest energy consumption. Test vector inhibiting techniques to filter out some non-detecting subsequences of a pseudorandom test set generated by an LFSR. The architectures apply the minimum number of test vectors required to attain the desired fault coverage and therefore reduce power [6].

Many low-power strategies have been proposed for full scan and scan-based BIST architecture. The architecture proposed in modifies the scan-path structure such that CUT inputs remain unchanged during a shift operation. A test pattern generator for scan-based BIST was proposed in [13] that reduce the number of transitions that occur at scan inputs during scan shift operation. Authors in [14] proposed a pseudorandom BIST scheme to reduce the switching activity in the scan chains. The activity and correlation in CUT is controlled by limiting the scan shifts to a portion of the scan chain structure using scan chain disable control.

III. PATTERN GENERATOR

The BIST contains two major components: test pattern generator and response checker. Both of these components use Linear Feedback Shift Register (LFSR). The paper described the three different pattern generation techniques by using LFSR can be designed to reduce the power consumption during test in the following ways.

A. Generating Test Vectors by using Modified Clock Scheme.

Girard et al. proposed the low-power test pattern generator (TPG) based on modified clock scheme. The low-power BIST technique relies on a gated clock scheme for the pseudo-random test pattern generator and the clock tree feeding the TPG. An n -bit LFSR is divided into two $n/2$ -bit LFSRs. Basically, a clock whose speed is half of the normal speed is used to activate one half of the D flip-flops in the TPG (i.e. a modified LFSR) during one clock cycle. During the next clock cycle, the second half of the D flip-flops is activated by another clock whose speed is also half of the normal speed. The two clocks are synchronous with a master clock CLK and have the same but shifted in time period. The clock CLK is the clock of the circuit in the normal mode and has a period equal to T [11].

As one can observe, a test vector is applied to the CUT at each clock cycle of the test session, only one half of the circuit inputs can be activated during the time. Consequently, the average powers as well as the peak power consumed in the CUT are minimized. Moreover, the power consumed in the TPG is also minimized since only one half of the D flip-flops in the TPG can be activated in a given time interval.

Another important feature is the total energy consumption during BIST is reduced, since the test length produced by the modified LFSR is roughly the same than the produced by a conventional LFSR to reach the same or sometimes a better fault coverage. The scheme reduces test power in the CUT, generator, and clock tree. The technique achieves important test power savings with no penalty to circuit performance, fault coverage, test time, or design time.

The drawback of the technique is to reduce the randomness property of the LFSR also requires two non-

overlapping clocks with half frequency and increases the area overhead.

B. Generating Test Vectors by using LPATPG

Zhang X proposed a Low Power Automatic Test Pattern Generator (LPATPG) with peak power reduction [15]. The authors used two n -bit random pattern generators and $n(2 \times 1)$ multiplexers but only add one flip flop to an n -bit LFSR, therefore the area overhead of bipartite LFSR is much lower than LPATPG.

C. Generating Test Vectors by using LT-LFSR

Mohammad Tehranipoor proposed a low-transition LFSR by combining techniques of random pattern generation called R-Injection (RI) and Bipartite LFSR for low-power BIST. The new LT-LFSR generates three intermediate patterns [16]. The RI method inserts a new intermediate pattern between two consecutive test patterns by positioning a random-bit (R) in the corresponding bit of the intermediate pattern when there is a transition between corresponding bits of pattern pairs. The bipartite LFSR generates an intermediate pattern using one half of each of the two consecutive random patterns.

The goal is to design a new random pattern generator reduces the total number of transitions among the adjacent bits in each random pattern (horizontal dimension) and transitions between two consecutive random patterns (vertical dimension) as well. In other words, the new low transition random pattern generator increases the correlation between and within patterns [12].

The main advantage of the technique can be used for both combinational and sequential circuits and the randomness quality of patterns does not deteriorate. The authors also use a k -input AND gate and T-latch to generate a high correlation between neighboring bits in the scan chain, reducing the number of transitions and the average power.

IV. BIST ARCHITECTURE

BIST, is the technique of designing additional hardware and software features into integrated circuits to allow them to perform self-testing, i.e., testing of their own operation (functionally, parametrically, or both) using their own circuits, thereby reducing dependence on an external ATE.

A. Implementation of BIST

A typical BIST architecture consists of Test Pattern Generator (TPG) usually implemented as a LFSR, Test Response Analyzer (TRA), Multiple Input Signature Register (MISR), CUT and BIST control unit as shown in figure 1.

CUT: It is the portion of the circuit tested in BIST mode. It can be sequential, combinational or a memory. Their Primary Input (PI) and Primary output (PO) delimit it.

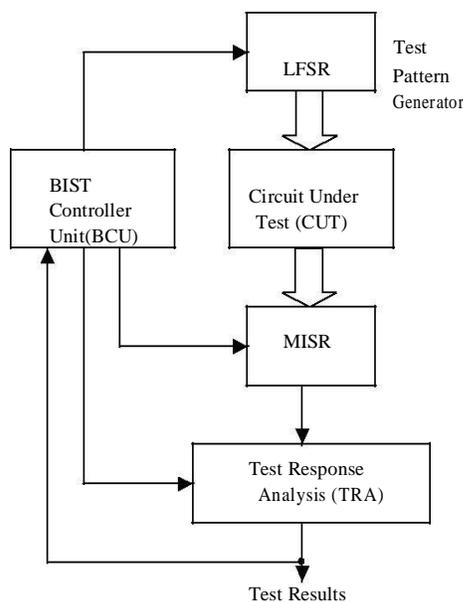


Figure 1. BIST Architecture.

TPG: It generates the test patterns for the CUT. It is dedicated circuit or a microprocessor. The patterns may be generated in pseudorandom or deterministically.

MISR: It is designed for signature analysis, which is a technique for data compression. MISR efficiently map different input streams to different signatures with every small probability of alias.

TRA: It will check the output of MISR & verify with the input of LFSR & give the result as error or not.

BIST Control Unit: Control unit is used to control all the operations. Mainly control unit will do configuration of CUT in test mode/Normal mode, feed seed value to LFSR, Control MISR & TRA. It will generate interrupt if an error occurs.

In BIST, LFSR generates pseudorandom test patterns for primary inputs (PIs) or scan chains input. MISR compacts test responses received from primary output or scan chains output. Test vectors applied to a CUT at nominal operating frequency, often cause more average and/or peak power dissipation than in normal mode. The result in more switching's and power dissipation in test mode.

B. Implementation of low transition test pattern

The basic idea behind low power BIST is to reduce the PI activities. The paper proposes a new transition test pattern generation technique which generates three intermediate test patterns between each two consecutive random patterns generated by a conventional LFSR. The proposed test pattern generation method does not decrease the random nature of the test patterns. The technique reduces the PI's activities and eventually switching activities in the circuit under test. Let us assume that T_i and T_{i+1} are two consecutive test patterns generated by a pseudorandom pattern generator (e.g. a conventional LFSR). The new low transition LFSR (LT-LFSR) generates three intermediate patterns (T_{i1} , T_{i2} and T_{i3}) between T_i and T_{i+1} . The total number of signal transition

occurs between these five vectors are equivalent to the number of transition occurs between the two vectors. Hence the power consumption is reduced. Additional circuit is used for few logic gates in order to generate three intermediate vectors. The area overhead of the additional components to the LFSR is negligible compared to the large circuit sizes.

The three intermediate vectors (T_{i1} , T_{i2} and T_{i3}) are achieved by modifying conventional flip-flops outputs and low power outputs [16].

C. Implementing algorithm for LT-LFSR

The proposed approach consists of two half circuits. The algorithm steps says the functions of both half circuits is Step1: First half is active and second half is idle and gives out

is previous, the generating test vector is T_{i1} .

Step2: Both halves are idle First half sent to the output and second halves output is sent by the injection circuit, the

generating test vector is T_{i1} .

Step3: Second half is active First half is in idle mode and

gives out as previous, the generating test vector is T_{i2} .

Step4: Both halves are in idle mode, First half is given by injection circuit and Second half is same as previous, the generating

test vector is T_{i3} .

After completing step 4 again goes to step1 for generating test vector T_{i+1} .

The first level of hierarchy from top to down includes logic circuit design for propagation either the present or next state of flip-flop to second level of hierarchy. Second level of hierarchy is implementing Multiplexed (MUX) function i.e. selecting two states to propagate to output which provides more power reduction compared to having only one of the R-Injection and Bipartite LFSR techniques in a LFSR due to high randomness of the inserted patterns.

V. RESULTS AND DISCUSSION

The power consumed by the chip under test is a measure of the switching activity of the logic inside the chip which depends largely on the randomness of the applied input stimulus. The existing technologies reduced correlation between the successive vectors of the applied stimulus into the CUT can result in much higher power consumption by the device. The increased power may be responsible for cost, reliability, performance verification, autonomy and technology related problems. The proposed approach is a new low power pattern generation technique is implemented using a modified conventional LFSR.

The comparison of experimental results for both ISCAS'85 (combinational) and ISCAS'89 (sequential) benchmarks given in tables.

Comparisons of the number of test patterns (N_p) required to hit target fault coverage (FC), the average and peak power of LT-LFSR, LPATPG and modified clock scheme are shown in Table-1 [16], [15], [11]. The used 50 different seeds for 10 different polynomials in the experiment. The performance of LT-LFSR is seed and polynomial-independent. The required number of patterns provides target FC does not quadruples, and preserving randomness.

Device Utilization Summary

Logic Utilization	Used	Available
Number of Slice Flip Flops	251	3,840
Number of 4 input LUTs	12	3,840
Logic Distribution		
Number of occupied Slices	45	1,920
Number of Slices containing only related logic	45	21
Number of Slices containing unrelated logic	0	21
Total Number of 4 input LUTs	12	3,840
Number of bonded IOBs	64	173
Number of GCLKs	1	8
Total equivalent gate count for design	562	
Additional JTAG gate count for IOBs	2,934	

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VI. CONCLUSIONS

The paper proposed an optimization procedure for Test Pattern Generation (TPG) technique with reducing power dissipation during testing along with fault coverage. The transition is reduced by increasing the correlation between the successive bits, reduces the power of a circuit during the test mode. By increasing the correlation between the test patterns in the CUT and eventually the power consumption is reduced. The circuit is tested during the presence of fault and without fault for fault coverage and the power consumed during testing is 14mw.

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