ISSN 2278-3091

International Journal of Advanced Trends in Computer Science and Engineering, Vol. 3 , No.1, Pages : 101– 104 (2014)
Special Issue of ICETETS 2014 - Held on 24-25 February, 2014 in Malla Reddy Institute of Engineering and Technology, Secunderabad– 14, AP, India

A CUSTOMIZED APPROACH FOR IDENTIFICATION OF FAULTY STATES IN VLSI CIRCUITS

SK.NAGUL MEERA[1] [1]*email: nagulmeera987@gmail.com*

A.NARESH [2] [2]*email: nari.432@gmail.com*

CH RAMA KOTI REDDY [3] [3]*email: rkr293@gmail.com*

Abstract

The FPGA BRAM testing is a separate testing procedure followed in VLSI technology. There are several test circuits available for testing the memory chips. However no test setup is developed so far for testing the memory blocks inside the FPGA. The BRAM blocks of FPGA are designed to work at much higher frequency than the FPGA core logic. Hence testing the BRAMs at higher speed is essential. The conventional memory test circuits cannot be used for this purpose. Hence the proposed work develops a memory testing tool based on March tests for FPGA based BRAM (block RAM testing).

Key words: march test, BRAM blocks, fault detection

1.INTRODUCTION

The memory testing procedure involves writing a specific sequence of bits into the memory locations and reading them again. This type of tests usually known as march tests. If all the values read back are same as those that were written then the memory device is said to pass the test otherwise device fails The main fault models have been developed in modern technologies are stuck-at faults, bridging faults models and some algorithms classically employed for test vector generation are D-Algorithm, PODEM,ATPG etc

Memory testing strongly differs from the test of conventional ASICs. In this paper, we present a versatile memory testing framework consisting of an SRAM memory test bench which is flexible and programmable. This test bench allows not only to employ different commercial SRAM memories allows but also to apply various algorithms for testing.

Conventional fault models are not sufficient to represent all important failure modes in a BRAM; Functional Fault models should be employed. Memory Fault models can be classified under the categories shown below, brief descriptions of the models are given as follows.

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II.TEST GENERATOR

Memory testing may be considered as a full disciplinary subject. Commonly, test sequences or test algorithms for memories are known under the name of March tests. Every March test has specific capabilities that allow revealing the typical defects of memories. A typical active test bench has to allow not only the implementation of March tests existing in the literature but also the creating of new test algorithms. A March test consists of a sequence of March elements. A March element has a certain number of operations (or March primitive) that must be applied to all memory cells of an array. Thus, ↑(r0;w1) is a March element and r0 and w1 are March primitives. The addressing order of a March element can be done in an up (↑), down (↓) way or (↕) if the order is not significant. A March primitive can be a write 1(w1), write 0 (w0), read 1(r1) and read 0 (r0) that can be performed in a memory cell.

Here, we introduce, for example, the March C- : {↑(w0);↑(r0,w1);↑(r1,w0);↓(r0,w1);↓(r1,w0);↑(r0}
This well-known March test allows to detect all the stuck @ and transition fault of a memory cell array, as well as all address decoder faults and coupling (interaction between two cells) faults.

1. Stuck-at fault (SAF): cell or line s-a-0 or s-a-1
2. Stuck-open fault (SOF): open cell or broken line.
3. Transition fault (TF): cell fails to transit
4. Data retention fault (DRF)

There are various fault models to test the functional faults stuck at faults; coupling faults are considered when it deals with SRAM. Address decoder faults and bridging faults will be considered when it deals with DRAM. Hence the most possible faults which occur in general are stuck at faults.

Stuck at fault (SAF) :The stuck-at fault (SAF) considers that the logic value of a cell or line is always 0 (stuck-at 0 or SA0) or always 1 (stuck-at 1 or SA1). To detect and locate all stuck-at faults, a test must satisfy the

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following requirement: from each cell, a 0 and a 1 must be read.

Transition Faults (TF): The transition fault (TF) is a special case of the SAF. A cell or line that fails to undergo a 0 to 1 transition after a write operation is said to contain an up transition fault. Similarly, a down transition fault indicates the failure of making 1 to 0 transitions.

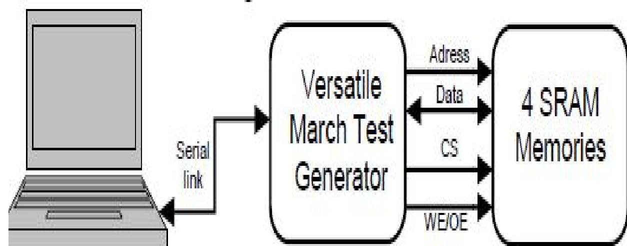

Fig 1 : Test bench architecture

An user interface allows users to choose or set a specific March test of the literature (March A, March C-, Matt, Matt +) or introduce a new one (Custom). The chosen March test is uploaded through the serial connection to the programmable test generator and then applied to each memory on the setup.

If no fault is detected, the programmable generator returns a positive acknowledgement on the four memories. Whether the opposite case occurs, i.e. when a reading operation (r0 or failing march element and operation. Only the knowledge of this information allows the identification of physical defects

III. LABORATORY ANALYSYS

Fig. 2 depicts the test bench (with four memories under the test bench to a computer. The four memories are tested in sequence (not simultaneously) following a scheduling that is fixed by the user.

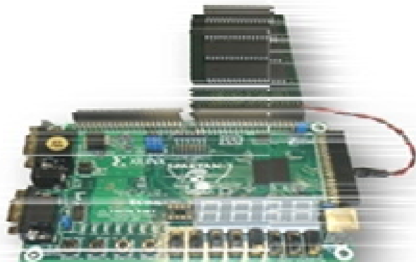

FIG2:Experimental FPGA Kit

One or more than one memory can be replaced by using a memory emulator.in which we can introduce any kind of fault model such as stuck-at, transition, address decoder, coupling faults etc.

The following are the possible march sequences shown in figure 3.

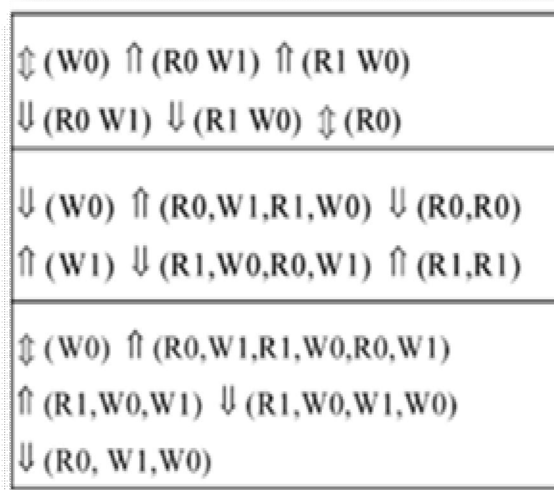

Fig 3: March test sequences

IV. ADVANTAGES OF TEST BENCH

The simulation results can be shown with the CAD tools. The users can take any of the following three possible march sequences the first test is more efficient and has high fault coverage.it has six elements with all possible logic primitives .

The generation and refinement of this framework will provide a test bench architecture for detecting stuck - at and transition faults more effectively with march tests. The test bench setup can be extended for different types of fault detections.

In all cases we clearly understood the way that March C and other Test sequence applied to memories as well as the sensitization and observation processes of the various fault models This type of tests will have excellent fault detection coverage and operates at higher frequencies.

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V.SIMULATION RESULTS

The experimental results with state identification and possible fault models for the test 1are shown in the figures 4 and 5 respectively.

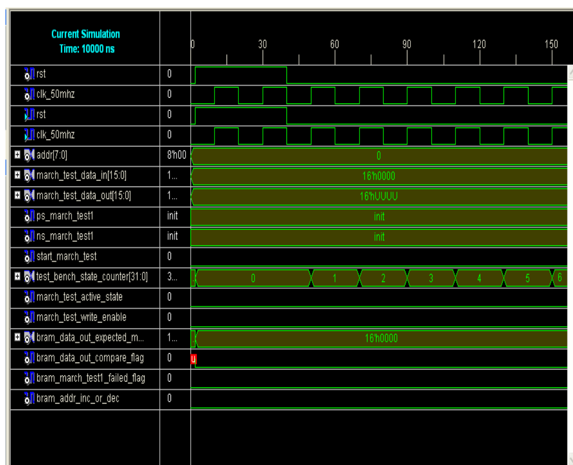

Fig4:simulation result for test 1

State id where error occurred	Possible faults
1	Unknown fault
2	SA1 or CFst<0;1>
3	SA0 or TF<↑/0> or CFid<↑;0> or CFst<1;0>
4	SA1 or TF<↓/1> or CFid<↓;1> or CFst<0;1>
5	SA0 or TF<↑/0> or CFid<↑;0> or CFst<1;0>
6	SA1 or TF<↓/1> or CFid<↓;1> or CFst<0;1>
7	Unknown fault
8	Unknown fault

Fig 5: possible faults for test 1

The results with state identification and possible fault models for the test 2 are shown in the figures5.

VI. APPLICATIONS AND ADVANTAGES

Advantages

1. Efficient fault detection
2. Reliable fault simulation
3. Easy to generate test patterns
4. Flexible to operate at higher frequencies
5. Low time complexity

Applications:

1. Used for testing complex memory circuits in FPGA devices
2. Used for generating complex test patterns for FPGA memory testing applications

The results with state identification and possible fault models for the test 2 are similar to that of test 1 ate not shown here.

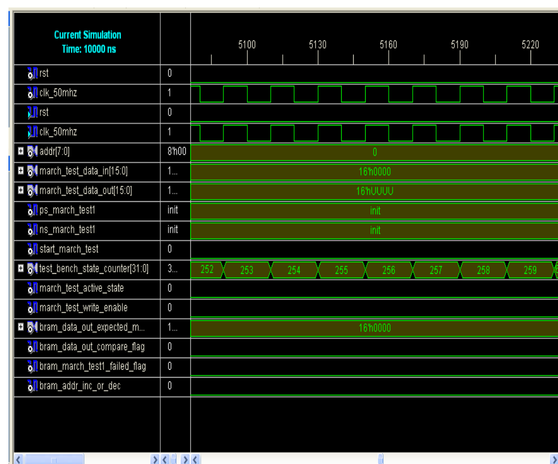

Fig6: simulation result for test 2

VII.CONCLUSION

The code modules for test generator shall be developed in VHDL and shall be synthesized for Xilinx Spartan Family device. A pc based GUI tool shall send command to FPGA using serial port for selecting the type of test. The FPGA core gets the command through UART and performs the appropriate and sends the test report back to PC. The result shall be verified in simulation with Xilinx ISE simulator and also in hardware by using Chipscope. Xilinx Spartan family FPGA board shall be used for hardware verification of the developed March test generator.

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AUTHORS

SK NAGUL MEERA received M.tech degree from JNTUH, in vlsi system design, presently working as an assistant professor in malla reddy institute of engineering &technology (MRIET), Hyderabad..

A.NARESH, received M.tech degree from Hindustan University, Chennai, presently working as an assistant professor in malla reddy institute of engineering &technology (MRIET), Hyderabad.

CH.RAM KOTI REDDY received M.tech degree from JNTUA, in Embedded systems, presently working as an assistant professor in malla reddy institute of engineering &technology (MRIET), Hyderabad..