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Performance Analysis of Switched Capacitor Three Phase Symmetrical Inverter Topology with Induction Drive

KATURI MAHESH
M-tech Student Scholar
Department of Electrical & Electronics Engineering,
Malla Reddy institute of Engineering & Technology,
A.P, India

P.VEERANJANEYULU
Associate Professor
Department of Electrical & Electronics Engineering,
Malla Reddy institute of Engineering & Technology,
A.P, India

***Abstract*— Using parallel-series converter in as DC Power supply appliance gives a good opportunity to maintain stable supply while the load is changing. A novel multilevel inverter with a small number of switching devices is proposed. It consists of an H-bridge and an inverter which outputs multilevel voltage by switching the dc voltage sources in series and in parallel. The proposed inverter can output more numbers of voltage levels in the same number of switching devices by using this conversion. The number of gate driving circuits is reduced, which leads to the reduction of the size and power consumption in the driving circuits. The total harmonic of the output waveform is also reduced. The proposed inverter outputs larger voltage than the input voltage by switching the capacitors in series and in parallel. The maximum output voltage is determined by the number of the capacitors. In this output side induction motor drive is applied, An induction motor's rotor can be either wound type or squirrel-cage type. Unlike traditional multilevel inverters, this topology does not require an external voltage balancing circuit, a complicated control scheme, or isolated dc sources to maintain its voltage levels while delivering sustained real power. In this paper, the circuit configuration, the theoretical operation, the simulation results with MATLAB/SIMULINK, results are shown.**

***Index Terms*— A boost converter, H-bridge, Switched capacitor converters, charge pump, switched-capacitor, Induction Machine Drive.**

I. INTRODUCTION

The conventional voltage source inverters produce an output voltage at the poles with levels +/-Vdc/2, where Vdc is the dc-link voltage, are known as the two-level inverter. To obtain a quality output voltage or a current waveform with a minimum amount of ripple content, they require high-switching frequency along with various pulse-width modulation (PWM) strategies [1]. In high-power and high-voltage applications, these two-level inverters however, have some limitations in operating at high frequency mainly due to switching losses and constraints of device ratings. Moreover, the semiconductor switching devices should be used in such a manner as to avoid problems associated with their series parallel combinations that are necessary to obtain capability of handling high-voltages and currents. The multi-level inverter includes an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages.

One of the issues raised in these studies is the limitation of switching devices [1]. If the devices which can sustain high voltage are used in the inverter, their switching frequency is restricted. On the other hand, when the rotation speed of the motor becomes high[3],[7],[9], the frequency of the reference waveforms also becomes high. When the frequency of the reference waveforms becomes close to the restricted switching frequency, the output waveform is distorted, and the reliability of the motor is reduced. As a provision against the problem [15], the device voltage must be reduced to use high-speed switching devices. The EVs and the grid connected DG systems need an inverter to convert dc to ac[9]. Boost converters or transformers are widely used in these systems when the input voltage is smaller than the output voltage. In this paper a novel boost switched-capacitor inverter is proposed. The circuit topology was introduced.

The modulation method, the determination method [11] of the capacitance, and the loss calculation of the inverter proposed. A charge pump outputs a larger voltage than the input voltage with switched capacitors [7], [8]. When the several capacitors and the input voltage sources are connected in parallel, the capacitors are charged. SC inverter is consists of a Marx inverter structure and an H-bridge [18]. The proposed inverter can output larger voltage than the input voltage by switching the capacitors in series and in parallel. The maximum output voltage is determined by the number of the capacitors.

The continuous economic development of many countries and the environmental issues (gas emissions and the green house effect) observed in the last decades forced an

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intense research in renewable energy sources. Hydro, photovoltaic (PV) and wind energy conversion are the most explored technologies due to their considerable advantages [1]-[2], such as reliability, reasonable installation and energy production costs, low environmental impact, capability to support micro-grid systems and to connect to the electric grid [3]. Among these energy sources the PV is pointed out as one of the most modular and environmentally friendly technologies. Therefore, PV systems have been frequently adopted worldwide, presenting a growth of 45% on the total PV power installed in 2009.

The proposed inverter does not have any inductors can be smaller than a conventional two-stage unit which consists of a boost converter and an inverter bridge, which make the system large. The structure of the inverter is simpler than [3] the conventional switched-capacitor inverters. THD of the output waveform of the inverter is reduced compared to the conventional single phase full bridge inverter as the conventional multilevel inverter. In this paper, an SC inverter whose structure is simpler than the conventional SC inverter is proposed. It consists of a Marx inverter structure and an H-bridge. The proposed inverter can output larger voltage than the input [3] voltage by switching the capacitors in series and in parallel. The proposed inverter does not have any inductors which make the system large [4]. The output harmonics of the proposed inverter are reduced by the multilevel output.

II. CIRCUIT DESCRIPTION

Fig. 1 shows a circuit topology of the proposed inverter, where *Sak*, *Sbk*, *Sck*(k = 1, 2, . . . , $2n$ − 2) are the switching devices which switch the capacitors *Ck*(k = 1, 2, . . . , $2n$ − 1) in series and in parallel. Switches $S1$ − $S4$ are in the inverter bridge.

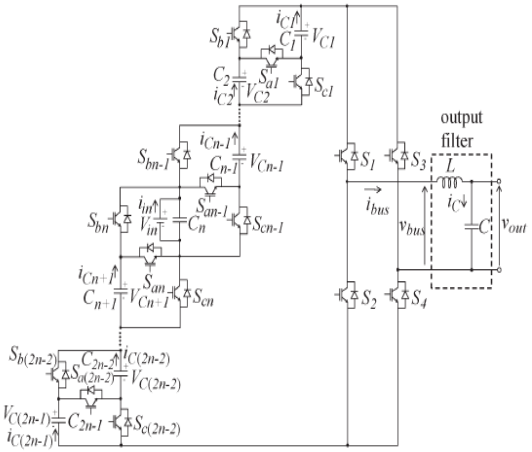
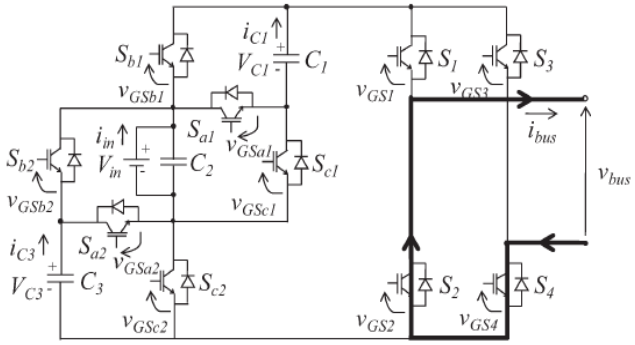
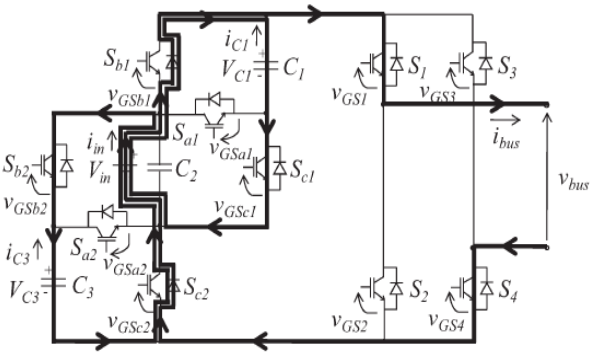


Fig.1. Circuit topology of the switched-capacitor inverter using series/parallel conversion

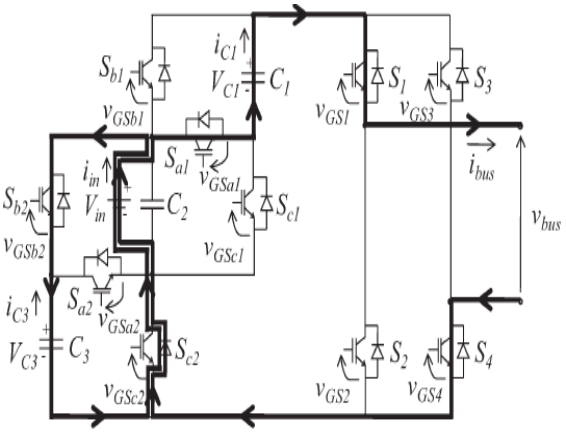
A voltage source *Vin* is the input voltage source. A lowpass filter is composed of an inductor *L* and a capacitor *C*. There are many modulation methods to drive a multilevel inverter: the space vector modulation the multicarrier pulse width modulation (PWM) the hybrid modulation the selective harmonic elimination and the nearest level control In this paper, the multicarrier PWM method is applied to the proposed inverter.



(a) The current i_{bus} does not flow in the capacitors C_k,



(b) All capacitors are connected in Parallel



(c) The capacitor C_1 is connected in series and the capacitor C_3 is connected in parallel

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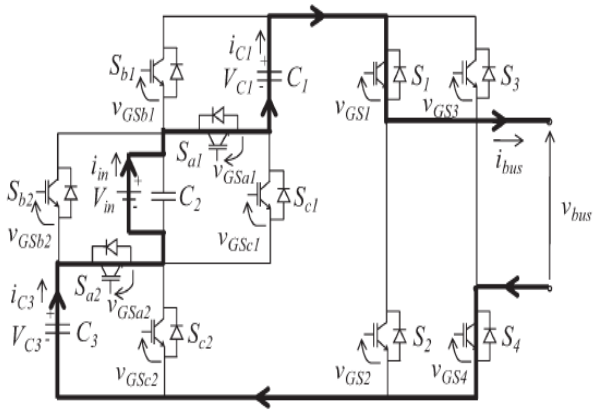

(d) All capacitors are connected in series.

Fig.2. Current flow of the proposed inverter (n = 2) on each state of (a),(b),(c)and(d)

There are many modulation methods to drive a multilevel inverter: the space vector modulation the multicarrier pulse width modulation (PWM) the hybrid modulation the selective harmonic elimination and the nearest level control. In this paper, the multicarrier PWM method is applied to the proposed inverter. Fig. 2 shows the current flow in the proposed inverter (n = 2) and Fig. 3 shows the modulation method of the proposed inverter (n = 2).When the time t satisfies $0 \leq t < t1$ in Fig. 3, the switches $S1$ and $S2$ are driven by the gate-source voltage $vGS1$ and $vGS2$, respectively. While the switches $S1$ and $S2$ are switched alternately, the other switches are maintained ON or OFF state as shown in Fig. 3.

Therefore, the states shown in Fig. 2(a) and (b) are switched alternately and the bus voltage V*bus* takes 0 or *Vin*. When the time t satisfies $t1 \leq t < t2$ in Fig. 3, the switches *Sa*1, *Sb*1, and *Sc*1 are driven by the gate-source voltage *vGSa*1, *vGSb*1, and *vGSc*1, respectively. While the switches *Sa*1, *Sb*1, and *Sc*1 are switched alternately, the other switches are maintained
ON or OFF state as shown in Fig.3.Therefore, the states shown in Fig. 2(b) and (c) are switched alternately. The capacitor $C1$ is charged by the current $-iC1$ as shown in Fig. 2(b) during the state shown in Fig.2(b). Therefore, the proposed inverter can output the bus voltage *vbus* while the capacitor $C1$ is charged. The bus voltage *vbus* in the state of Fig. 2(c) is

$$v_{bus} = V_{in} + V_{C1} \tag{1}$$

III. MODULATION METHOD OF THE PROPOSED INVERTER

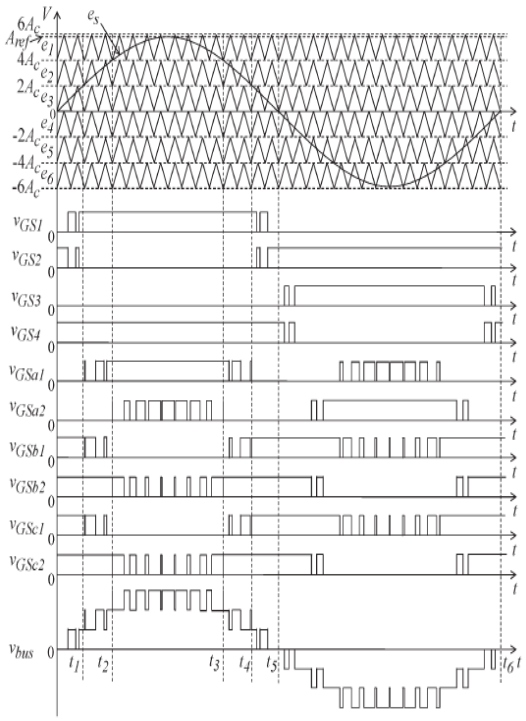

Fig. 3. Modulation method of the proposed inverter (n = 2).

where $VC1$ is the voltage of the capacitor $C1$. Therefore, the proposed inverter outputs *Vin* or *Vin* + $VC1$ alternately in this term. When the time t satisfies $t2 \leq t < t3$ in Fig. 3, the switch *Sa*2, *Sb*2 and *Sc*2 are driven by the gate-source voltage *vGSa*2, *vGSb*2 and *vGSc*2, respectively. While the switches *Sa*2, *Sb*2, and *Sc*2 are switched alternately, the other switches are maintained ON or OFF state as shown in Fig. 3. Therefore, the states shown in Fig. 2(c) and (d) are switched alternately. The capacitor $C3$ is charged by the current $-iC3$ as shown in Fig. 2(c) during the state shown in Fig. 2(c). The bus voltage *vbus* in the state of Fig. 2(d) is

$$v_{bus} = V_{in} + V_{C1} + V_{C3} \tag{2}$$

where $VC3$ is the voltage of the capacitor $C3$. Therefore, the proposed inverter outputs *Vin* + $VC1$ or *Vin* + $VC1$ + $VC3$ alternately in this term. After $t = t3$, the four states shown in Fig. 2 are repeated by turns. Table I shows the list of the on-state switches when the proposed inverter (n = 2) is driven by the modulation method shown in Fig. 3. The ideal bus voltage *vbus* in Table I means the bus voltage on each state when $VC1 = VC3 = Vin$ is assumed. As the conventional SC inverter, the proposed inverter has a full bridge which is connected to the high voltage.

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TABLE I
LIST OF THE ON-STATE SWITCHES ON EACH STATE

Relationship between e_s and e_k	On-state switches	Ideal bus voltage v_{bus}
$e_s > e_1$	S_1, S_4, S_{a1}, S_{a2}	$3V_{in}$
$e_1 \geq e_s > e_2$	S_1, S_4, S_{a1}, S_{b2}, S_{c2}	$2V_{in}$
$e_2 \geq e_s > e_3$	S_1, S_4, S_{b1}, S_{c1}, S_{b2}, S_{c2}	V_{in}
$e_3 \geq e_s > e_4$	S_2, S_4, S_{b1}, S_{c1}, S_{b2}, S_{c2}	0
$e_4 \geq e_s > e_5$	S_2, S_3, S_{b1}, S_{c1}, S_{b2}, S_{c2}	$-V_{in}$
$e_5 \geq e_s > e_6$	S_2, S_3, S_{b1}, S_{c1}, S_{a2}	$-2V_{in}$
$e_6 \geq e_s$	S_2, S_3, S_{a1}, S_{a2}	$-3V_{in}$

Therefore, the device stress of the switches $S1 - S4$ in the full bridge is higher than the other switches as the conventional SC inverter. The proposed inverter (n = 2) outputs a 7-level voltage by repeating the four states as shown in Fig. 2. Because the driving waveform $vGSa1$ and $vGSa2$ change alternately as shown in Fig. 3, the capacitors $C1$ and $C3$ are equally discharged. Assuming that the number of the capacitors is $2n - 1$, the proposed inverter can outputs $4n - 1$ levels voltage waveform. The modulation index M is defined as the following equation because the amplitude of the output voltage waveform is inversely proportional to the double amplitude of the carrier waveform.

$$M = A_{ref}/2A_c. \tag{3}$$

In (3), *Aref* is the amplitude of the reference waveform and *Ac* is the amplitude of the carrier waveform. The proposed inverter requires 10 switching devices for the 7-level, and 16 switching devices for the 11-level. On the other hand, the conventional SC inverter requires 20 switching devices for the 7-level, and 28 switching devices for the 11-level [9]. The conventional cascaded H-bridge (CHB) inverter requires 12 switching devices for the 7-level, and 20 switching devices for the 11-level, when all the dc voltage sources take the same voltage [17]. Therefore, the proposed inverter has less number of switching devices than the conventional multilevel inverters.

IV. DYNAMIC MODELLING OF INDUCTION MOTOR

In a conventional four pole induction motor, there are two sets of identical voltage profile windings will be present in the total phase winding. These two windings are connected in series as shown in fig. 4(a). For the proposed inverter these two identical voltage profile winding coils are disconnected, and the available four terminals are taken out, like shown in the fig.4 (b). Since these two windings are separated equally, stator resistance, Stator leakage inductance and the magnetizing inductance of each identical voltage profile windings are equal to the half of the normal induction motor shown in fig.4 (a). The voltage equitation for the stator winding is given by common dc link.

$$V_{a1} - V_{a2} = \left(\frac{r_s}{2}\right) * i_{as} + \left(\frac{L_{ss}}{2}\right) * i_{as} - \left(\frac{1}{2}\right) * \left(\frac{L_m}{2}\right) * i_{bs} - \left(\frac{1}{2}\right) * \left(\frac{L_m}{2}\right) * i_{cs} \tag{4}$$

$$V_{a3} - V_{a4} = \left(\frac{r_s}{2}\right) * i_{as} + \left(\frac{L_{ss}}{2}\right) * i_{as} - \left(\frac{1}{2}\right) * \left(\frac{L_m}{2}\right) * i_{bs} - \left(\frac{1}{2}\right) * \left(\frac{L_m}{2}\right) * i_{cs} \tag{5}$$

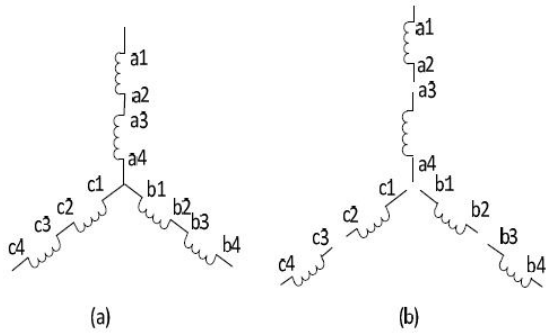

Fig. 4 Induction Motor stator winding: (a) General arrangement (b) Arrangement for the proposed inverter

The effective voltage across the stator winding is the sum of the voltages across the two individual windings.

$$V_{as} = (V_{a1} - V_{a2}) + (V_{a3} - V_{a4}) \tag{6}$$

The motor phase voltage can be achieved by substituting equations (4) and (5) in (6)

$$V_{as} = r_s * i_{as} + L_{ss} * i_{as} - \left(\frac{1}{2}\right) * L_m * i_{bs} - \left(\frac{1}{2}\right) * L_m * i_{cs} \tag{7}$$

Similarly voltage equitation for the remaining phases are

$$V_{bs} = r_s * i_{bs} + L_{ss} * i_{bs} - \left(\frac{1}{2}\right) * L_m * i_{as} - \left(\frac{1}{2}\right) * L_m * i_{cs} \tag{8}$$

$$V_{cs} = r_s * i_{cs} + L_{ss} * i_{cs} - \left(\frac{1}{2}\right) * L_m * i_{as} - \left(\frac{1}{2}\right) * L_m * i_{bs} \tag{9}$$

Voltage equations in dq0 frame can be solved from the basic equations of induction motor

$$V_{qs} = r_s * i_{qs} + \omega * \lambda_{ds} + \rho * \lambda_{qs}$$

$$V_{ds} = r_s * i_{ds} - \omega * \lambda_{qs} + \rho * \lambda_{ds}$$

$$V_{0s} = r_s * i_{0s} + \rho * \lambda_{0s}$$

$$V_{qr} = r_r * i_{qr} + (\omega - \omega_r) * \lambda_{dr} + \rho * \lambda_{qr}$$

$$V_{dr} = r_r * i_{dr} - (\omega - \omega_r) * \lambda_{qr} + \rho * \lambda_{dr}$$

$$V_{0r} = r_r * i_{0r} + \rho * \lambda_{0r}$$

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Flux linkages are as follows

$$\lambda_{qs} = L_{ss} * i_{qs} + L_M * i_{qr}$$

$$\lambda_{ds} = L_{ss} * i_{ds} + L_M * i_{dr}$$

$$\lambda_{0s} = L_{1s} * i_{0s}$$

$$\lambda_{qr} = L_{rr} * i_{qr} + L_M * i_{qs}$$

$$\lambda_{dr} = L_{rr} * i_{dr} + L_M * i_{ds}$$

$$\lambda_{0r} = L_{1r} * i_{0r}$$

The expression for the electromagnetic torque in terms of dq0 axis currents is

$$T_e = \left(\frac{3}{2}\right) * \left(\frac{P}{2}\right) * L_M * \left(i_{qs} * i_{dr} + i_{ds} * i_{qr}\right) \quad (10)$$

Rotor speed in terms of Torque is

$$\frac{d}{dt}\omega_e = \left(\frac{P}{2 * J}\right) * (T_e - T_L) \quad (11)$$

Where
d: direct axis,
q: quadrature axis,
s: stator variable,
r: rotor variable,
V_{ds},V_{qs},: q and d–axis stator voltages,
V_{dr},V_{qr},: q and d–axis rotor voltages,
r_r : Rotor resistance,
V_{rs} : Stator resistance,
L_{1s}: stator leakage inductance,
L_{1r} : rotor leakage inductance,
i_{qs} ,i_{ds}: q and d–axis stator currents,
i_{qr}, i_{dr}: q and d–axis rotor currents,
p: number of poles,
J: moment of inertia,
T_e : electrical output torque,
T_L : load torque.

From the equations (4), (5),(6) it can be observed that there is no difference between the normal induction motor shown in fig.2 (a) and the disconnected (Identical voltage profile windings) motor shown in fig.2 (b).

V. SIMULATION RESULTS

Here simulation is carried out in different cases 1). Proposed Single Phase Series/Parallel Topology 2). Proposed Three Phase Series/Parallel Topology Applied to Induction machine Drive.

Case 1: Proposed Single Phase Series/Parallel Topology

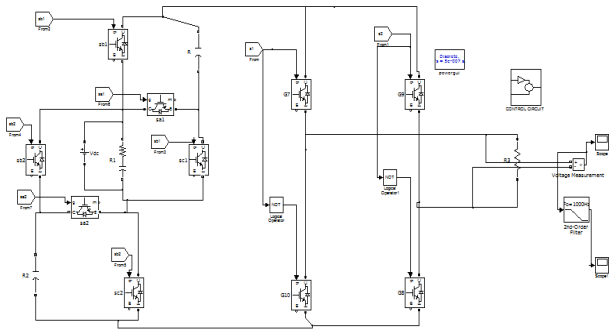

Fig. 5 Matlab/Simulink Model of Proposed Single Phase Series/Parallel Converter

Fig.5 shows the Matlab/Simulink Model of Proposed Single Phase Series/Parallel Converter.

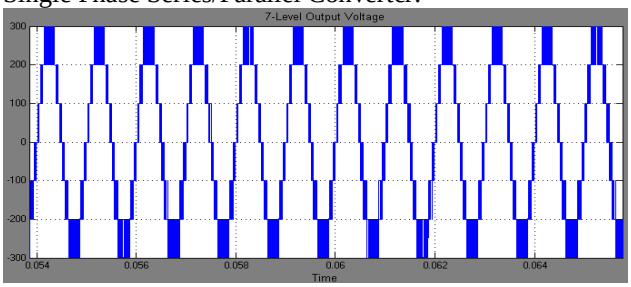

Fig. 6 Seven Level Output Voltage

As Fig.6 shows the single phase seven level output voltage without filter of proposed series/parallel converter.

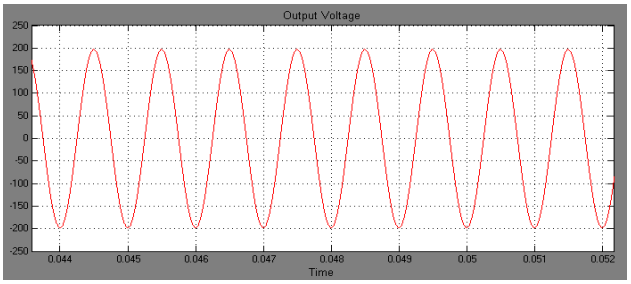

Fig. 7 Output Voltage with Filter

As Fig.7 shows the single phase output voltage with filter of proposed series/parallel converter, by using filter we get fully sinusoidal nature of voltage.

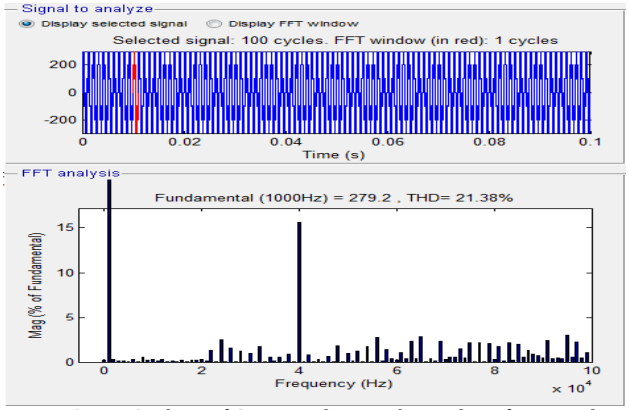

Fig. 8 FFT Analysis of Output Voltage without Filter of Proposed Series/Parallel Converter

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As above Fig. 8 shows the FFT Analysis of Output Voltage without Filter of Proposed Series/Parallel Converter, we get 21.38%.

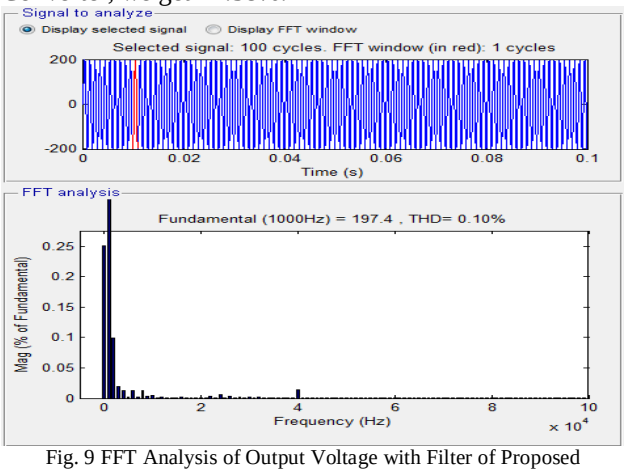

Fig. 9 FFT Analysis of Output Voltage with Filter of Proposed Series/Parallel Converter

As above Fig. 9 shows the FFT Analysis of Output Voltage with Filter of Proposed Series/Parallel Converter, we get 0.10%.

Case 2: Proposed Three Phase Series/Parallel Topology Applied to Induction machine Drive.

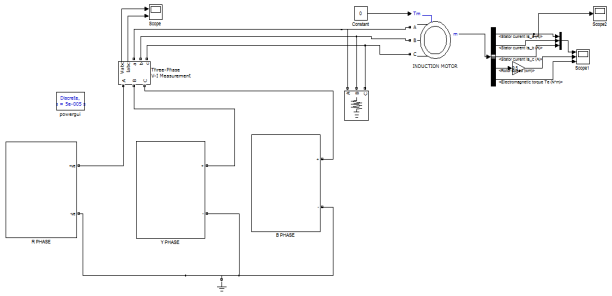

Fig. 10 Matlab/Simulink Model of Proposed Three Phase Series/Parallel Converter Applied to IM Drive

Fig.10 shows the Matlab/Simulink Model of Proposed Three Phase Series/Parallel Topology Applied to Induction machine Drive.

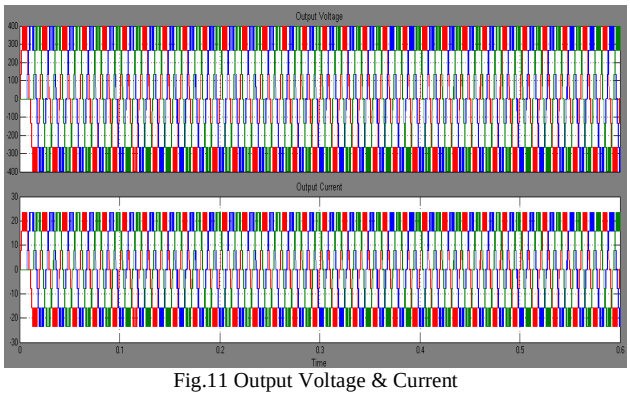

Fig.11 Output Voltage & Current

Fig.11 shows the Output Voltage & Current of Proposed Three Phase Series/Parallel Topology.

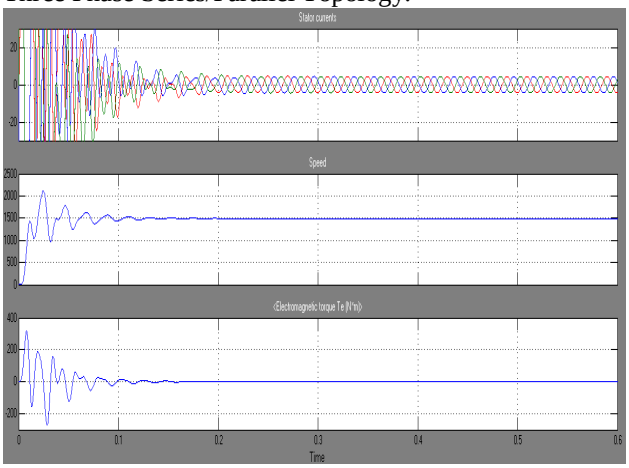

Fig.12 Stator Currents, Speed, Electromagnetic Torque

Fig.12 Stator Currents, Speed, Electromagnetic Torque of Proposed Three Phase Series/Parallel Topology Applied to Induction machine Drive.

VI. CONCLUSION

With the advancement of power electronics and emergence of new multilevel converter topologies, it is possible to work at voltage levels beyond the classic semiconductor limits. The multilevel converters achieve high-voltage switching by means of a series of voltage steps, each of which lies within the ratings of the individual power devices. In this paper, a novel boost switched-capacitor inverter was proposed & proposed three phase series/parallel topology applied to induction machine drive to check the performance of drive characteristics, the circuit topology was introduced. The modulation method, the determination method of the capacitance, and the loss calculation of the proposed inverter were shown. The circuit operation of the proposed inverter was confirmed by the simulation results with a resistive load and a machine load. The proposed inverter outputs a larger voltage than the input voltage by switching the capacitors in series and in parallel. The structure of the inverter is simpler than the conventional switched-capacitor inverters. THD of the output waveform of the inverter is reduced compared to the conventional single phase full bridge inverter as the conventional multilevel inverter.

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