Dual-Mode Supply Modulator for CMOS Power Amplifier Based on PFM Control

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Abstract: This paper presents a dual-mode supply modulator adopting a PFM scheme for the APT and a PWM scheme for the ET mode for CMOS power amplifiers. The supply modulator operates as just a buck converter based on a PFM control for the low power APT mode and operates as a hybrid buck converter based on a PWM control for the high power ET mode. The CMOS power amplifier was designed to have a two-stage differential common-source structure. The dual-mode supply modulator and power amplifier were designed using a 0.18μm CMOS process for the 0.78 GHz LTE band. The 16-QAM LTE signal which has a 16-QAM signal bandwidth of 5 MHz and a PAPR of 7.3 dB was used for the test. The CMOS power amplifier exhibited a PAE of 38.82% at an average output power of 22 dBm with an ET mode, while it also exhibited a PAE of 16.53% at average output power of 12 dBm with an APT mode, which is 8.07% higher than that of the stand-alone power amplifier.

Keywords: Power amplifier, dual-mode supply modulator, envelope tracking, average power tracking, long-term evolution.

INTRODUCTION

The wireless communication systems have evolved to have higher data rates. The radio frequency (RF) modulated signals to have high data rates are required to have wide signal bandwidth and high peak-to-average power ratio (PAPR). Power amplifiers (PAs) consumes significant portion of power in the total wireless communication systems since they must be backed off to meet the strict linearity standards.

Many research results have been reported to improve the efficiency of PA especially at the back-off region. The representative techniques for efficiency improvement can be listed as Doherty, Envelope Elimination and Restoration (EER), Envelope Tracking (ET), and so forth [1]-[3]. Among the various techniques for the efficiency improvement, ET is one of the most suitable solutions if both the linearity and efficiency are considered [4]. The ET method improves the efficiency of the PA by supplying the modulated supply voltage according to the envelope signal to the PA using a supply modulator.

In this paper, a dual-mode supply modulator adopting a PFM scheme for the APT and a PWM scheme for the ET mode is proposed for CMOS power amplifiers. The supply modulator operates as a simple buck converter based on a PFM control for the low power APT mode, while it operates as a hybrid buck converter based on a PWM control for the high power ET mode. Switches and multiplexers (MUXs) are included in the supply modulator to switch the operational modes.

A PA integrated circuit (IC) and a dual-mode supply modulator were designed and fabricated using a 0.18μm CMOS process for the 0.78 GHz band. The dual-mode supply modulator is applied to the integrated differential CMOS PA and is verified its performances

compared to the stand-alone PA and the previously published results.
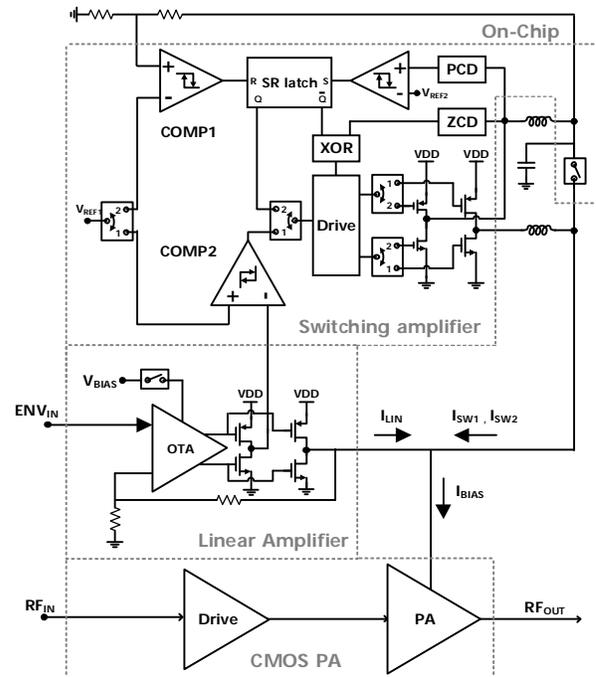
Fig 1: Schematic of the dual-mode supply modulator and the CMOS PA IC.

SUPPLY MODULATOR DESIGN

Fig 1 shows a schematic of the dual-mode supply modulator whose mode is switched from a buck converter for the APT mode to a hybrid buck converter for the ET mode or vice versa. The hybrid buck converter consists of a linear amplifier for a wide bandwidth and a switching amplifier for high efficiency. For high output power levels, the hybrid buck converter can effectively boost the efficiency of the PA with the ET mode using a PWM control. In a large back-off power region, the improvement of the efficiency is significantly degraded due to the relatively high DC consumption of the linear amplifier. The PFM based buck converter can be applied to the PA for the APT mode for the large back-off region. Though the PFM control is too slow to handle the envelope signal, it can improve the efficiency of the supply modulator for the APT mode.

According to the reference output power level, the mode control signal controls single-pole double-through (SPDT) switches to "1" for ET mode or to "0" for APT mode. Single-pole single-through (SPST) switches are also controlled to "open or OFF" for ET mode or to "short or ON" for APT mode by the mode control signal. For the APT mode, the mode control signal turns the linear amplifier off to have a buck converter only with the switching amplifier.

For the APT mode, the comparator 1 generates a PFM signal. Using the input reference voltage (VREF1) at the negative input terminal of the comparator 1, the output DC voltage of the buck converter can be appropriately adjusted according to the average

output power level. If the feed-back output voltage is higher than VREF1, the comparator 1 returns "HIGH" and resets the SR latch.
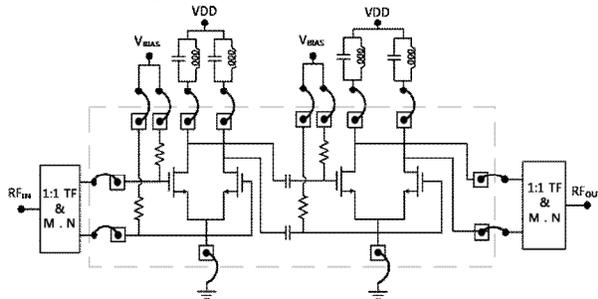
Fig. 2: Schematic of the CMOS PA

And the supply modulator charges the off-chip inductor and capacitor of the buck converter until the inductor current reaches to the peak by PCD. When the sensed voltage by PCD is larger than VREF2, the SR latch is set and the stored energy in the inductor is released to charge the capacitor. As the inductor releases all of the stored energy and if the feedback voltage is still lower than VREF1, the signal sets the SR latch is masked to turn off both power switches and the output capacitor is discharged by the load current until the feedback voltage is larger than VREF1 the off-chip inductor and capacitor of the buck converter start to be charged again. This process goes periodically.

For a low power region, the inductor and capacitor are charged and discharged using this cycle. The PFM control method reduces the switching loss of the output switches which can lower the efficiency. The off-chip inductor and capacitor must be optimized for better performance for the APT mode.

POWER AMPLIFIER DESIGN

A schematic of the CMOS PA is shown in Fig. 2. For sufficient gain, the PA consists of two differential stages which have common-source configuration. The drain bias of the second stage is supplied by the dual-mode supply modulator. The first stage has a total gate width of 1,200 μm and a quiescent current of 10 mA with a fixed drain bias of 3.3 V. the second stage has a total gate width of 4,000 μm and a quiescent current of 28 mA with a variable drain bias according to the selected operation mode. For high efficiency with a compromised linearity, both stages are biased for a deep Class-AB operation. To achieve a proper load match and to make a differential to a single-ended conversion, an external passive components and a 1:1 transformer having a loss of about 0.2 dB are used. For both stages, the second harmonics are controlled using bond wires and capacitors at the drain terminals to improve the linearity and efficiency.

MEASUREMENT RESULTS

The proposed dual-mode supply modulator is designed and fabricated with a CMOS PA using a 0.18 μm CMOS process. Fig. 3 shows a microphotograph of the implemented IC. Its size is 1.89 mm x 0.08 mm including the bond pads. The fabricated chip is mounted on a FR-4 printed circuit board for evaluation. The dual-mode supply modulator and PA requires a single supply voltage of 3.3 V.

A. DUAL MODE SUPPLY MODULATOR

The 16-QAM LTE up-link signal with a PAPR of 7.3 dB, a signal bandwidth of 5 MHz, and a center frequency of 0.78 GHz was used as an input signal to evaluate the dual-mode supply modulator. The supply modulator linearly amplifies the input envelope signal with a proper gain for the ET mode. For the APT mode, the supply modulator supplies a DC voltage which is much lower than the normal drain bias to the drain of the second stage.

The equivalent load resistance of the supply modulator for low output power is larger than that for high output power. In our design, the equivalent load resistances of 10 Ω and 39 Ω are selected for the ET mode and the APT mode, respectively, through the simulation using the LTE signal.
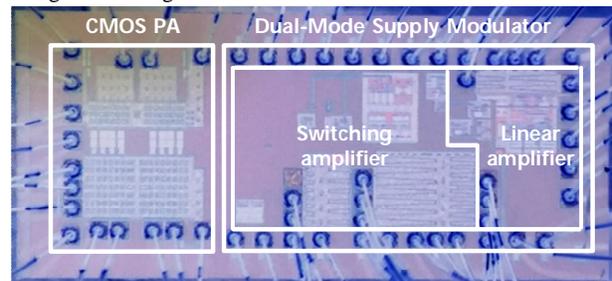
Fig 3: Chip microphotograph
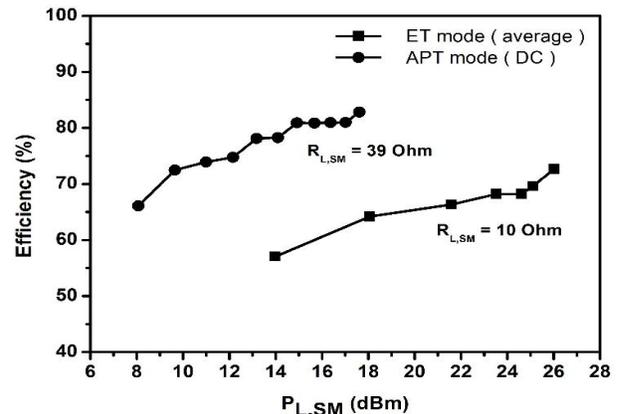
Fig. 4: Measured efficiencies for the ET and APT modes using a 16-QAM LTE signal according to the power delivered to the load.

Table 1 Performances of the dual-mode supply modulator

Parameters	ET mode	APT mode
Supply voltage	3.3 V	
Output voltage range	0.1 – 3.0 V	0.1 – 1.5 V
Unit-gain bandwidth	50 MHz	N/A
Efficiency	72.7%	82.8%
APT mode	$R_{L,SM} = 39\ \Omega$, DC, $V_{DC} = 1.5V$	
ET mode	$R_{L,SM} = 10\ \Omega$, LTE 5 MHz, $P_{load} = 26.1\ dBm$	

The measured efficiencies according to the power delivered to the load are plotted on Fig. 4. An average output power of 26.1 dBm was achieved with an efficiency of 72.7% for the ET mode. For the APT mode, the supply modulator exhibits higher efficiency at relatively low power levels. An average output power of 17.61 dBm was delivered to the load with an efficiency of 82.8% for the APT mode. The measured performances of the proposed dual-mode supply modulator are summarized in Table 1.

B. CMOS POWER AMPLIFIER

The 16-QAM LTE up-link signal with a PAPR of 7.3 dB, a signal bandwidth of 5 MHz, and a center frequency of 0.78 GHz is applied to the fabricated CMOS PA. Fig. 5 shows the efficiency and gain of the PA with various supply voltages of from 0.5 to 3.3 V. The PA exhibited a power gain of 27 dB and an efficiency of 46.37% at an 1 dB compression point of 27 dBm with a supply voltage 3.3 V. By lowering the supply voltage, the PA maintains high efficiency at a back-off power region. The output power level with a given ACLR of -30 dBc accordingly moves lower as the supply voltage decreases.

C. PERFORMANCES of OVERALL CIRCUITS

Fig. 6(a) shows the measured gain and overall efficiency for the conditions including the stand-alone PA, PA for ET mode, and PA for APT mode. The efficiency of the ET PA at an average output
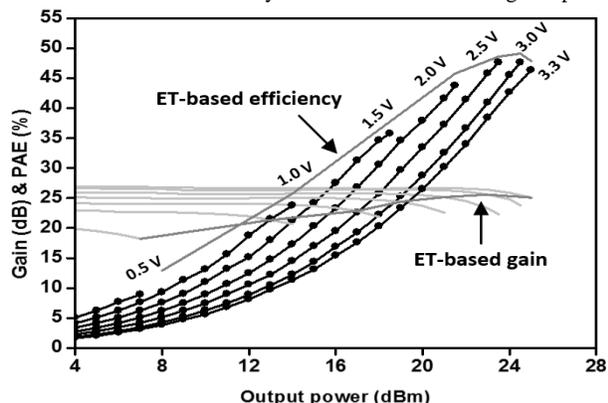
Fig 5: Measured gain and PAE for LTE signal

power of 22 dBm is as high as 38.82% which is 3.8% higher than that of the PA alone. For a 10 dB back-off point, at which the output power is 12 dBm, the efficiency of the APT PA is 1.81% better than that of the ET PA. The efficiency improvements of the PA for both modes are plotted in Fig. 6(b). As expected, the APT PA shows better efficiency in the low power region which is lower than the efficiency crossover. The efficiency crossover is experimentally found at an output power of around 13 dBm. The ET PA and APT PA have efficiencies of 7.71% at an output power of 16 dBm and 8.07% at an output power of 12 dBm, respectively. The performances of the ET/APT PA for the LTE signal are summarized in Table 2.

CONCLUSION

In this paper, a single-chip CMOS power amplifier with a dual-mode supply modulator is designed and fabricated for 0.78 GHz LTE applications using a 0.18 μm CMOS process. For better efficiency at the very low power level, the supply modulator is controlled to operate as a buck converter for the APT mode based on PFM control. At an output power level higher than a given threshold, the supply modulator is controlled to operate as a hybrid buck converter for the ET mode based on PWM control. For the ET mode, a dynamic voltage according to the envelope signal after proper shaping is supplied to the drain of the PA. For an APT mode, a constant DC voltage lower than the normal supply voltage is applied to the drain of the PA.

The fabricated PA IC was evaluated using an up-link 16-QAM LTE signal with a channel bandwidth of 5 MHz. The ET PA exhibited a PAE of 38.82%, a gain of 21.7 dB, and an ACLR of -30 dBc at an average output power of 22 dBm. Compared to the stand-alone PA, the ET PA shows an improved PAE of 7.71% at an

(a)

(b)
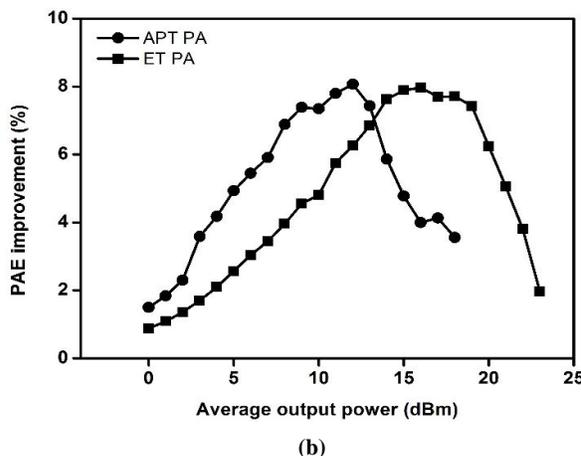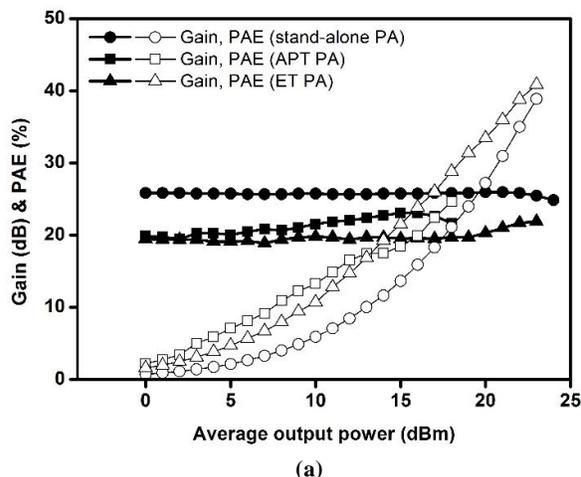
Fig 6: Measured performances of the stand-alone PA, PA for ET mode, and PA for APT mode (a) gain and PAE, (b) PAE improvements compared to the stand-alone PA

average output power of 16 dBm. At an average output power of 12 dBm which is a 10dB back-off from the peak output power, the APT PA showed a PAE of 16.53% which is 8.07% improvement over the stand-alone PA. The buck converter using PFM control can be used for the supply modulator to improve the efficiency of the PA with APT mode.

Table 2. Performance of Comparison of the ET PAs

Ref.		Freq. (GHz)	Supply (V)	Pout (dBm)	PAE(%) at back-off			Gain (dB)	ACLR (dBc)	Modulation	Technology
					0 dB	9 dB	15 dB				
5		1.85	5.0	28.9	42.2	18.0	-	24.5	-	LTE 16-QAM 10 MHz	PA : 2-μm InGaP/GaAs SM : 0.13-μm CMOS
6		1.90	4.2	24.0	41.0	12.0	-	15.0	-	LTE 16-QAM 5 MHz	PA, SM : 0.35- μm SiGe BiCMOS
7		1.74	5.0	27.0	39.8	22.6	9.0	3.8	-35.7	LTE 16-QAM 10 MHz	PA : 2- μm InGaP/GaAs SM : 0.18 μm CMOS
8		1.85	5.0	26.0	34.1	15.0	6.0	10.0	-34.2	LTE 16-QAM 10 MHz	PA, SM : 0.18 μm CMOS
This work	APT ET	0.78	3.3	22.0	- 38.82	17.47 14.72	9.18 5.70	23.06 21.70	-30	LTE 16-QAM 5 MHz	PA, SM : 0.18 μm CMOS

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