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Implementation of DDR SDRAM Memory Controller for embedded SOC

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Abstract: DDR SDRAM is similar in function to the regular SDRAM but doubles the bandwidth of the memory by transferring data on both edges of the clock cycles.DDR SDRAM most commonly used in various embedded application like networking, image/video processing, Laptops etc. The memory controller accepts commands using local interface and translates them to the command sequences required by DDR SDRAM devices. However there are challenges in its controller design those are arising to its straight requirement much as regular refresh operation, memory initialization process, proper active and precharge command etc. The principle and commands of DDR SDRAM controller design are explained in this paper. The operations of DDR SDRAM controller are realized through Verilog HDL .This proposed architecture design of DDR SDRAM controller is used as IP core into any FPGA based embedded system having requirement of high -speed operation.

Keywords: DDR SDRAM, AHB, burst access, pipeline, Verilog HDL.

I. INTRODUCTION

Double data rate synchronous dynamic random-access memory (DDR SDRAM) is a class of memory integrated circuits used in computers. Nowadays, Memory devices are almost found in all systems, high speed and high performance memories are in great demand. For better throughput and speed, the controllers are to be designed with clock frequency in the range of megahertz. As the clock speed of the controller is increasing, the design challenges are also becoming complex. Therefore the next generation memory devices require very high speed controllers like double data rate and quad data rate memory controllers. In this paper, the double data rate SDRAM Controller is implemented using ASIC methodology. Synchronous DRAM (SDRAM) is preferred in embedded system memory design because of its speed and pipelining capability. In high-end applications, like microprocessors there will be specific built in peripherals to provide the interface to the SDRAM. But for other applications, the system designer must design a specific memory controller to provide command signals for memory refresh, read and write operation and initialization of SDRAM. In this paper, the SDRAM controller, located between the SDRAM and the bus master, minimizes the effort to deal with the SDRAM memory by providing a simple system to interact with the bus master. Figure 1 is the block diagram of the DDR SDRAM Memory Controller that is connected between the bus master and SDRAM.

Single data rate (SDR) SDRAM that drives/latches data and command information on the rising edge of the synchronous clock. DDR SDRAM is a type of SDRAM that inherits technologies from SDR SDRAM and realizes faster operation and lower power consumption.DDR SDRAM achieves a data transfer rate that is twice the clock frequency by employing 2-n bit prefetch architecture [3].In this architecture, 2n bits of data are transferred from the memory cell array to the I/O buffer every clock. Data transferred to the I/O buffer is output n bits at a time every half clock (both rising and falling edges of the clock (CK)).

The proposed memory controller shown in figure 1 used to interface memory to other rest of the embedded system. Several tasks like refresh management, initialization, command generation, address mapping etc are done by memory controller. This Memory controller design has implemented in RTL in Verilog. The focus of this work is to implement design of DDR SDRAM controller which provide memory interface between the DDR SDRAM memory module and main embedded system. Top level model is shown in fig.1.The design contains the DDR SDRAM controller between the Host and the DDR SDRAM memory.

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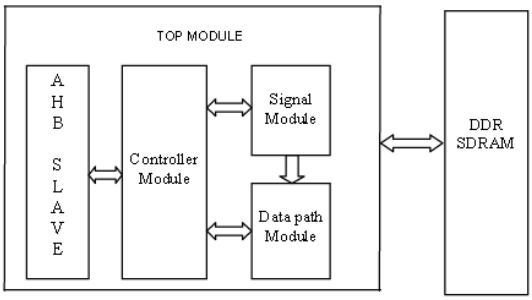

Fig.1: Top level Block Diagram of DDR SDRAM Controller for FPGA

Synchronous DRAM

Synchronous dynamic random access memory (SDRAM) is dynamic random access memory (DRAM) that is synchronized with the system bus. Classic DRAM has an Asynchronous interface, which means that it responds as quickly as possible to changes in control inputs. SDRAM has a synchronous interface, meaning that it waits for a clock signal before responding to control inputs and is therefore synchronized with the computer's system bus enabling higher speed. The SDRAM controller is capable of either 16-bit or 32-bit data path, and supports byte, half -word and word access. Bursts can be used for both write and read access. A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during Reads and by the memory controller during Writes. DQS is edge-aligned with data for Reads and canter-aligned with data
for Writes. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed. The address bits registered coincident with the Read or Write command are used to select the bank and the starting column location for the burst access. The DDR SDRAM provides for programmable Read or Write burst lengths of 2, 4 or 8 locations. An Auto Precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access. As with standard SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

II. Implementation of Block Diagram

The DDR SDRAM Controller architecture is implemented using Verilog HDL. The methodology followed is ASIC design flow. The basic steps that an ASIC design must go through are Design entry and Analysis, Technology Optimization and Floor planning, Design Verification. The RTL Synthesis and Simulations are performed using existing tools like RTL Compiler. Figure 1 shows the different blocks in top level reference design. The user interface module contains the I/O registers to latch system signals coming into the FPGA. The DDR controller module contains the DDR SDRAM controller, including I / Os to interface with the DDR SDRAM.

DDR SDRAM Controller Architecture

DDR SDRAM Controller module receives addresses and control signals from the BUS Master. The Controller generates command signals and based on these signals the data is either read or written to a particular memory location. The DDR SDRAM Controller architecture is shown in Figure 2.

It consists of three modules:

1) Main control module
2) Signal generation module
3) Data path module.

The main control module has two state machines and a refresh counter. The two state machines are for initialization of the SDRAM and for generating the commands to the SDRAM. They generate iState and cState outputs according to the system interface control signals. The signal generation module now generates the address and command signals depending upon the iState and cState. The data path module performs the read and write operations between the bus master and DDR. Following are some of the important features of DDR SDRAM Controller:

i. The DDR SDRAM Read and Write operations are simplified by the controller.
ii. For initializing the DDR SDRAM controller,
Separate state machines are designed internally.
iii. The access time for read and the write cycle is optimized based on the CAS latency and burst
length of the DDR SDRAM.

The main control module consists of three sub modules:

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1) Initialization FSM module (INIT_FSM).
2) Command FSM module (CMD_FSM)
3) Counter module.

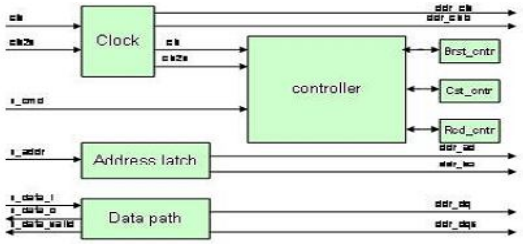

Figure 2: DDR Controller Architecture

III. Different Functional Blocks

Address Latch

The basic function of address latch module is to gets its control signals from the controller and generates row, column and bank addresses for the DDR SDRAM. The address latch also generates different control signals like burst_max, cas_lat_max for the burst counter and cas latency counter.

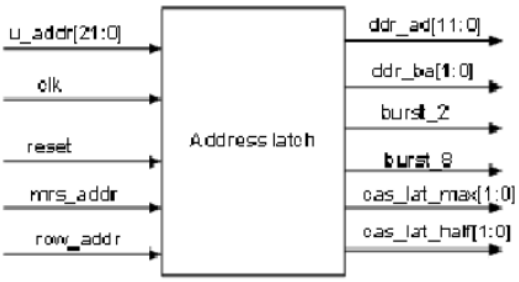

Figure 3: Address Latch Module

Data Path

One of the most difficult aspects of DDR SDRAM controller design is to transmit and capture data at double data rate. This module transmits data to the memories. The basic function of data path module is storing the write data and calculates the value for read data path.

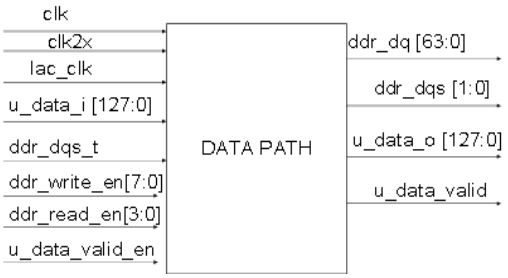

Figure 4: Data Path Module

Controller

The controller consists of a state machine which performs DDR SDRAM read and write accesses based on user interface request. The controller consists of a high performance timing & control state machine that observes all timing requirements and issues the commands to the memory devices at the shorted
time possible. The pin diagram of controller is shown in figure 5:

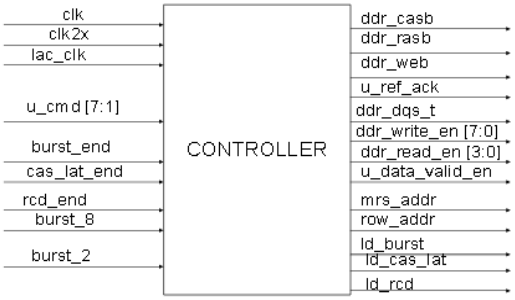

Figure 5: Controller Module

The DDR controller consists of a high performance memory controller for system requiring access to external devices with lowest latency and highest throughput. The controller accepts and decodes user interface commands and generates read, write, refresh commands. It also generates signals for other modules. The memory is initialized and powered up using a defined process. The controller state machine handles the initialization process upon power up. Controller state machine diagram

Initially the controller is in the IDLE state. That means no operation is performing. A PRECHARGE ALL command is then applied. This command is used to deactivate any open row in a bank or the open bank row in all banks. Once a bank

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is pre charged, it is in idle state and must be activated prior to any READ and WRITE operation. Next a LOAD MODE REGISTER command should be issued for the extended mode register to enable the DLL, then another LOAD MODE REGISTER command to the mode register to reset the DLL and to program the operating parameters. Again a PRECHARGE command should be applied which place the device in all banks in IDLE state. In the IDLE state two AUTO REFRESH cycles must be performed.

The controller next state could be PRECHARGE, LOAD_MR, REFRESH or ACT, depending upon the required command. The ACT command is used to open a row in a bank before starting any read or write operation. The controller state machine diagram is shown in figure 6.

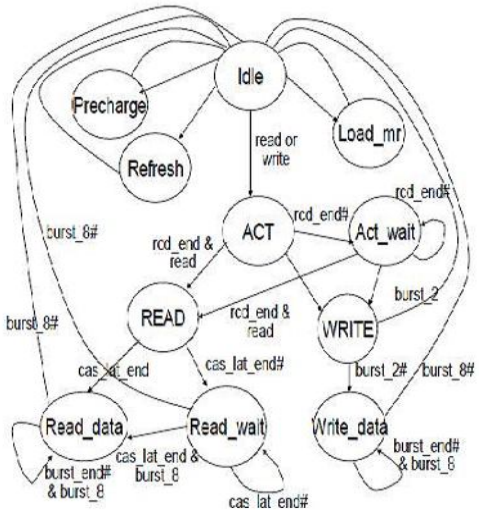

Figure 6: controller state machine diagram

counter

The task of Burst Count is to count when there are consecutive READ and WRITE operations. While doing consecutive READ and WRITE operations, the Burst count value determines when the next READ and WRITE command should be issued.

IV. Implementation and results

In this work we have designed a High speed DDR SDRAM Controller with 64-bit data transfer which synchronizes the transfer of data between DDR RAM and External AHB compatible devices. This can be used in ARM based SOC design. The advantages of this controller compared to SDR SDRAM is that it synchronizes the data transfer, and the data transfer is twice as fast as previous, the production cost is also very low. This core is verified by using test bench and several test cases, which cover most of the functionality of the core. Cadence RTL Compiler for the Synthesis of Controller.

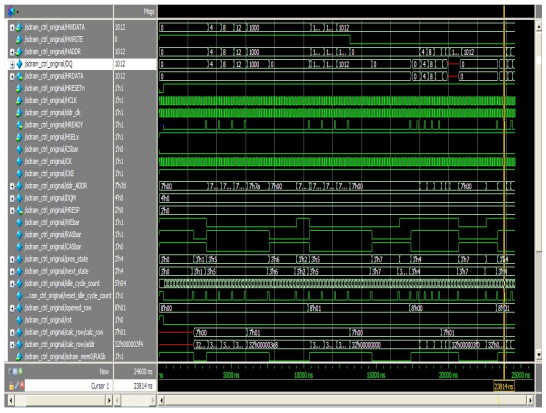

Figure 7: Simulation waveform for Controller

Read operation

In the Read operation the data with DQS signal coming from the memory which is latched at data path module.

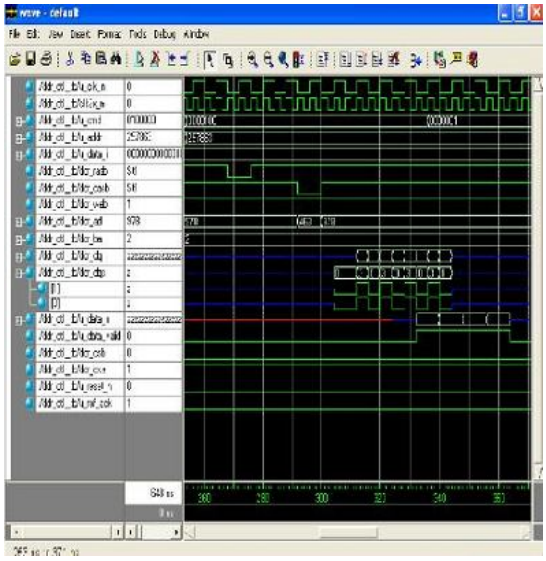

Figure 8: Simulation waveform for Controller Read Cycle

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Write operation

In the Write operation the data with DQS signal and DM (data mask) signal coming from the memory controller to Memory.

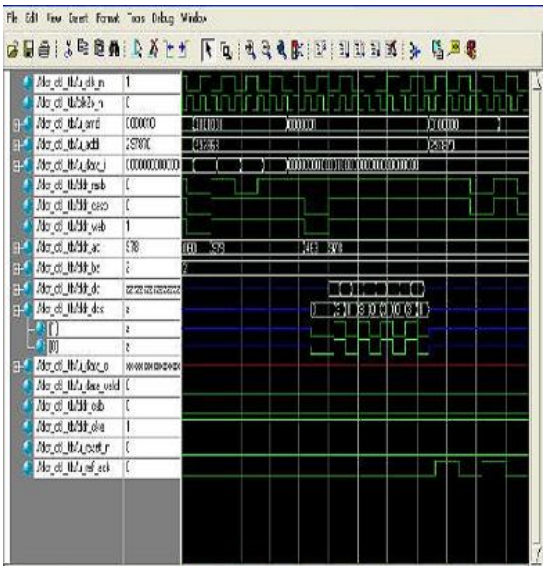

Figure 9: Simulation waveform for Controller write Cycle

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