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Elimination of Glitch in DG-GDI based full adder

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Abstract: Addition and multiplication are the fundamental operations for any digital system like digital signal processor to compute FFTs. For these computations speed of operation is needed. There are various technologies for developing the full adder circuits some of them are 28-Transistor full adder, 26-Transistor full adder, 20-Transistor full adder, full adder. In this paper we proposing full adder which is based on double gate GDI (DG_GDI) as basic element for implementation of the functionality of the full adder with 180nm technology. Two DG-GDI full adders are designing for reducing delay and power. DG-GDI full adder uses less no. of transistor count and improves the speed of operation. The propagation delay, area and speed are important design metrics for the design of adder circuits in VLSI. The full adder circuits are designed using Cadence tool and simulation done using Spectre tool with 180nm technology. By the transient analysis of adder circuits using cadence tool found that the delay of proposed DG-GDI full adder is 87.13 ps and the average power is 0.03mW. Hence it gives better performance than conventional full adders.

Keywords: GDI, DG-DGI, Full Adder, CMOS technique, Propagation Delay, Power dissipation

1. INTRODUCTION

VLSI is abbreviated as “Very Large Scale Integration” in this field hundreds of thousands of transistors are integrated on a single chip thus reducing the chip size. VLSI is one of the basic building blocks of today’s high-end technology. This technology has opened many new gate ways in advancement of technology. Increasing the need of integrating large number of circuits on a single chip can be fulfilled by these technologies. VLSI finds its huge application in nano technology by reducing the size of the chip to the least. In VLSI design some of the important design metrics are to be considered which are power, delay, speed, area.

Adders and multipliers circuits are essential in most of the signal and image processing applications. The basic block for design of MAC unit in digital signal processors is full adder circuit. Full adder circuits has three inputs and two outputs, it performs addition operation on three inputs and generates sum and carry output as per the truth table shown in table I. Full adder can also be used in ALUs in microprocessors, Digital signal processing. Here by increasing the performance of the full adder circuit the overall performance of the respective applications increases.

Table I: Full adder truth table

A	B	C_IN	SUM	C_OUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

1.1 The Basic circuit of a Full Adder:

From the table I, the full adder logic is implemented. We can observe that the output SUM is the XOR operation between the inputs A, B, C_IN and we have also noticed that the C_OUT will only be HIGH if any of the two inputs out of the three are HIGH. Thus, from the above conclusion the full adder circuit can be implemented with the help of two half adder circuits. Among these two half adder circuits the first half adder add A and B to produce a partial Sum and the second half adder circuit can be used to add CIN and the Sum produced by the first half adder to generate the final SUM output. If any of the provided two half adder logic generates a carry, then the carry out (C_OUT) goes high. Take a look at the implementation of the full adder circuit using XOR gate and MUX is shown in the figure 1.

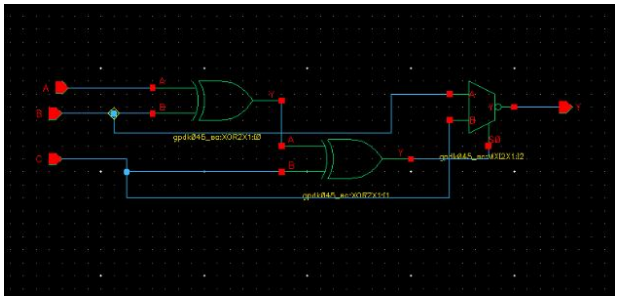

Figure 1: Basic adder circuit

1.2 EXISTING FULL ADDERS

Saradindu et al**.** *[1]* initiated the research work by proposing a full adder built by 28 transistors. There are various design styles for implementation of full adder circuit [1]. Now a day the major challenge in the VLSI technology is to reduce the chip size and power. Increasing the number of transistors does not meet the area and power requirement of the circuits. So starting from the basic conventional-CMOS

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full adder to the 8T full adder the number of transistors used for the implementation of full adder is reduced which in turn reduces the power consumption of the circuit [3].

1.2.1 Conventional -CMOS Full Adder Cell:

Conventional CMOS full adder cell utilizes 28 transistors based on standard CMOS topology. The schematic of the conventional CMOS full adder circuit is shown in figure 2. Since it requires more number of transistors to design full adder therefore the power consumption is high. This technology uses more number of PFET transistors in pull up network high which results in the increase of the input capacitance and since the PFET transistor has high delay therefore the overall delay of the adder circuit goes high.

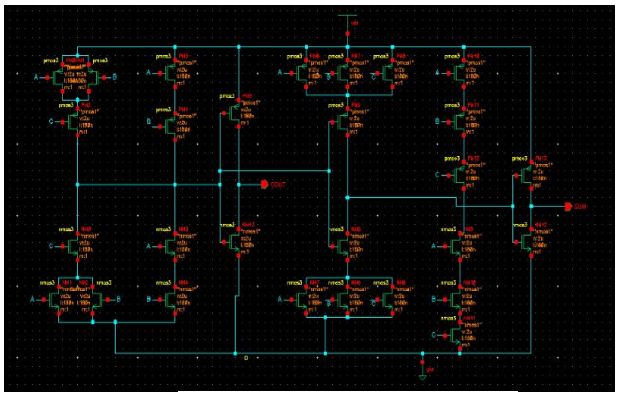

Figure 2: Conventional -CMOS Full Adder

1.2.2 Bridge style Full Adder Cell:

One of the important parameter in the circuit design is chip area so in order to reduce the chip area of full adder circuit we use bridge style full adder. In the paper [2], Authors have proposed a new style of design of full adder circuit by combining the common digital gates and majority functions. They have compared the performance of the better one with six other full adders [2]. Full adder design using bridge style consists of 26 transistors where conventional-CMOS uses 28 transistors .The number of transistors used in this design style of full adder is less than conventional-CMOS full adder, the power Consumption is low when compared with the conventional-CMOS full adder. The schematic for the bridge style full adder is shown in the figure 3.

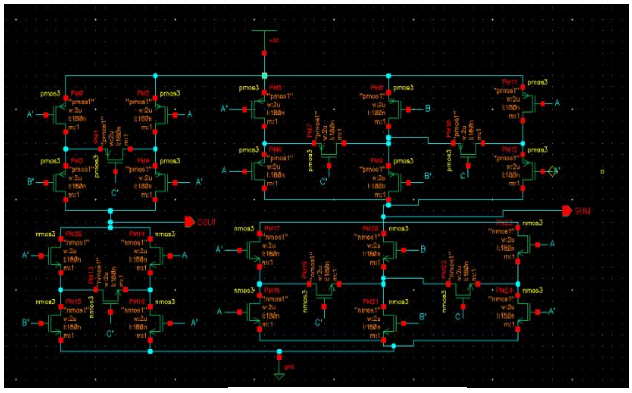

Figure 3: Bridge style Full Adder

1.3 BASIC GDI:

GDI stands for "Gate Diffusion Input". GDI cell has three inputs G, P, N and one output Y (from drain- drain connection of PMOS and NMOS). 'G' terminal is designed by combining the gate inputs of NFET and PFET. 'P' terminal is the source of PFET. 'N' terminal is the source of NFET as shown in Figure 4.

The 4 terminal GDI cell can be known as multifunctional device which performs 6 functions with different possibility of inputs N, P and G. The table shows the different combinations of inputs G, P and N and their respective outputs. Some of the outputs of the GDI cell are Boolean functions. To design these complex Boolean functions we generally need 6-12 transistors in CMOS but coming to GDI technology we need only 2 transistors to design one function. [4] .Table II shows that simple configuration.

Table II: Functions of the Basic GDI Cell

Input			output	Function
P	G	N		
B	A	0	A`.B	FUNCTION1
0	A	B	A`+B	FUNCTION2
B	A	1	A+B	OR gate
1	A	B	A.B	AND gate
B	A	C	A1.B+A.C	MUX
0	A	0	A`	NOT gate

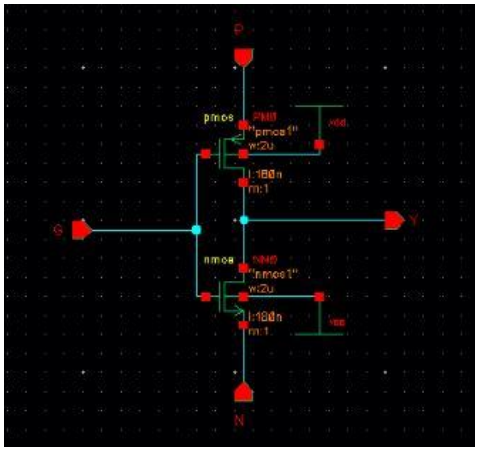

Figure 4: GDI cell

1.4 DG_GDI:

DG-GDI stands for "Double Gate-Gate Diffusion Input" in this technique we use 4 transistors to design a DG-GDI cell looks like FINFET. The sample DG-GDI cell has three inputs and one output as shown in the Figure 5. Among these 4 transistors, two are of PFET and remaining two are NFET. The sources of two PFET are combined to get the source terminal and the two sources of NFET are combined to get the source terminal of DG-GDI cell. The individual gates of PFET and NFET are tied up which is in turn connected to a common gate terminal of DG-GDI.

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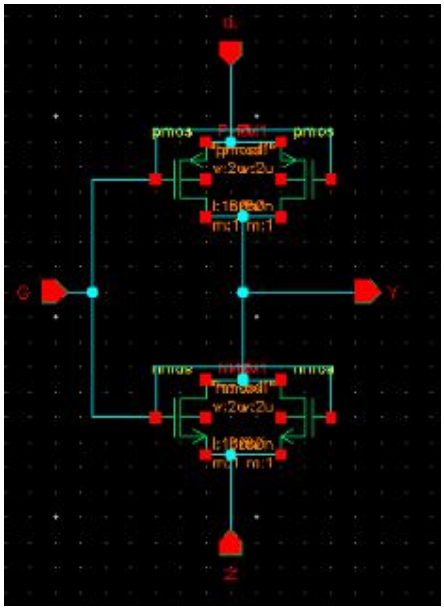

Figure 5: DG-GDI cell

1.4.1 XOR GATE using DG-GDI:

Symbol of XOR gate using GDI technology is shown in Figure 6. Functionality of XOR gate is, it gives output HIGH when both the inputs are different and gives LOW output when both the inputs are same. As shown in Table III.

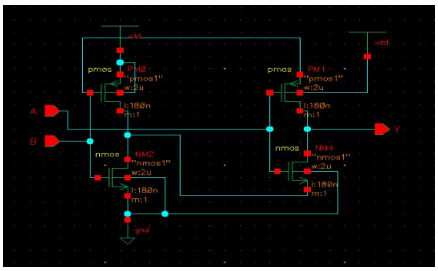

Figure 6: GDI XOR circuit

Table III XOR truth table

A	B	OUTPUT
0	0	0
0	1	1
1	0	1
1	1	0

2. PROPOSED DG-GDI SYSTEM

FA using DG-GDI:

The schematic of the DG-GDI full adder circuit is shown in the Figure 7. To design the full adder circuit in DG-GDI it requires 14 transistors

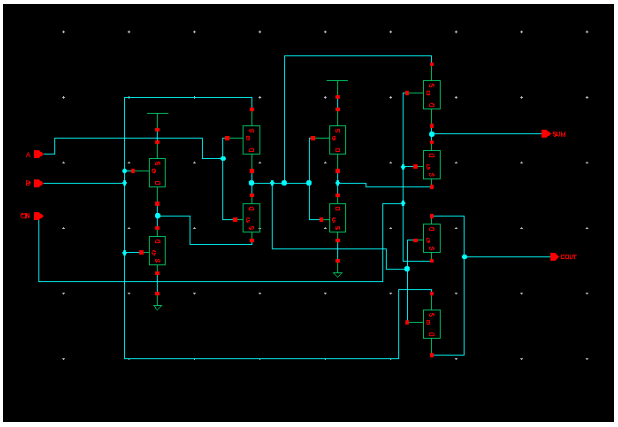

Figure 7: DG-GDI FA schematic

for design the C_OUT of DG-GDI based full adder is based on the reduced truth table for C_OUT as shown in table IV.

Table IV

A XOR B	C_out
0	B
1	C_IN

The circuit is simulated using Cadence Spectre simulator with gpdk180. It requires 1.8v as Vdd to drive all the transistors. In the simulation we observed some glitches in the output waveform as shown in figure 9. For elimination of the glitches we inserted the buffers in the circuit as shown in the figure 8.

After the simulation we found reduction in the glitches at the cost of increasing in average power.

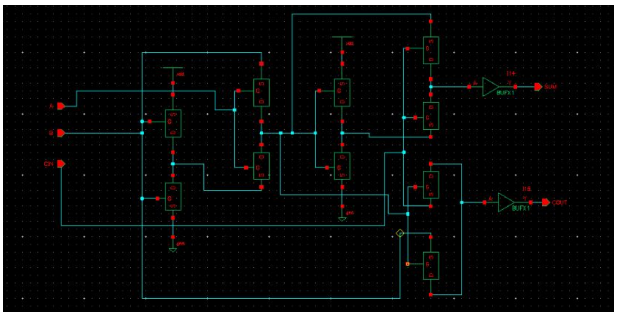

Figure 8: FA schematic with buffers

3. SIMULATION RESULTS

The technology used for designing of proposed system is gpdk180. The simulation is carried out using cadence spectre simulator. The functionality of proposed system is verified. The figure 6 shows the output of DG-GDI full adder, in this we can notice glitches for the outputs sum and carry.

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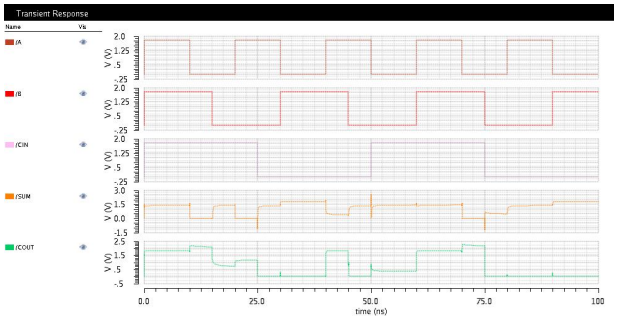

Figure 9: FA-DG_GDI-without buffer

The glitches are eliminated by insertion of buffers in the output stage and the results are shown in figure 10.

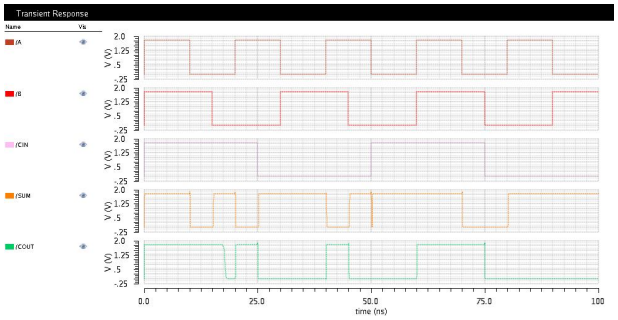

Figure 10: FA-DG_GDI-with buffer

4. Results and Discussion

The DC and transient analysis have done on the proposed system. The delays with respect to the paths i.e, any input to SUM and any input to C_OUT and the average power for the two cases are listed in the table V, table VI.

Table V: FA-DG_GDI-with buffer results

FA-DG_GDI-with buffer		
Path	Delay(ps)	Power(mW)
A-SUM	108.5	900.1
A-C_OUT	77.64	900.1
B-SUM	108.5	900.1
B-C_OUT	77.64	900.1
C-SUM	108.5	900.1
C-C_OUT	77.64	900.1

Table VI: FA-DG_GDI-without buffer results

FA-DG_GDI-without buffer		
Path	Delay(ps)	Power(mW)
A-SUM	87.13	0.03
A-C_OUT	108.3	0.03
B-SUM	87.13	0.03
B-C_OUT	108.3	0.03
C-SUM	87.13	0.03
C-C_OUT	108.3	0.03

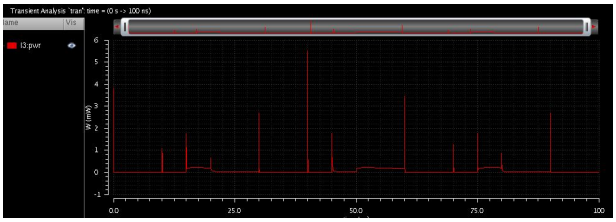

Figure 11: average power

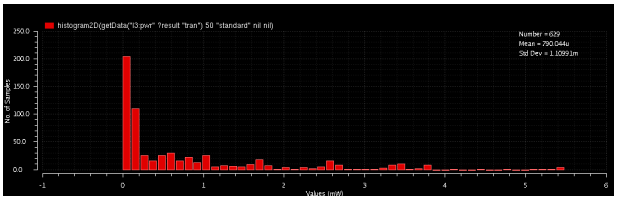

Figure 12: Histogram

5. CONCLUSION

The proposed system in the paper eliminates the glitches in the output waveforms by inserting buffers in the output circuit.

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