ISSN 2278-3091

International Journal of Advanced Trends in Computer Science and Engineering, Vol.5 , No.1, Pages : 88 -91 (2016)
Special Issue of ICACEC 2016 - Held during 23-24 January, 2016 in Institute of Aeronautical Engineering, Quthbullapur, Telangana-43, India

Low power and speed M-GDI based full adder

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Abstract: Addition is a fundamental operation in arithmetic units of calculators, ALUs Processors. For designing high complexity computation applications the speed of operation is mainly concern. These are various number of architectures exist for full adders. In this paper we are implementing Modified Gate Diffusion Input (MGDI) logic for the implementation of full adder. It uses less no. of transistors. The propagation delay, area and speed are important design metrics for the design of any circuit in VLSI. So the metrics are estimated and analyzed for GDI and MGDI full adder. The full adder circuit is implemented using Cadence tool and simulation carried-out using Spectre tool. The technology used for the implementation of the proposed system is gpdk180 technology library. The conventional adder and MGDI adder are compared in terms of power and delay. By the transient analysis of MGDI full adder circuit using cadence tool we found that the delay of proposed adder is 153.1ps with average power 1.077E-6 W.

Keywords: GDI, MGDI, Full Adder, CMOS technique, Propagation Delay, Power dissipation

1. INTRODUCTION

VLSI as abbreviated Very Large Scale Integration is a justification for integrating numerous components on a small chip area. It has been viral because of its ability of saving microchip area by minimizing the interconnect fabrics area. With the gradual increase in circuit complexity and high speed requirement in modern technology, power optimization is of utmost importance. Also, in realization of VLSI, high performance with high speed plays a predominant role. Alongside, customer's fantasy for portable electronics gave rise to small size chip, faster speeds, highly reliable and low power requirement.

Full adders that constitute the basic block of various circuitries, if implemented effectively and efficiently with high speed and low power can meet the above requirements. In each and every logic circuit, addition is a fundamental step. As such there is a need to compute logics in swift using low power and high accuracy.

1.1 FULL ADDER

Full adder performs addition between two input bits, along with the carry generated by the previous addition operation. So, for a one bit full adder, the count of input is three- i.e. two binary input bits (A, B) and a carry bit (C_in). It implements XOR operation for calculating the sum. Sum is equivalent to the XOR of all the input bits. As along the sum,Full adder generates a carry referred as C_out. As such the output of a full adder is two - Sum and C_out. The Boolean expressions for its outputs are mentioned below:

$$Sum = A \oplus B \oplus C\_in$$
$$C\_out = AB + BC + CA$$

The schematic of the full adder is shown in Figure 1.

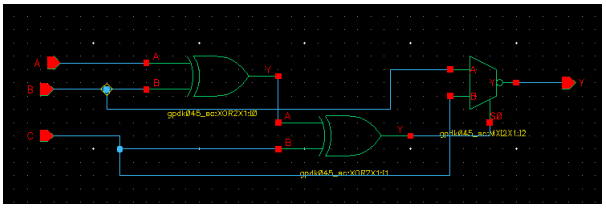

Figure 1: The schematic of Full adder

For different combinations of the input, outputs are calculated using above equations. Since we have three inputs we have eight combinations of the input to be verified for Sum and C_out. These information is stated in the truth table shown in Table I :

Table I: Truth table of Full adder

A	B	C_in	Sum	C_out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

1.2 REVIEW OF VARIOUS FULL-ADDER DESIGNS

Various designs exists to implement Full adder operation. In which two of designs Conventional CMOS (C CMOS) full adder and Bridge Style CMOS Full adder are discussed here. Saradindu et al. *[1]* initiated the research work by proposing a full adder built by 28 transistors. Also, these circuits incorporate a larger dealy thus effecting the speed and performance of the system. It is obvious that using of many transistors result in large power requirement for operation that in turn lead to high power dissipation in the form of heat.Various advanced Full adders have been evolved for designing Full adder with using few transistors to overcome the above dealy and power issues.Power and delay optimization have succesfully met when operated Full adder at different volatges [2].

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1.2.1 Conventional CMOS Full adder

C CMOS as depicted in Figure 2**,** contains twenty eight transistors that are interconnected to each other. It's a complementary CMOS circuit consuming a large chip area due to its numerous transistors count. Even it has high input capacitances due to its multiple PMOS pull up networks. Moreover, it adds to more delay and power requirement. Besides these, its advantage includes layout regularity, high noise margin and stability at low voltage.

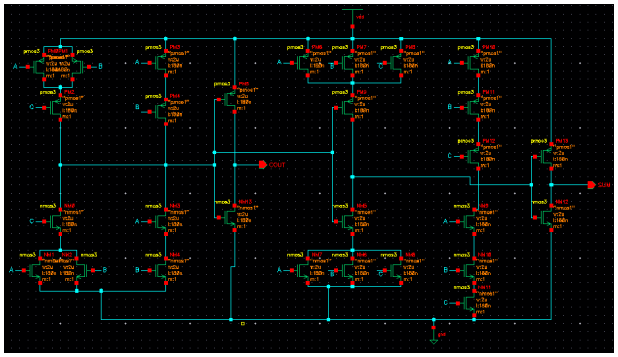

Figure : 2 C CMOS Full adder circuit

1.2.2. Bridge Style CMOS Full Adder

The Bridge Style [3] CMOS Full adder circuit constitutes twenty six transistors that is described in Figure 3. In comparison with C CMOS this design contains fewer counts of transistors. In this design, a bridge is developed between every adjacent mesh by adding a transistor [4]. The main advantage of Bridge transistors is that it paves an ultimate different path from supply line to output. Along with preserving the networks of PMOS and NMOS, these transistors as well connected to meet the accuracy of the Bridge Full adder circuit. In this style, control signals are applied at mesh sides and inputs are given at gates of the transistor. It allows simulations generation of Sum and C_out. However, chip area and power are crucial elements of the circuitry; the Bridge CMOS might not be an advised method.

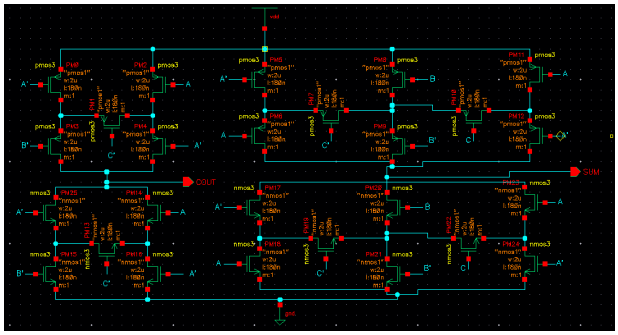

Figure : 3 Bridge Style CMOS Full adder circuit

1.3 GDI

GDI(Gate Diffusion Input) method stands out for its abitility to perform the same task as a CMOS does, reducing the transistor count, delay and power consumption thus improving the speed of the circuit. The basic GDI cell is depicted in Figure 4.As acknowledged from the figure, it has three inputs with an output pin.[4] These inputs are given at the common gate inputs of PFET and NFET (G)and at the source of both the transistors(P,N).The output are taken from the common drain point(Y).

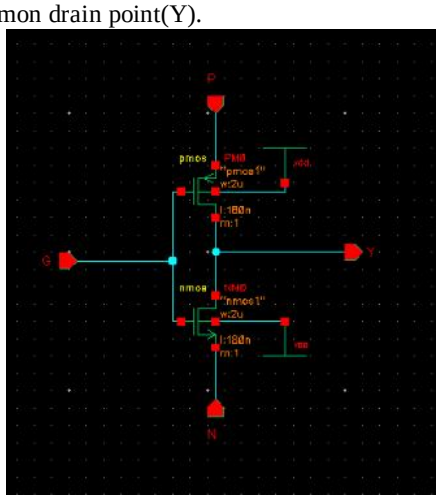

Figure 4: GDI Basic model

This 4port GDI can perform six operations, that are complex to function using CMOS, provided with various input combination that is depicted in the table below. Meantime, by combining several GDI cell, multiple-input gates can be implemented [4].

Table II: GDI Cell's different functions

Input G	Input P	Input N	OUTPUT	FUNCTION
A	B	0	A`.B	F1
A	1	B	A`+B	F2
A	B	1	A+B	OR
A	0	B	A.B	AND
A	B	C	A`.B+A.C	MUX
A	1	0	A`	NOT

1.3.1 GDI XOR

A GDI full adder carries out XOR operations. As such it need GDI XOR unit for its functioning. The GDI XOR model and truth table is as mentioned in Figure 5. It involves one inverter (using GDI unit), a PMOS, a NMOS. The drain of these transistors is connected where the output is traced. One input is given to PFET source whereas complement of other input is supplied to NFET source.

2. PROPOSED DESIGN

2.1 Full Adder using M-GDI

The proposed MGDI Full adder requires two GDI-XOR models along with a NFET and a PFET that is specified in below Figure 6. Firstly, XOR of the two input bits (A, B) is performed. The output of which is then applied as input to other XOR module along with C_in bit and to common gate input of the PMOS and NMOS.

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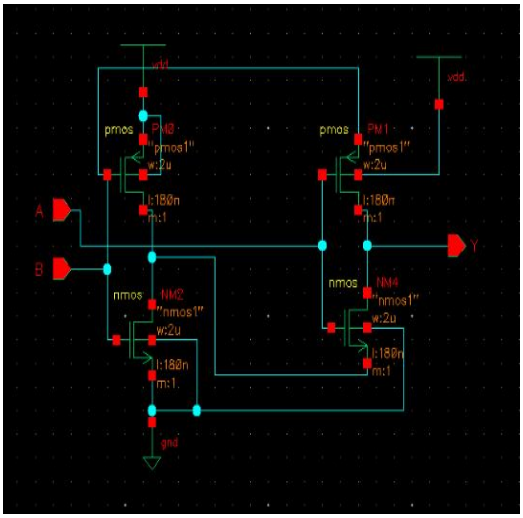

Figure 5: GDI XOR Module

Sum is generated at its output pin. Further C_in bit is supplied to source pin of NMOS and B bit is applied to NMOS source. C_out is taken at this common drain.

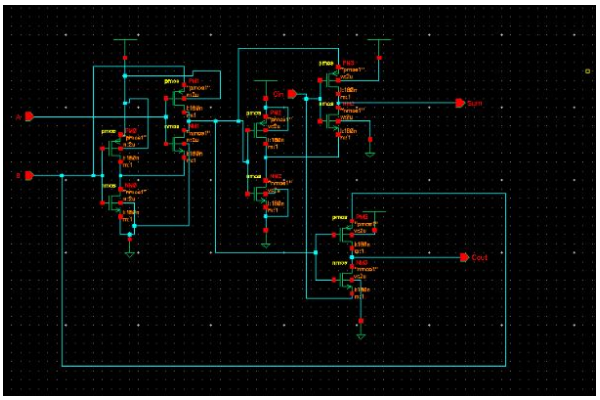

Figure 6: GDI Full adder without buffer

When MGDI Full adder is implemented without buffer, we notice glitches in the output waveforms. For overcoming these side effect buffers are included in the circuitry as shown in Figure 7.

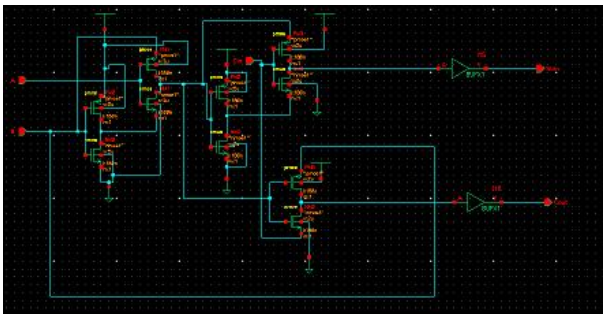

Figure 7: GDI Full adder with buffer

3. Simulation Results

For the proposed system we have utilized gpdk180 technology and implemented using cadence simulator. MGDI Full adder functionality is verified .The Figure 8 depicts its output where we find glitches in Sum and C_out.

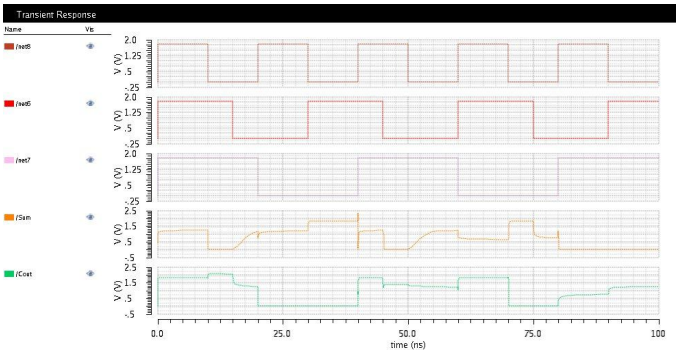

Figure 8: GDI Full adder output with buffer

As mentioned earlier to eliminate these glitches, buffers are added in the circuitry at the output pins as shown in Figure 5**.** As a result the output is glitches free as can be noticed in Figure 9.

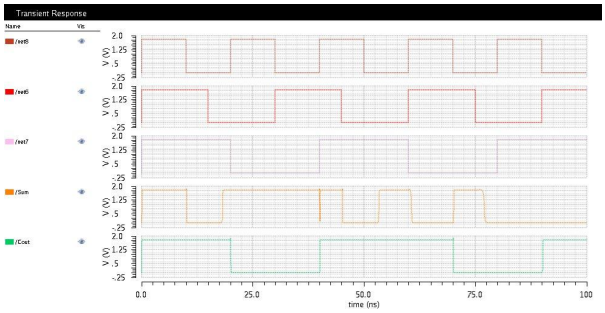

Figure 9: GDI Full adder output with buffer

4. Result and Discussions

For the proposed system DC and transient analysis have been performed. The delay of every input applied with respect to the Sum and C_out and the average power for the two cases i.e MGDI Full adder circuit with buffer and without buffer are listed in the Table III and Table IV respectively.

Table III : MGDI Full adder results with buffer

Path	Delay(ps)	Power(mW)
A to Sum	153.1	1.077
A to C_out	111.6	1.077
B to Sum	153.1	1.077
B to C_out	111.6	1.077
C to Sum	153.1	1.077
C to C_out	111.6	1.077

Table IV : MGDI Full adder results with buffer

Path	Delay(ps)	Power(mW)
A to Sum	468.84	52.56
A to C_out	33.11	52.56
B to Sum	468.84	52.56
B to C_out	33.11	52.56
C to Sum	468.84	52.56
C to C_out	33.11	52.56

The average power and its histogram are shown in Figure 10, Figure 11 respectively.

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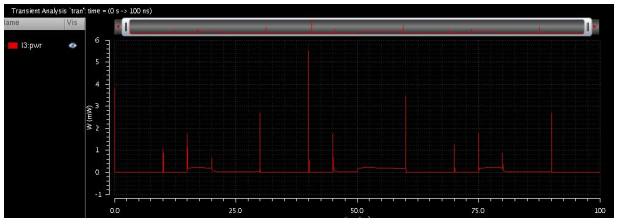

Figure 10: average power

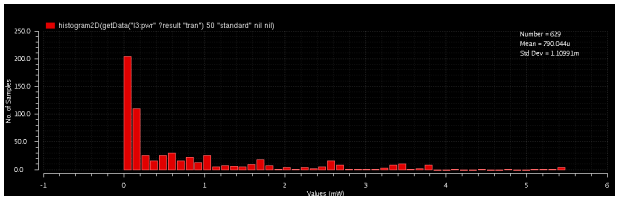

Figure 11: histogram average power

CONCLUSION

The proposed system is implemented using cadence tool (gdpk180 technology). The transient analysis of MGDI full adder circuit using cadence tool we found that the delay of proposed adder is 153.1ps with average power 1.077E-6 W. By using buffers in the circuit ,it eliminated glitches successfully

ACKNOWLEDGEMENT

The authors would like to acknowledge the Management, Director, Principal, HOD and other faculty members who helped in successful completion of this research paper.

REFERENCES

[1] Saradindu Panda, N. Mohan Kumar, C. K. Sarkar, (2009), "Transistor Count Optimization Of Conventional CMOS Full Adder And Optimization Of power And Delay Of New Implementation Of 18 Transistor Full Adder By Dual Threshold Node Design With Submicron Channel Length", International Conference On Computers And Devices For Communication, pp. 978-981.

[2] Nitasha Jaura, Balraj Singh Sidhu, Neeraj Gill, "Optimization Of Low Power Adder Cells using 180nm TG Technology", International Journal of Advanced Technology in Engineering and Science, Volume No.02, Issue No. 10, October 2014

[3] O. Kavehei, M. Rahimi Azghadi, K. Navi, A.P Mirbaha, "Design of Robust and High-Performance 1-bit CMOS Full Adder for Nanometer Design" , IEEE computer Society Annual Symposium on VLSI, ISVLSI'08, Montpellier, France, April 2008, pp.10-15.

[4] Nitasha Jaura1, Balraj Singh Sidhu2, Neeraj Gill 3," Optimization of Low Power Adder Cells using 180nm tg technology", ", International Journal of Advanced Technology in Engineering and Science www.ijates.com,Volume No.02,Issues No. 10,October 2014.

[5] 87,chapter 6,gdi based low power full adder cell for dsp data path blocks http://shodhganga.inflibnet.ac.in/bitstream/10603/13423/11/11_chapter%206.pdf

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