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Design and Implementation Of Dynamic Track and Latch Comparator Using CMOS In 0.18um Technology

Noorullah Khan
sistant Professor,ECE,
Muffakham Jah College of Engineering and Technology,
Hyderabad,Telangana,
mdnoorece@mjcollege.ac.in

Jabar Oathman,
Assistant Professor,ECE,
Muffakham Jah College of Engineering and Technology,
Hyderabad,Telangana,
jaberyemeni@gmail.com

P.Safinaz Tahseen,
Student,ME,ECE,
Muffakham jah College of engineering and technology,
Hyderabad,Telangana
safinaz.papabhai@gmail.com

Abstract— **This paper describes the design and implementation of a dynamic track and latch comparator circuit. It includes a latch, buffers and differential amplifier. The comparator is used in pipeline ADC is a dynamic latch based comparator. The comparator consumes very low static power and operates at high frequencies of MHz's. The dynamic comparator with differential input and output is suitable to reduce the area and power consumption of ADC, due to large use of comparators in ADC. This comparator doesnot need multiple clocks or inverted clocks instead one clock signal is sufficient to trigger transition from one phase to another and back again. It is being implemented in 180nm CMOS Technology. The simulation results of Dynamic track and latch comparator is done in Cadence environment.**

Keywords — **Dynamic Track and Latch Comparator, Differential Amplifier, Latch, Buffers.**

INTRODUCTION

The second most widely used electronic components after amplifiers are comparators. A comparator is used to detect if a signal is greater or smaller than zero, or to compare the size of one signal to another. They also find wide spread use in many other applications such as data transmission, switching power regulators and others. The high speed comparators typically have one or two stages of pre-amplification followed by the track- and- latch- stage as shown in figure1[1].

The preamplifier used to obtain higher resolution and to minimize the effects of kickback .The output of pre-amplifier although larger than the comparator input , it is still much smaller than voltage levels needed to drive digital circuitry. The track-and-latch-stage reduces the total number of gain stages even when good resolution is needed. Pre-amplifier does not have gains more than 10 and speed is limited. It is simply used as a unity gain buffer so it is eliminated in the proposed dynamic track and latch comparator. The proposed architecture involves the differential amplifier and the latch circuitry.

DIFFERENTIAL PAIR AMPLIFIER

A differential amplifier is a circuit that can accept two input signals and amplify the difference between those input signals. It provides high voltage gain and high common mode rejection ratio. It requires very low input bias current, very low offset voltage and very high input.The above proposed comparator circuit consists of total 9 The above proposed comparator circuit consists of total 9 (4 pmos and 5 nmos) transistors.

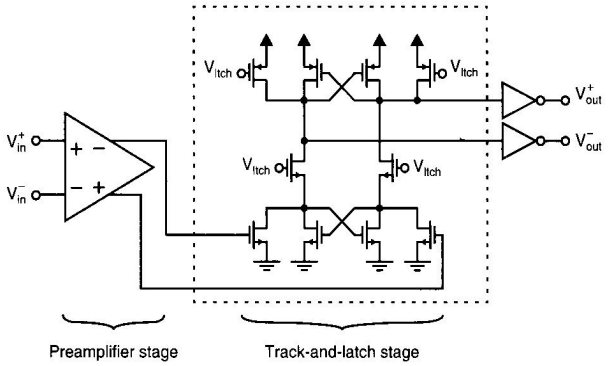

Fig 1: Dynamic Track and Latch Comparator using Pre-amplifier[1].

Differential amplifier can operate in two modes which are differential mode and common mode .The common mode gives result of output zero while differential mode gives result of high output, hence this amplifier has the common mode rejection ratio. If two voltages are equal, then differential amplifier gives an output voltage of almost zero volt and if two input voltages are not equal differential amplifier gives the high output voltage.

The differential amplifier has been shown in figure 2. MOSFET M1 and M2 from fig2 formed differential amplifier pair. MOSFET M5 is a current sink which provides bias current to the amplifier. MOSFET M3 and M4 together form a current mirror. Assuming that all transistors are in saturation region. The Bulk of all transistors connected to their sources. The current flowing through transistor M5 is divided into two equal parts and flows through M1, M3 and M2, M4 respectively. Transistor M3, M4 connects to the VDD supply, whereas transistor M5 connected to VSS.

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The differential amplifier output can be described as

$$V_{out} = A(V_{in}^{+} - V_{in}^{-})$$

where A is the gain of the amplifier. [1]

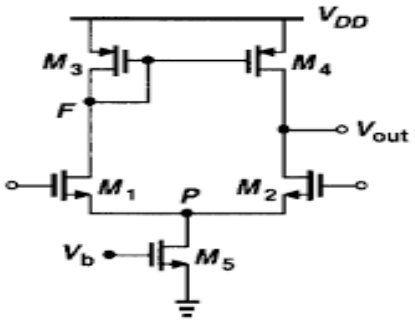

Fig 2 : Differential Amplifier

DYNAMIC TRACK AND LATCH COMPARATOR

The fundamental circuit often is a latch , which consists of two inverters, where each output is connected with the input of the other(cross-coupled inverters) [7]. The schematic of the latch-type comparator is given in Fig 3. The operation of the comparator begins when the V_{latch} is low; the two output nodes (Von & Vop) pre-charge fully to digital 1 level (3.3V) and the lower NMOS cross-couple circuit is disconnected from the upper part by the NMOS switches in this phase. This simplified principle is similar to Fig 3.

When the V_{latch} is high, the upper pre-charging switches open and stop pre-charging, the lower NMOS discharging circuit starts its operation. The comparison is made by comparing the rate of discharging the output node(V_{on} & V_{op}).

When Vin+ input has a higher voltage than another input, the rate of the voltage drop at node V_{op} is faster than that at node V_{on} due to the larger current flow at M1. This generates an imbalance voltage which is further enhanced by the regenerative action of the Cross-couple NMOS and PMOS pairs. Thus their voltage difference at the two outputs of the comparator is further diverged to V_{dd} and gnd respectively.

The above proposed comparator circuit consists of total 9 (4 pmos and 5 nmos) transistors. The widths and lengths of each of these transistors is shown in table I.

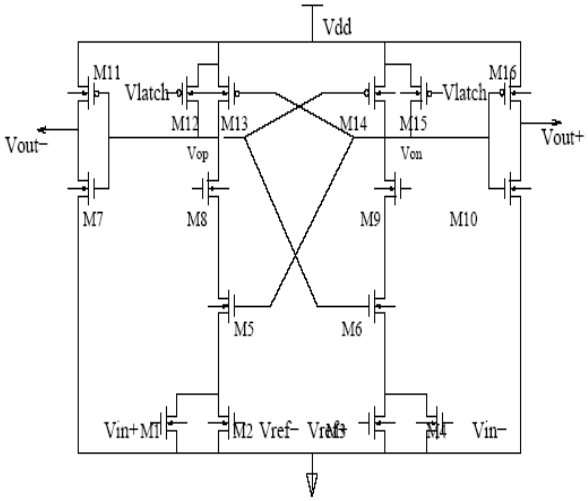

Fig 3: Dynamic track and latch schematic

SIMULATION RESULTS

The simulation of the fig3 dynamic track and latch comparator circuit has been simulated in the cadence tools environment. The simulation of the test bench of comparator shown in fig4 has been obtained in the virtuoso simulation window in fig 5.The fig5 depicts the transient response of the track and latch dynamic comparator functionality.

The comparator operates in both the track and latch phases as per the operation mentioned earlier. The simulations are performed on the 10KHz frequency of input signal. The fully differential output obtained is summed to get overall output as shown in fig7.The operation of comparator can also be explained using input ramp signals.

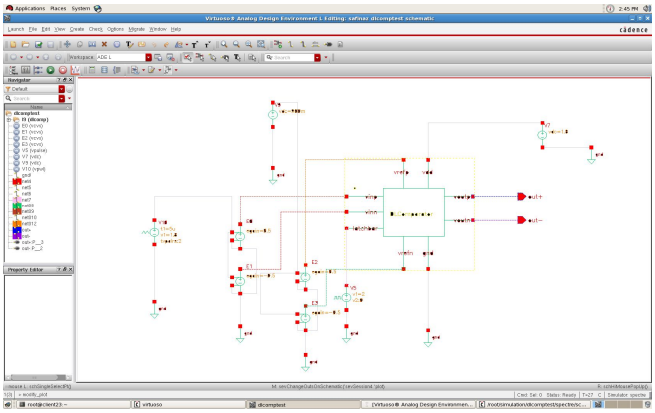

Fig 4: Dynamic Comparator test bench schematic

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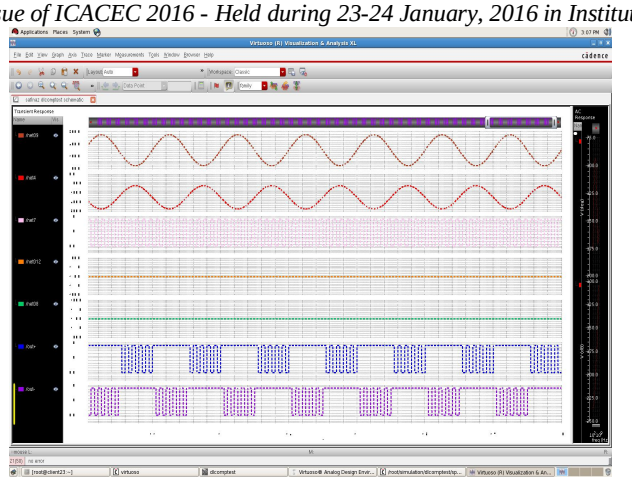

Fig 5:Dynamic comparator Simulation result

The two differential input signals when fed to the dynamic Track and Latch Comparator in the fig 5 the output gets pre-charged to high voltage 1v whenever the latch bar input is low. The comparator generates the compared output of both the signals with respect to the reference signals whenever the latch bar input is high [2].

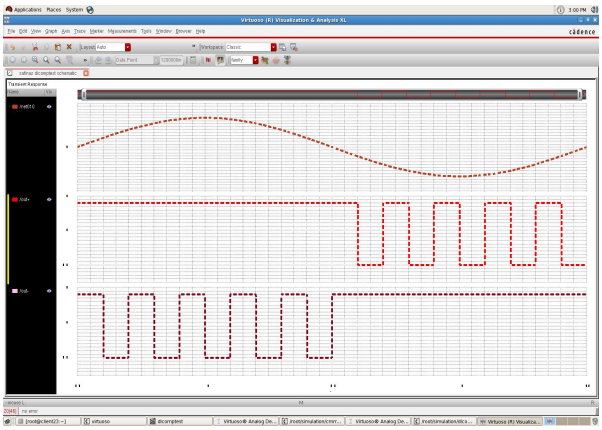

Fig 6: Dynamic Comparator differential output waveforms

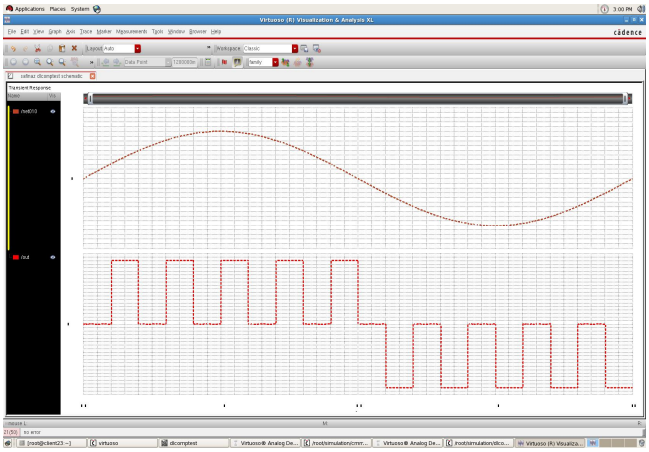

Fig 7:Dynamic Comparator overall Output

The positive output in the fig6 represents the pre-charged output during the positive cycle of input and the latched output during the negative input cycle. Similarly during the positive input cycle the negative output gives the latched output and the pre-charged output during the negative input cycle.

CONCLUSION

The Dynamic track and latch circuit has been implemented in cadence tools of 180nm technology. The design is made for input sinusoidal signal of 500mV and the frequency of 10KHz.It can be used for even frequencies till 100MHz.The given comparator has very low offsets of the order of few tens of mill volts at maximum. The comparator consumes static power of only few hundred nanowatts . The simulation results are obtained to have met the functionality of the dynamic track and latch comparator.

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