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EFFECTIVE OPTIMIZING DATA ENCODING SCHEMES FOR REDUCING ENERGY CONSUMPTION IN N-O-C

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***Abstract*— The power dissipation of links of network on chip increases as the technology going to reduce. This power dissipation is even larger than other elements of communication subsystem like router and network interface. Here, in this paper we represent three different data encoding schemes which are helpful for reducing power dissipation by links of network on chip. The proposed system gives reduction in dynamic power dissipation by reducing coupling switching activity and self switching activity when compared to previous system. Also, the proposed scheme does not need any type of modification of the routers and link architecture. Using this, power dissipation and energy consumption will be reduced without any significant performance degradation.**

KEYWORDS: Data encoding; coupling switching activity; network-on-chip (NoC); low power, power analysis.

1.INTRODUCTION

Semiconductor technology to nanometer technology, power required became a critical factor in digital system. Network on chip is a communication subsystem on integrated circuit between IP cores in a system on a chip (SOC). NoC technology is a implied method for on-chip communication and performed by conventional bus and crossbar interconnections. The next few years many cores on a single chip can be possible. In digital design, static power is device consumption power and dynamic power is consumed during digital data transition. For low-power design, the signal switching activities have to be reduced. This paper focus on reducing link power consumption. In literature survey we properly summarize some of the works in the area and link power reduction. Shielding [1], increasing line to-line spacing [8] and repeater insertion [2] these are some methods. But all these methods face the problem of large area. The encoding of data before injecting it to the network is another way to reduce the power consumption. The data encoding technique are broadly categorize into two. The first category focuses on reduction of coupling switching activity and avoids the dissipation of power. Bus invert [BI], INC-XOR these are proposed methods used for random patterns of data transmission via lines. While, gray code, T0, working-zone encoding, and T0-XOR are methods for correlated data patterns. Out of total interconnects capacitance if the coupling capacitance is a major part network on chip (NoC) design example is recognized as the most featured way to solve the scalability and variability problems as defines the ultra deep submicron meter era. As the design complex increases, the total length of the interconnection wires enlarged which results in long transmission delay and high power consumption. In practical, the power dissipated by the network links is as large as the dissipated by network interfaces and routers and it will increase in next future nodes as technology scales. In particular, represent different designs of encoders which operated at flit level and worked on end-to-end basis, these make it easier to decrease both the switch activity as well as the coupling switching activity on links of the routing paths followed by the packets. We focus on data encoding schemes as another way to reduce dissipation of power by the links of network. The basic thought is to just encode the data before they injected in the network in such a way that it will reduce the switching activity of the links. In Silicon area, reduction in power and energy are the parameters are taken into consideration for analysis. The results showed by using this proposed encoding schemes power and energy can be saved**.**

2.RELATED WORK

The Several data encoding techniques have been proposed in literature for low power consumption. The demand of chips is increasing every years. In the then this category of encoding is not applicable for deep sub-micron meter technology nodes. Second category focus on reducing power dissipation caused by the coupling switching. Power effective Bus Invert come under this category. It presented a method based on Odd/Even Bus-Invert techniques. The coupling capacitances between on-chip bus lines become dominant in deep-submicron meter technologies. Coding to reduce the switching activity of the individual lines was enough to reduce power on buses in older technologies, but new coding techniques that reduce the coupling activity between lines are needed for deep-submicron buses. A coding technique that reduces the coupling switching activity by taking the advantage of end-to-end encoding for wormhole switching has been presented in “Data encoding schemes in networks on chip” [5]. It is based on lowering the coupling switching activity by eliminating only Type II transitions.

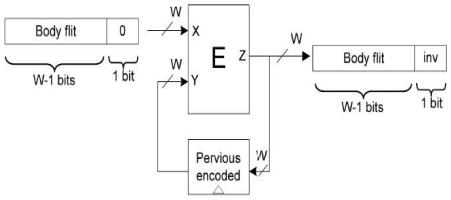
3.Proposed method

The proposed method suggest to encode flits before sending them into the network. Because of self-switching and coupling switching activity link power is more dissipated. In this project, there is end-to-end scheme, means flits which passes through the links of the routing path are encoded first at network interface [6]. Encoder and decoder block are added at network interface level. The encoder encodes all the outgoing flits of the packet except header flit so that power dissipation in path of inter router is getting reduced [6]. This encoding technique is proposed to reduce power dissipation by minimizing both, self and coupling switching activities on the links of interconnected network. In this paper, three encoders are designed using three different.

TABLE I. Change of transition types on effect of odd inversion

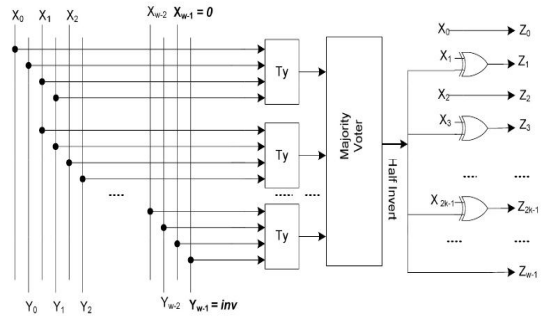
Time	Normal			Odd Inverted		
	Type I			Types II, III, and IV		
$t-1$	00, 11	00, 11, 01, 10	01, 10	00, 11	00, 11, 01, 10	01, 10
t	10, 01	01, 10, 00, 11	11, 00	11, 00	00, 11, 01, 10	10, 01
	T1*	T1**	T1***	Type III	Type IV	Type II
$t-1$	Type II			Type I		
t	01, 10			01, 10		
	10, 01			11, 00		
$t-1$	Type III			Type I		
t	00, 11			00, 11		
	11, 00			10, 01		
$t-1$	Type IV			Type I		
t	00, 11, 01, 10			00, 11, 01, 10		
	00, 11, 01, 10			01, 10, 00, 11		

Type I and Type II transitions are the main cause of dynamic power dissipation. So, in scheme I we reduce type I transitions while in scheme II we reduce both type I and type II transitions and decide whether half invert or full invert operation has to be performed. And at last, in type III decision is made by different behaviors of type I transition which shows which operation is better odd or even invert. The encoder architecture in Figure. 1 for scheme 1, scheme 2 and scheme 3 is same. The encoder block gets w-1 bit as one of the input and previous encoded output is another input. Then comparison is done between these two inputs by encoder block and then any one of the inversion operation is performed based on the transition types.



"Figure 1 Encoder architectur

4.SCHEME I

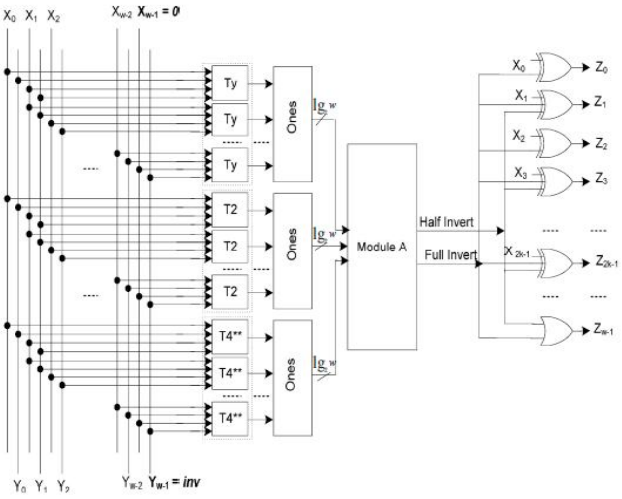


"Figure 2, Encoder block internal view scheme I"

In scheme I, we concentrate on minimizing the number of Type I transitions (by transforming them into Types III and IV transitions) and Type II transitions (by transforming them into Type I transition). As in figure 2 The scheme compares the current data with the previous one to decide whether odd inversion or no inversion of the current data can lead to the link power reduction. If the flit is odd inverted before being transmitted, the dynamic power on the link is where T0→1, T1, T2, T3, and T4 are the self-transition activity, and the coupling transition activity of Types I, II, III, and IV respectively. This is the condition used to determine whether the
odd inversion has to be performed or not

$$T_y > \frac{\omega - 1}{2}$$

5.SCHEME II



"Fig 3. Encoder block internal view scheme II"

. Encoder block internal view figure 3 scheme II Here, in this proposed encoding scheme, we utilize both odd as well as full type of inversion. In full inversion operation, there is conversion of Type II transition into Type IV transition. There is comparison made of current data with the previous data and after that decision will be made to convert current data into odd, full or no inversion. So that finally, we will get least power dissipation. The previously encoded body flit is show by the wth bit in that, inv which tells if odd or full inversion operation is done (inv = 1) or left as it was (inv = 0). Now, indicate P, P' and P" for the power dissipation by the link at a time when the flit is transmitted with no inversion, odd and full inversion, respectively. Power reduction occur in odd inversion condition when P' < P and P' < P",

odd inversion condition is obtained as

$$2(T_2 - T_4^{**}) < 2T_y - \omega + 1,\ T_y > \frac{\omega - 1}{2}$$

the full inversion condition is obtained

$$2(T_2 - T_4^{**}) > 2T_y - \omega + 1,\ T_2 > T_4^{**}$$

If above mentioned conditions are not satisfied then no inversion will be performed.

6. SCHEME III

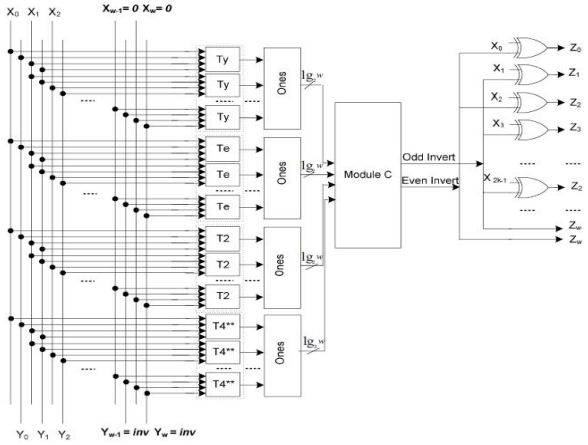


Figure 4. Encoder block internal view scheme III

Encoder block internal view figure 4 scheme III encoding architecture,for the even invert condition ,full invert condition and the odd invert condition ωth bit of the previously encoded body flit is indicated by inv as shown in figure 4 if it was even, odd, or full inverted (inv = 1) or left as it was (inv = 0). first stage of the encoder determines the transition types while the second stage is a set of one's (1) count number of ones in their inputs.

Table II. Change in Transition types on effect of even inversion

Time	Normal			Even Inverted		
	Type I			Types II, III, and IV		
$t-1$	01, 10	00, 11, 01, 10	00, 11	01, 10	00, 11, 01, 10	00, 11
t	00, 11	10, 01, 11, 00	01, 10	10, 01	00, 11, 01, 10	11, 00
	T1*	T1**	T1***	Type II	Type IV	Type III
$t-1$	Type II			Type I		
t	01, 10			01, 10		
	10, 01			00, 11		
$t-1$	Type III			Type I		
t	00, 11			00, 11		
	11, 00			01, 10		
$t-1$	Type IV			Type I		
t	00, 11, 01, 10			00, 11, 01, 10		
	00, 11, 01, 10			10, 01, 11, 00		

Full inversion Condition is

$$2(T_2 - T_4^{**}) > 2T_y - \omega + 1,\ (T_2 > T_4^{**})$$

$$2(T_2 - T_4^{**}) > 2T_e - \omega + 1$$

odd inversion condition is satisfied when

$$,2(T_2 - T_4^{**}) < 2T_y - \omega + 1, T_e > \frac{\omega - 1}{2}$$

$$T_e < T_y$$

When none of condition is satisfied, no inversion will be performed.

7.RESULTS

Tools implemented of proposed encoding schemes

1.Xilinx ISE

2.Modelsim XE

3.Power calculation in Xilinx ISE

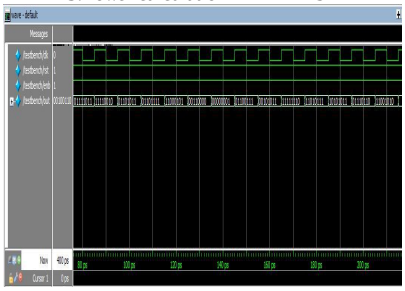


Figure 5.Simulation results of Scheme I in modelsim

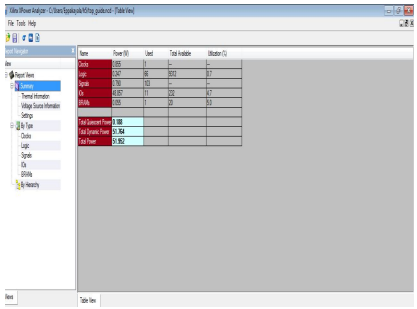


Figure6.Power report scheme I in xilinx ise

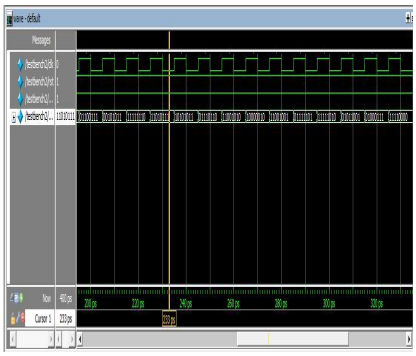


Figure.7. Simulation results of scheme II in modelsim

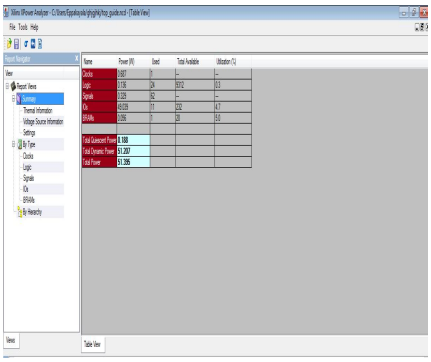


Figure 8. power report scheme II in xilinx ise

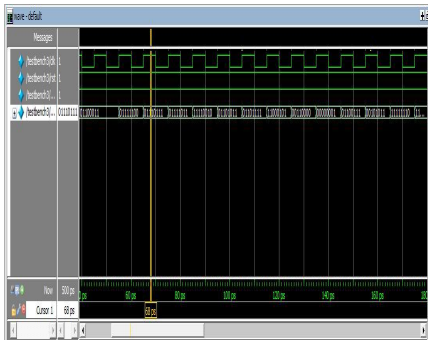


Figure 9.Simulation results of scheme III in modelsim

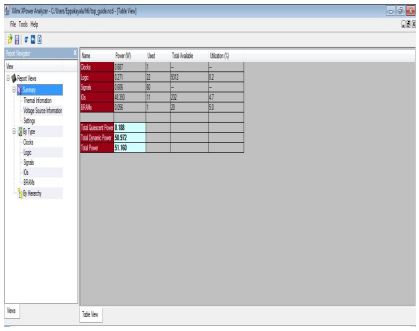


Figure 10. power report of scheme III in xilinx ise

Table III. Power comparisons between three schemes

Methods used	Total Power	Dynamic power
SCHEME I	51.952mW	51.764mW
SCHEME II	51.395mW	51.207mW
SCHEMEIII	51.160mW	50.972mW

Above comparisons between schemes I,II,III encoding schemes which reduced no. of transition from scheme I to scheme II and scheme II to scheme III terms reduces power consumption as well as area also

8. CONCLUSION

In this paper, three data encoding schemes are presented. The aim of this scheme is to reduce power dissipation by links of NoC. Because link is mainly responsible for dynamic power dissipation. And its contribution will increase in future nodes. So, when compared with previous encoding schemes in literature, proposed scheme reduces both activities, switching as well as coupling switching in deep sub micrometer technology. The encoders implementing the proposed schemes have been accessed in terms of power dissipation.

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