ISSN 2319 - 6629
Volume 1, No.1, August- September 2012
International Journal of Wireless Communications and Networking Technologies
Available Online at http://warse.org/pdfs/ijwcnt03112012.pdf

Design of Direct CPSFF Flip-Flop for low power Applications

K.Suryanarayana Raju [1], D.Mahesh Varma[2] , Y.R.K.Parama Hamsa[3]
[1]PG Student, Kakinada Institute Of Engineering & Technology, Kakinada, A.P, India. pjrece@gmail.com
[2]Assistant Professor, Kakinada Institute Of Engineering & Technology, Kakinada, Andhra pradesh, India
[3]Associate Professor, Sri Sunflower College Of Engineering & Technology, Machilipatnam, A.P.,India

ABSTRACT

Low power flip-flops which plays a vital role for the design of low-power digital systems. Flip flops and latches consume a large amount of power due to redundant transitions and clocking system. In addition, the energy consumed by low skew clock distribution network is steadily increasing and becoming a larger fraction of the chip power. Almost, 30% - 60% of total power dissipation in a system is due to flip flops and clock distribution network. In order to achieve a design that is both high performances while also being power efficient, careful attention must be paid to the design of flip flops and latches. We survey a set of flip flops designed for low power and High performance.

Keywords: Flip Flop, Low Power, CMOS Circuit.

1. INTRODUCTION

In the past, the major concerns of the VLSI designer were area, performance, cost and reliability. Power consideration was mostly of only secondary importance. In recent years, however, this has begun to change and, increasingly, power is being given comparable weight to area and speed considerations. One of the important factors is that excessive power consumption is becoming the limiting factor in integrating more transistors on a single chip or on a multiple-chip module.

Unless power consumption is dramatically reduced, the resulting heat will limit the feasible packing and Performance of VLSI circuits and systems. Most of the current designs are synchronous which implies that flip-flops and latches are involved in one way or another in the data and control paths. One of the challenges of low power methodologies for synchronous systems is the power consumption of the flip-flops and latches. It is important to save power in these flip-flops and latches without compromising state integrity or performance.

Power Consumption is determined by several factors including frequency f, supply voltage, data activity, capacitance, leakage and short circuit current.

circuit power which is caused by the finite rise and fall time of input signals, resulting in both the pull up network and pull down network to be ON for a short period

$$P_{short\ circuit} = I_{short\ circuit} * Vdd.\ P_{leakage}$$

is the leakage power. With supply voltage scaling down, the threshold voltage also decreases to maintain performance. However, this leads to the exponential growth of the subthreshold leakage current.

$$P_{leakage\ current} = I_{leakage\ current} * Vdd.$$

Based on the above factors, there are various techniques for lowering the power consumption shown as follows: In Double Edge Triggering, Using half frequency on the clock distribution network will save approximately half of the power consumption on the clock distribution network. However the flip-flop must be able to be double clock edge triggered. Double clock edge triggering method reduces the power by decreasing frequency. Using a low swing voltage on the clock distribution network can reduce the clocking power consumption since power is a quadratic function of voltage. To use low swing clock distribution, the flip-flop should be a low swing flip- flop. The low swing method reduces the power consumption by decreasing voltage.

There are two ways to reduce the switching activity: conditional operation (eliminate redundant data switching: conditional capture flip-flop (CCFF)) or clock gating, conditional discharge flip-flop (CDFF). In Conditional Operation, there are redundant switching activities in the internal node. When input stays at logic one, the internal node is kept charging and discharging without performing any useful computation. The conditional operation technique is needed to avoid the redundant switching. In Clock Gating, when a certain block is idle, we can disable the clock signal to that block to save power. Both conditional operation and clock gating methods reduce power by decreasing switching activity.

2. LOW POWER FLIP FLOP DESIGN SURVEY

There are three source of power dissipation in digital complementary metal-oxide-semiconductor (CMOS) circuit. That is static power dissipation, dynamic power dissipation and short circuit power dissipation. Dynamic and short circuit power dissipation fall under the category of Transient Power

Dissipation. Static power dissipation is due to leakage currents.

$$P = P_{dynamic} + P_{short\ circuit} + P_{leakage} \quad (1)$$

Dynamic Power is also called as switching Power. It is caused by continuous charging and discharging of output parasitic capacitance. Short circuit power is the result when pull up and pull down network will conduct simultaneously. Leakage power dissipation arises when current flow takes place from supply to ground in idle condition. Power consumption is directly proportional to supply voltage, frequency and capacitance.

3. LOW POWER FLIP FLOP DESIGN TECHNIQUES

There are many low power techniques available to reduce the flip flop power like Low swing Voltage, Conditional operation, Double Edge triggering, Clock gating, Dual Vt/MTCMOS, Proposed Pulsed flip flop and Reducing the capacity of clock load etc. In this paper the Removal of noise coupling transistor, Double Edge triggering and SVL methods is used for proposed flip flops to reduce the total power consumption because, it can be easily incorporated in new flip flop.

4. DIRECT DATA CLOCKED PAIR SHARED FLIP FLOP

This is the first proposed flip flop called DDCPSFF. The noise coupling transmission gate, N5 and output inverters I2 and I4 is removed in CPSFF. The data is applied to N1directly, instead of applying through the transmission gate, named as Direct Data Clocked Pair Shared Flip Flop. So the power consumption is reduced than the CPSFF. Compared to a static D-flip-flop, the absence of feedback loops leads to an increase in speed. The data signal does not need to overwrite nodes.

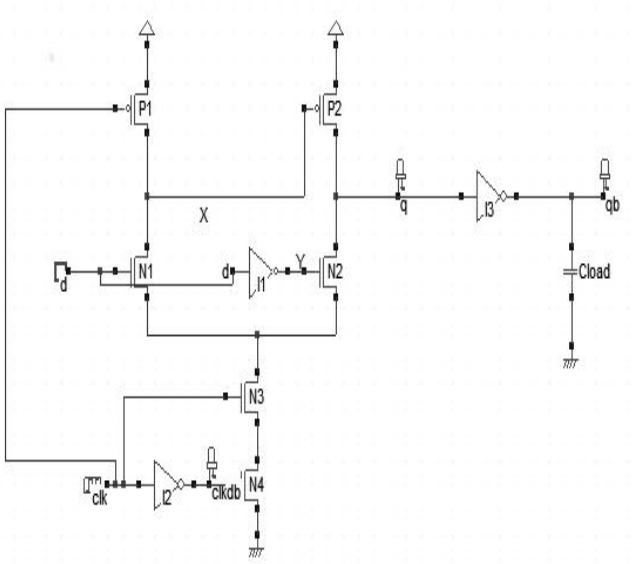


Figure 1: Direct Data Clocked Pair Shared Flip Flop

Feedback-inverters are also writing to this, holds only for circuits where the feedback cannot be disconnected by clocked transmission gates. However, these disconnecting transmission gates lengthen the feedback path and require proper clocking to turn off immediately. The schematic of DDCPSFF is shown in the Figure 1. The total number of transistor is twelve and number of clocked transistor is four. So it will lead to 37% of transistor reduction than CPSFF. If the number of transistor is reduced the power consumption is also reduced.

Whenever clk and clkdb is high the output follows the input. If d=1 and clk=0, the node X pre-charge to vdd through the P1, i.e. the node X act as a capacitor. This phase is called pre-charging phase. Then d=1 and clk=1, the MOSFET N1, N3, N4 is switched ON and P1 is Switched OFF and P2 is ON, the node X is discharged to GND. Then q=1. This phase is called evaluation phase. The analysis is extended to other input combination in the same manner. The glitches are reduced in this flip flop. Simulated results will be explained in the below Section.

4.1 Double Edge Triggered DDCPSFF

In double edge triggering flip flop the number of clocked transistor is high than single edge triggering flip flop. This method is preferable to the circuits which consist of reduced number of clocked transistors. In dual edge triggering the flip flop is triggered in both edges of clock pulses. So the half of the clock operating frequency is enough and it will reduce the power consumption.

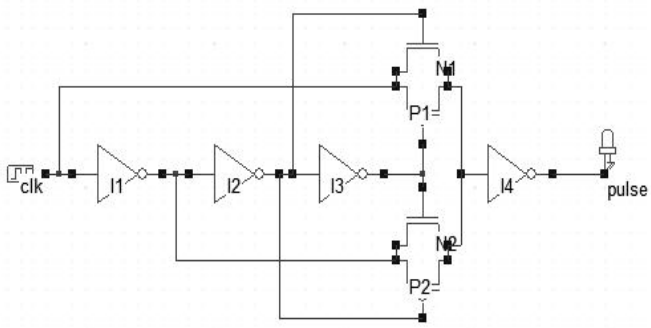


Figure 2: Dual Pulse Generator Circuit

Instead, applying the clock signal to the flip flop the dual pulse is applied using dual pulse generator scheme shown in Figure 2. The flip flop will evaluate the output in both edge of the clock.

4.2 Dual Pulse Generator Circuit

The pulse generator consists of two transmission gates and four inverters shown in Figure 3. When clk=1 the upper TG is ON and lower TG if OFF the output pulse=0. When the clk

transit from 1 to 0 suddenly the pulse=1. That is the output of the invertor I3 is '1' after three inverter delay. Similarly, When clk=0 the lower TG is responsible to produce the pulse at negative edge of the clock.

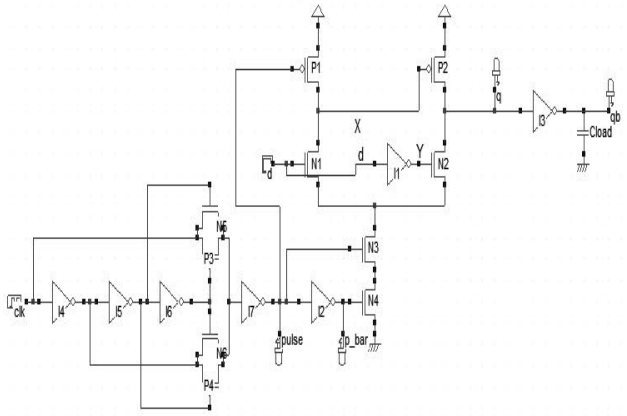


Figure 3: Schematic of DET-DDCPSFF

The pulse generator is interfacing with the DDCPSFF flip flop we get the second proposed flip flop called double edge triggered direct data clocked pair shared flip flop (DET-DDCPSFF) as shown in Figure 3. The pulse generator circuit is the external circuit it may drive one or more flip flop. Whenever the pulse is high the q output follows the d input. The pulse is applied to the input of the inverter I2 instead of clock. The working principle is same as the DDCPSFF.

5. CLOCKED PAIR SHARED FLIP FLOP

This low power flip flop is the improved version of Conditional Data Mapping Flip flop (CDMFF). It has totally 19 transistors including 4 clocked transistors as shown in Figure 1. The N3 and N4 are called clocked pair which is shared by first and second stage. The floating problem is avoided by the transistor P1 (always ON) which is used to charge the internal node *X*. This flip flop will operate, when clk and clkdb is at logic '1'. When D=1, Q=0, Qb_kpr=1, N5=OFF, N1=ON, the ground voltage will pass through N3, N4 and N1 then switch on the P2. That is Q output pulls up through P2. When D=0, Q=1, Qb_kpr=0, N5= ON, N1= OFF, Y=1, N2= ON, then Q output pulls down to zero through N2, N3 and N4.

The flip flop output is depending upon the previous output Q and Qb_kpr in addition with clock and data input. So the initial condition should be like when D=1 the previous state of Q should be '0' and Qb_kpr should be '1'. Similarly when D=0 the previous state of Q should be '1' and Qb_kpr should be '0'. Whenever the D=1 the transistor N5 is idle, Whenever the D=0 input transmission gate is idle.

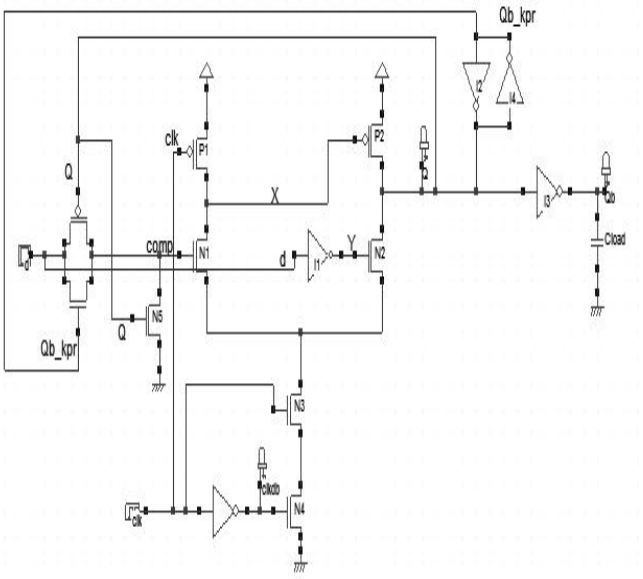
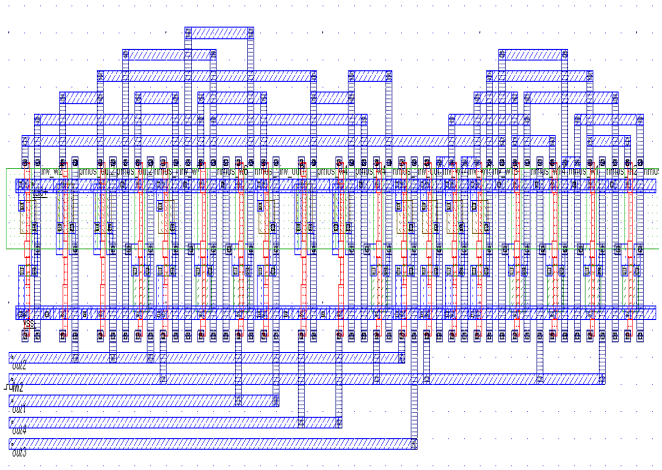
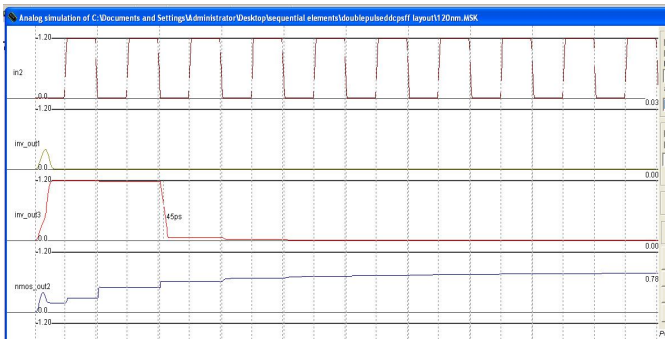


Figure 4: Clocked Pair Shared Flip Flop

In high frequency operation the input transmission gate and N5 will acquire incorrect initial conditions due to the feedback from the output. The noise coupling occurred in the Q output due to continuous switching at high frequency. The glitch will be appearing in the Q output. It will propagate to the next stage which makes the system more vulnerable to noise. In order to avoid the above drawbacks and reduce the power consumption in proposed flip flop, we can make the flip flop output as independent of previous state. That is without initial conditions and removal of noise coupling transistors. In addition double edge triggering can be applied easily for power reduction to the proposed flip flop. It will be a less power consumption than other flip flops.

6. SIMULATION RESULTS





7. CONCLUSION

We conclude this paper by outlining an important set of guidelines which are the corner stone for low power flip-flop design methodology and low power flip-flop simulation .In general, low power design for combinational and sequential circuits is an important field and gaining more importance as time goes by and will stay an important area of research for a long time. We have presented a survey and evaluation of low-power flip-flop circuits. Our experimental results enabled us to identify the power and performance trade-offs of existing flip-flop designs.

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