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A Pipelined Implementation of OFDM for Wireless LAN

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***Abstract*— The Orthogonal Frequency Division Multiplexing (OFDM) is a parallel transmission scheme. It has attained the high data rate by splitting the data stream into a number of low-rate sub-carriers (SC) instead of utilizing one carrier at a high rate. OFDM have been around 1960s.This technique is mainly used in digital audio/video broadcast (DAB/DVB), wireless LAN (802.11a and HiperLAN2) and broadband wireless (802.16). In this design, the pipelined implementation of OFDM model is designed and its used in Wireless LAN IEEE 802.11a. The aim of this work is to implement the digital baseband part of the physical layer of an OFDM transmitter that conforms to the IEEE 802.11a standard. In this work, the VHDL is used to implement the OFDM transmitter according to the IEEE 802.11a WLAN standard. This implementation will be done in Field Programmable Gate Arrays (FPGA) due to their speed and capabilities. Simulator tool (MODELSIM) is used to verify the design functionality and the designed module is synthesized the OFDM Module into Xilinx Spartan - 3E (XC3S500E).**

***Key Words* — FPGA, VHDL, OFDM, IEEE 802.11a and Pipelining.**

I. INTRODUCTION

The Orthogonal Frequency Division Multiplexing (OFDM) is mainly used in the wireless communications at earlier days. Then some other related communications also used this technique. This is due to the genuine advantage of OFDM over single carrier system in multi-path fading channels. Some of the OFDM based techniques are the IEEE 802.11a&g for Wireless Local Area Networks (WLANs), Wi-Fi, and the growing IEEE802.16 for Metropolitan Access, Worldwide Interoperability for Microwave Access (WiMAX) [5].In this design, we used OFDM for wireless LAN 802.11a model. The main work is to implement the digital baseband part of the physical layer of OFDM transmitter. A pipeline is a set of data processing element connected in series, so that the output of one element is the input of the next one. The elements of a pipeline are often executed in parallel or in time-sliced fashion; in that case, some amount of buffer storage is often inserted between elements. This pipelined model is used in this OFDM for increasing the throughput, low power consumption and reducing the hardware complexity of the design. These are the main purposes of this design. This paper organized into six sections. Section 2 shows the basics and process of OFDM. In section 3, we discuss about the IEEE 802.11a standard. Section 4 discusses about the proposed design and process. In section 5, we can see the implementation results of the design. Finally, the section 6 shows the conclusion.

II.OFDM SYSTEM AND PRINCIPLES

The Orthogonal Frequency Division Multiplexing (OFDM) is a parallel transmission scheme. At first, this technique is used in Digital Audio Broadcasting in 1995. After that, in 1999 the IEEE 802.11a standard was released based on OFDM [2]. Then this technique is widely adopted to many related wireless communication systems. Thus the OFDM is developed in communication

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models due to many advantages mainly like high data rates. Orthogonal frequency division multiplexing (OFDM) is nowadays widely used for achieving high data rates as well as combating multipath fading in wireless communications. In this multi-carrier modulation scheme data is transmitted by dividing a single wideband stream into several smaller or narrowband parallel bit streams. Each narrowband stream is modulated onto an individual carrier. The narrowband channels are orthogonal vis-à-vis each other, and are transmitted simultaneously [1]. A major benefit of OFDM systems is their low cost of implementation, due to the relatively simple components required. An OFDM system requires Digital Signal Processing (DSP) hardware for the implementation of the IFFT and FFT transformations. These processors are inexpensive and widely available, either as stand-alone components or on FPGA hardware. An OFDM receiver requires only one modulator and demodulator, in contrast with other multi-carrier systems. OFDM is well-suited for wireless communication.

OFDM makes efficient use of the spectrum by allowing overlap. By dividing the channel into narrowband flat fading sub channels, OFDM is more resistant to frequency selective fading than single carrier systems are. It eliminates ISI and ICI through use of a cyclic prefix. OFDM has no inter carrier guard bands. It controlled overlapping of bands. OFDM has Maximum spectral efficiency (Nyquist rate). It is very sensitive to freq. synchronization. We can easily implement this using IFFTs. OFDM makes efficient use of the spectrum by allowing overlap. It eliminates ISI and ICI through use of a cyclic prefix. OFDM is computationally efficient by using FFT techniques to implement the modulation and demodulation functions. The figure 1 shows that the basic OFDM architecture building blocks.

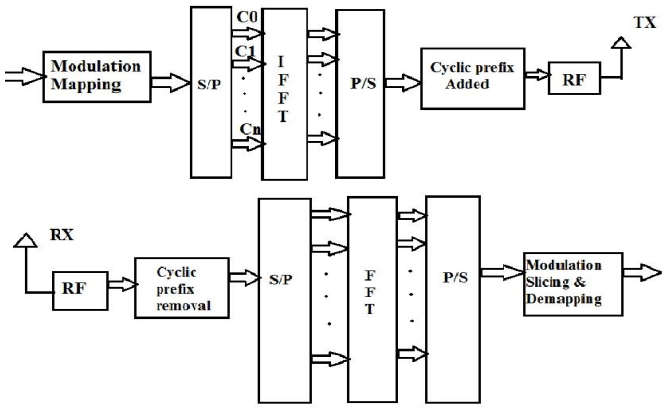

Figure 1 Basic OFDM system Architecture[1]

In this design, the same building blocks in transmitter side is used in the receiver side. So this model is known as mirror circuit model. In this model, the most important block is the Discrete and Inverse Discrete Fourier Transform (DFT and IDFT) that are used to demodulate and modulate the constellation data processed by the mapping block.

III . WIRELESS LAN IEEE 802.11aSTANDARD

In 1999, the IEEE802.11a standard for WLAN was established. IEEE Std 802.11 [ISO/IEC DIS 8802-11] defined the Wireless LAN Medium Access Control and Physical Layer Specifications. Until recently it has mainly been used in USA, but it is now coming to other parts of the world. The radio transmission takes place in a 20 MHz wide frequency band divided into 64 sub bands. 48 of these sub bands are used for transmission and 4 are used as pilot sub carriers. The remaining 12 sub bands are unused [3]. The data rates in the standard are 6, 9, 12, 18, 24, 36, 48, and 54Mbps. The design supports only the mandatory data rates in the standard, the 6, 12 and 24 Mbps [2]. The 802.11a standard is based on the OFDM technique of modulation, 52 sub carriers (SCs)

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are standard, and used to spread the serial data stream on parallel slow rate streams.

The main design parameters for the OFDM in the 802.11a standard are listed in below table 1.The IEEE 802.11a standard can achieve variable data rates which are shown in the above table 1.This data rates variation is achieved through the various modulation schemes used.

Parameter	values
Sampling Frequency	20 MHz
Number of Sub-carriers	52 (48 data and 4 pilots)
OFDM Symbol Period	4 µs (80 samples)
Cyclic Prefix Period	0.8 µs (16 samples)
Modulation Scheme	BPSK,QPSK,16&64-QAM
Data rate	6,9,12,18,24,36,48 and 54 Mbps
FFT Processor	64 point

Table 1 OFDM Parameters in the IEEE802.11a Standard.

IV PIPELINED IMPLEMENTATION DETAILS.

This design is made use of pipelining which is achieved through the duplicating memory elements (Registers, RAMs or ROMs). The main purpose of pipelining is to reduce the delay of process and to avoid complexity. That memory elements will buffer the incoming bit while the previous bit is being processed [5]. This design was finished and targeting in the Xilinx Spartan 3(XC3S50) FPGA.The divide- and-conquer technique is used for this design. That means each module of the system will be separately designed and tested. Then finally, the all modules are combined and the entire design was designed with addition of some extra modules. Before the modulation process, the scrambling and coding process will be done. Scrambling is the process which transposes or inverts the otherwise encodes a message at the transmitter to make the message unintelligible for some noise avoidance. Coding is the process to add redundant data long with the input data in transmitter side and it will be removed in receiver side. The main purpose of the coding is to protect the data from error and noises. This coding gives the error detecting and error correcting capability to the receiver. Next, in the existed model system, the main interleave design is based on the RAMs. In this type, the data is written in row order and read in column order [4]. This design needs large number multiplexers and large memory is used in the FPGA.The interleaves are used in data transmission for error correction. The interleaving is a way to arrange the data in non-continuous way to increase the performance. It is also a technique commonly used in communication systems to overcome correlated channel noise such as burst error or fading. Now, while implementation, this system needs lot of multiplexers and different sizes of RAMs according to the interleave sizes. The interleave is based on the equations described in [2]. In the proposed design, the interleave work is based on the look up tables. They were implemented as small read only memories (ROM). One ROM is designed for each different interleave size required. This ROM block is designed using VHDL in this system. Using this design, the need for large number of multiplexers are avoided and the abundant memory inside the FPGA was used. Thus, the interleaving pattern stored in these ROMs is used as an index for the output memory [5].

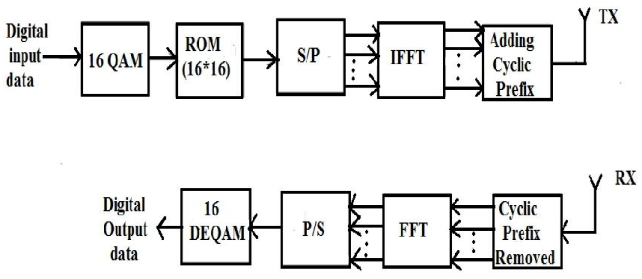

Figure 2 Pipelined Implementation Architecture.

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In this model, the transmitter first converts the input data from a serial to parallel. Each set of data contains one symbol, Si, for each subcarrier signal. Before performing the IFFT this data set is arranged on the horizontal axis in the frequency domain. An inverse Fourier transform converts the frequency domain data set into samples of the corresponding time domain representation of this data. The receiver performs the inverse of the transmitter. The FFT converts the time domain samples back into a frequency domain representation. Magnitudes of the frequency components correspond to the original data. Finally, the parallel to serial block. converts this parallel data into a serial stream to recover the original input data. The above process are done by the transmitter and receiver in the basic OFDM. In this design, we used the pipelined implementation in the transmitter block.

Next, in the design of IFFT, the interleaved bits are translated and mapped into Phase and Quadrature components. The OFDM sub carriers are modulated using the different type of modulations. The grouped bits are used to address the specific ROM and to be mapped into the corresponding I/Q values as per the selected modulation scheme. Here we are using ROM (16*16) due to the 4 bit data transmission. The Figure 3 shows that the mapping system. In this system, the ROM contains the I & Q values. The values are already stored in the ROM. The grouped bits are used to index the ROMs and obtain the corresponding I/Q pair.

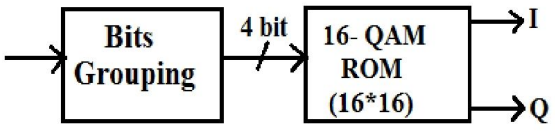

Figure 3 Mapping system.

In this design , the IFFT needs 64 pairs of I & Q. But the mapping system produces only 48 sub carriers.4 pilot carriers are added at specific locations. The remaining 12 pairs are unused in this model. This was implemented as a block used to store the generated I & Q pairs by the mapping system and it also to add both pilot and zero sub carriers. Next the main IFFT block is designed. This block is designed using the pure VHDL. The pipelining is used in the previous stage, where each generated I/Q pair in the I/Q bank is fed to the IFFT processor. Next, after the required number of cycles by the IFFT block, the generated real and imaginary pairs are forwarded to the Cyclic Prefix block. In the Cyclic Prefix block, they are 80 samples are used. In the IEEE 802.11a standard, the last 16 samples of the output of the IFFT is copied and added with the starting samples and completes the OFDM symbol. The maximum delay in this process is 0.8 µs. This delay is due to the 16 samples copied and added with the beginning samples.

V IMPLEMENTATION RESLUTS

Thus the design is implemented using the divide and conquer approach. It was used to design and test each module of the design in separately and later combine the all blocks and make the complete system. Thus the work was finished for the implementation design of the digital baseband part of the OFDM transmitter that conforms to the IEEE 802.11a standard. In this method, the implementation is done in pure VHDL. However, the implemented design supports only for the data rates in the standard, the 6, 12 and 24 Mbps because of the puncturing and modulation technique (16-QAM) and 4 bits data transmission. It has difficulties in the implementation design for the other data rates. Because some difficulties are placed in puncturing process. From the implementation, we can know the below important process for this work. It is the mapping process through the utilizing look up tables and memory. Therefore, the most resources consumed by the design will

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be the pure LUTs available on the FPGA and the memory elements as well. The IFFT block is designed using the available IP cores for the pipelining implementation. The design was targeted and to be mapped on Xilinx FPGA [6]. Xilinx Spartan-3E (XC3S500E). This FPGA is selected based on the availability of IFFT in the FPGA.

The table 2 shows the device required and utilized in the FPGA for the implementation of the OFDM transmitter that conforms to the IEEE 802.11a standard.

Logic Utilization	Used	Available	Utilization
Number of Slices	1521	3584	42%
Number of Slice Flip Flops	1682	7168	23%
Number of 4 input LUTs	2549	7168	35%
Number of bonded IOBs	66	141	46%
Number of MULT 18*18s	12	16	75%
Number of GCLKs	1	8	12%

Table 2 Device Utilization Summary.

From the device utilization summary table, we know that the less number of multiplexers, LUTs and number of Flip flops are used compare with the before architecture.

VI. CONCLUSION

Thus, the pipelined implementation of OFDM is designed for the IEEE 802.11a standard. The design is done using the pure VHDL. From the results, the design can easily fit into Xilinx Spartan-3E FPGA. Some difficulties are in the placing and routing fields of that FPGA. But this results are best than the previous method results. This design has been done only to the specific data rates (6,12 and 24 Mbps). We can solve this problem using to make the changes in modulated schemes and the puncturing process.

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