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IMPLEMENTATION OF SINGLE PHASE 13 LEVEL INVERTER USING SINGLE DC SOURCE

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ABSTRACT:

This Paper has emerged recently as a very important alternative in the area of high-power medium voltage energy control. The multilevel voltage source inverters unique structure allows them to reach high voltages with low harmonics without use of transformers or series connected synchronized switching devices. The general function of the multilevel inverter is to synthesize a desired voltage from several levels of dc voltages for these reason multilevel inverters can easily provide the high power required of a large electric drives. As the number increases the synchronized output waveform has more steps, which produces a staircase waveform that approaches a desired waveform. Also as more steps are added to the waveform the harmonic distortion of the output wave decreases approaching zero as the number of levels increases. As the number of levels increases, the voltage that can be spanned summing multiple inverters much that no voltage sharing problems are encountered by the active devices.

INTRODUCTION:

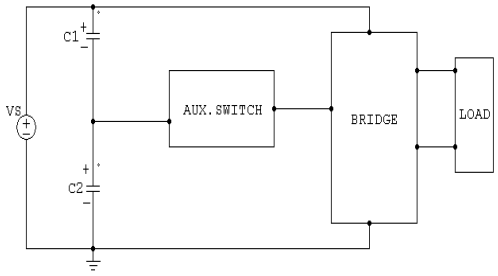
Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of switches permit the addition of capacitor voltages, which results as high voltage at output, while the power semiconductor must withstand only reduced voltages. The all different topologies presented in the multilevel inverter are cascaded, diode clamped and capacitor clamped. The main disadvantage associated with them is their circuit complexity, requiring a high number of power switches. This topology includes an H-Bridge stage with an auxiliary bidirectional switch, drastically reducing the power circuit complexity, and a modulator and firing control circuit developed using a controller.

PROPOSED METHOD:

The different topologies presented in the multilevel inverter shows a number of characteristics in common. The main disadvantage associated with the multilevel inverter configuration is their circuit complexity, requiring a high number of power switches. When we are entering the simplified H-Bridge multilevel inverter, power devices will be reduction and circuit complexity also reduction so circuit losses also reducing.

Even taking into account the technological tendency to lower the prize at which multilevel inverter can compete with standard configuration. This topology includes an H-Bridge stage with an auxiliary bidirectional switch, drastically reducing the power circuit complexity, and a modulator and firing control circuit developed using a controller

The simplified H-bridge multilevel inverter achieves a reduction in the number of main switch required and uses no more diodes and capacitors that the second best topology, the asymmetric cascade configuration .In the modulator circuit, the FPGA can perform all required modulation functions providing another important reduction in cost and circuit complexity.



BLOCK DIAGRAM OF SIMPLIFIED 13 LEVEL INVERTER

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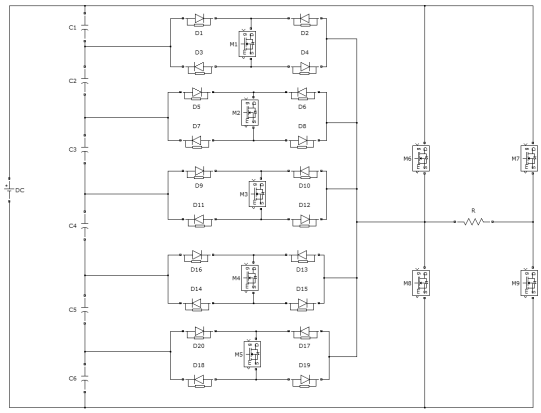


CIRCUIT DIAGRAM OF 13-LEVEL INVERTER

Circuit Configuration

The block diagram of simplified H-bridge multilevel inverter that 13- level simplified H- bridge multilevel inverter. The H-bridge is formed by four main power devices, S1 to S4. For 13 level output voltage, five auxiliary switches, four main switches and six capacitor requires.

Stage Advantages

To prove the reduction in component numbers achieved by this simplified H-bridge multilevel inverter configuration, the number of component required to implement a 13 level inverter using simplified H- bridge multilevel inverter and three previously defined ones: the two that considered as the standard multi-level stages, the diode clamped and the capacitor clamped configuration, and a new and highly improved multi-level stage with reduced switches.

Main power switches:

The new topology achieves a around 40% reduction in the number of main switches required, using only nine controlled power switches instead of twelve required in any of the other three configurations. The auxiliary switch voltage and current rating are lower than the once required by the main controlled switches.

Auxiliary Devices (diodes & capacitors):

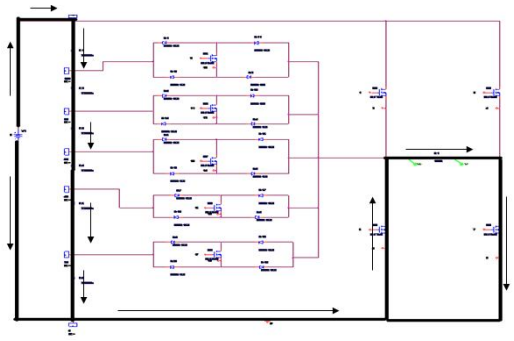
The new configuration reduces the number of diodes and capacitors, when compared with diode clamped configuration. The new configuration reduces the number of capacitors, when compared with the capacitor clamped configuration. The new configuration uses no more diodes or capacitors.

Additionally, since three capacitors are connected in parallel with the main dc power supply, no significant capacitor voltage swing is produced during normal operation, avoiding a problem that can limit operating range in some other multi-level configuration.

MODE OF OPERATION

The operating principle of this inverter can be divided into thirteen, which has positive mode of operation and negative mode of operation.

MODE 1(0 VOLTAGE LEVEL)

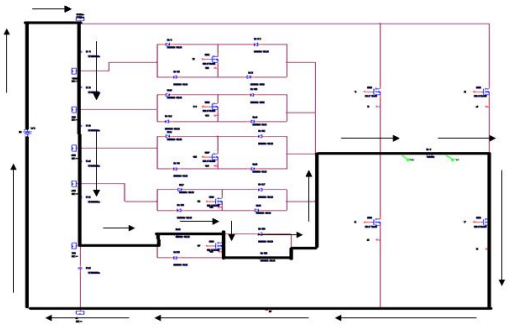


Switches M3 and M4 on.

Capacitors C1, C2, C3, C4, C5, C6 charging

KVL equation Vs + Vm8 –Vr –Vm9 = 0

MODE 2(VOLTAGE LEVEL: +VDC/6)



Switches M4 and M9 on.

Capacitors C1,C2,C3,C4,C5 charging.

KVL equation Vs + Vm5 – Vr – Vm9 = 0

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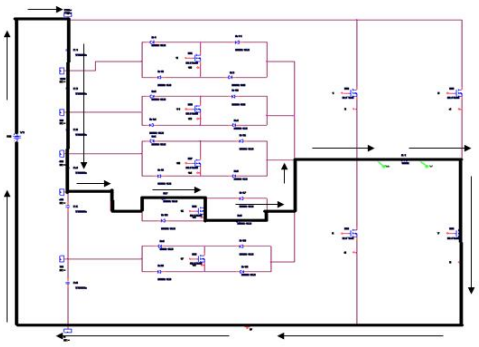
MODE 3(VOLTAGE LEVEL: +2VDC/6)

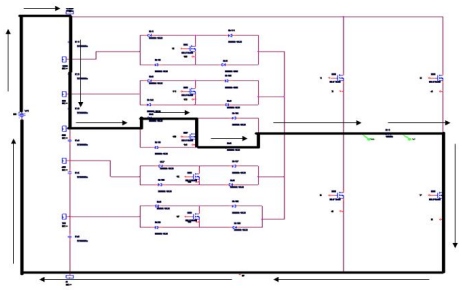


Switches M4 and M8 on.

Capacitors C1,C2,C3,C4 charging.

KVL equation Vs+ Vm4 – Vr – Vm9 = 0

MODE 4(VOLTAGE LEVEL: +3VDC/6)

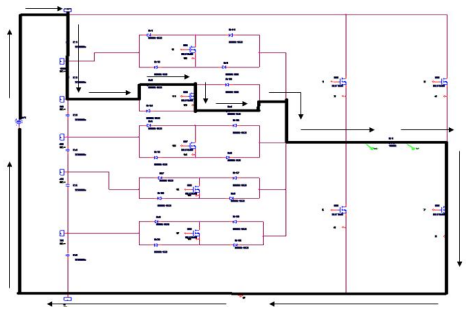


Switches M4 and M7 on.

Capacitors C1,C2,C3 charging.

KVL equation Vs + Vm3 – Vr – Vm9 = 0

MODE 5(VOLTAGE LEVEL:+4VDC/6)

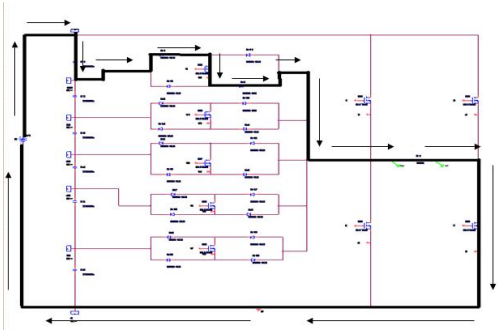


Switches M4 and M6 on.

Capacitors C1,C2 charging.

KVL equation Vs + Vm2 – Vr – Vm9 = 0

MODE 6(VOLTAGE LEVEL:+5VDC/6)

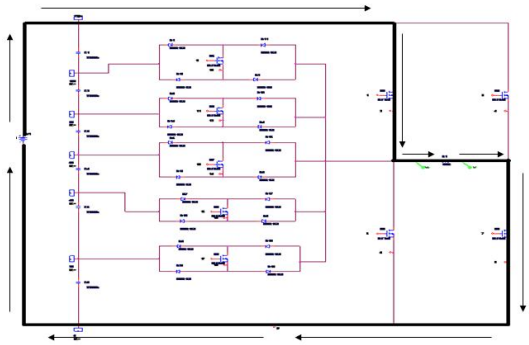


Switches M4 and M5 on.

Capacitor C1 charging.

KVL equation Vs + Vm1 – Vr – Vm9 = 0

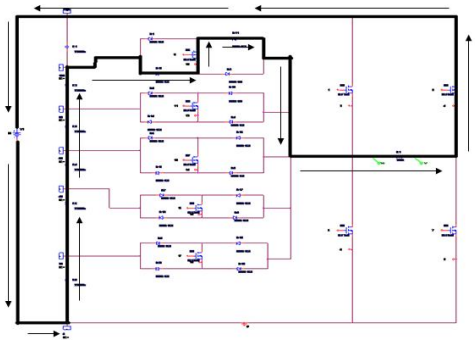
MODE 7(VOLTAGE LEVEL: +VDC)



Switches M1 and M4 on.

KVL equation Vs + Vm6 – Vr – Vm9 = 0

MODE 8(VOLTAGE LEVEL:-VDC/6)



Switches M2 and M5 on.

Capacitors C2,C3,C4,C5,C6 charging.

KVL equation Vs + Vm5 – Vr –Vm7 = 0

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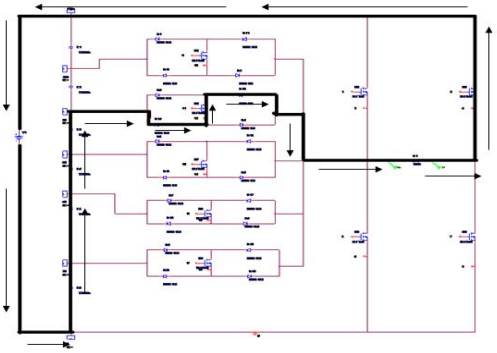
MODE 9(VOLTAGE LEVEL: -2VDC/6)

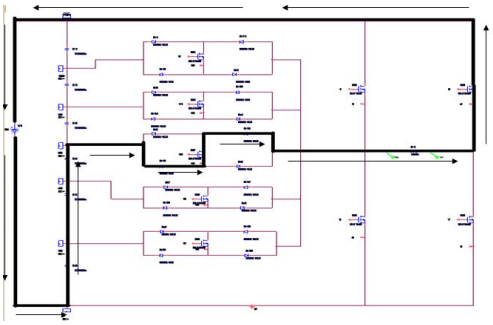


Switches M2 and M6 on.

Capacitors C3,C4,C5,C6 charging.

KVL equation Vs + Vm2 – Vr – Vm7 = 0

MODE 10(VOLTAGE LEVEL: -3VDC/6)

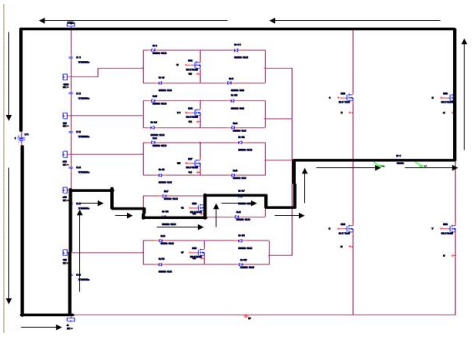


Switches M2 and M7 on.

Capacitors C4,C5,C6 charging.

KVL equation, Vs + Vm3 – Vr – Vm7 = 0

MODE 11(VOLTAGE LEVEL: -4VDC/6)

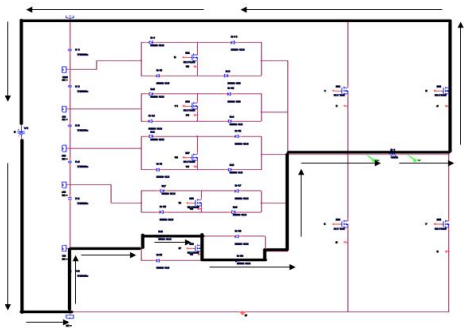


Switches M2 and M8 on.

Capacitors C5,C6 charging.

KVL equation, Vs + Vm4 – Vr – Vm7 = 0

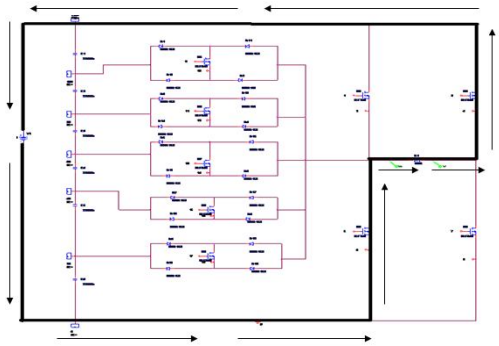
MODE 12(VOLTAGE LEVEL: -5VDC/6)



Switches M2 and M9 on.capacitor C6 charging.

KVL equation Vs + Vm5 –Vr – Vm7 = 0

MODE 13(VOLTAGE LEVEL: -VDC)



Switches M2 and M3 on.

KVL equation, Vs + Vm8 –Vr – Vm7 = 0

CONCLUSION:

A multilevel inverter with individual dc sources has been proposed for use in large electric drives. Simulation and experimental results have shown that with a control strategy operates the switches at the fundamental frequency, these converters have low output voltage THD and high efficacy and power factor. In summery the main advantages of using multilevel converters for large electric drives include the following,

1. They are suitable for large volt-ampere rated and /or high voltage motor drives.
2. These multilevel converters systems have higher efficiency because the devices can be switched at minimum frequency.

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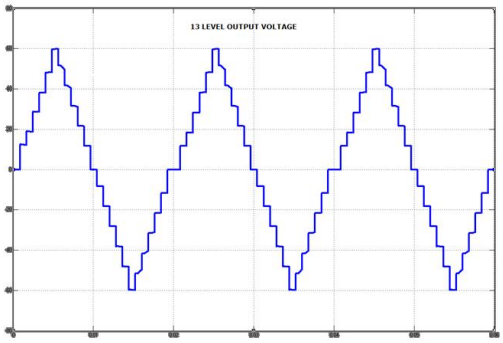
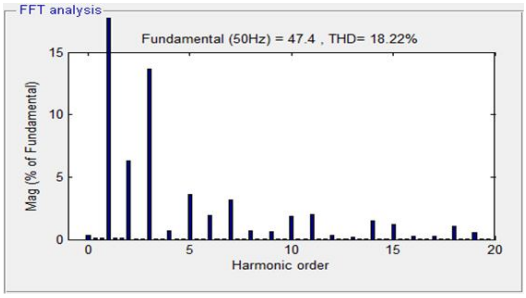
3. Power factor is close to unity for multilevel inverters used as a rectifier to convert generated ac to dc.

4. No EMI problem or common mode voltage/current problem exists.

5. No charge unbalance problem results when the converters are in higher charge mode or drive mode.



OUTPUT VOLTAGE OF 13-LEVEL



Total harmonic distortion

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