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Design of Two Stage Op-Amp

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ABSTRACT

The Operational Amplifier (Op-Amp) is a fundamental building block in Mixed Signal design. Two stage Op-Amp is one of the most commonly used Op-Amp architectures. In this paper an operational amplifier by CMOS is presented whose input depends on bias current which is 30uA and designed using 1 um technology. In sub-threshold region due to unique behaviour of the MOS transistors not only allows a designer to work at low voltage and also at low input bias current. Most CMOS Op-Amps are designed for specific on-chip applications and are only required to drive capacitive loads of a few pf. In this paper design of a two stage fully differential CMOS operational amplifier is presented. The proposed two stage op amp produces gain of 80 dB. Comparator designed from CMOS Op-Amp is also discussed.

Key words: CMOS(Complementary metal oxide Semiconductor), Gain, Op-Amp (Operational amplifier), pf (picofarad), Phase.

1. INTRODUCTION

Operational amplifiers (Op-Amps) are basic building blocks of a wide range of analogue and mixed signal systems. Basically, Op-Amps are voltage amplifiers being used for achieving high gain by applying differential inputs. The gain is typically between 50 to 60 decibels. This means that even very small voltage difference between the input terminals drives the output voltage to the supply voltage. In the case of using 1um CMOS technology, this small voltage difference can be around tens of mili volts. As new generations of CMOS technology tend to have shorter transistor channel length and scaled down supply voltage, the design of Op-Amps stays a challenge for designers. An operational amplifier is a direct-coupled high-gain amplifier usually consisting of one or more differential amplifiers. The operational amplifier is a versatile device that can be used to amplify dc as well as ac input signals and was originally designed for performing mathematical operations.

Operational Amplifiers was used describe amplifiers that performed various mathematical operations in the computing field. It was found that the application of negative feedback around a high gain DC amplifier would produce a circuit with a precise gain characteristic that depended only on the feedback used. By the proper selection of feedback components, operational amplifier circuits could be used to add, subtract average, integrate, and differentiate. [1].

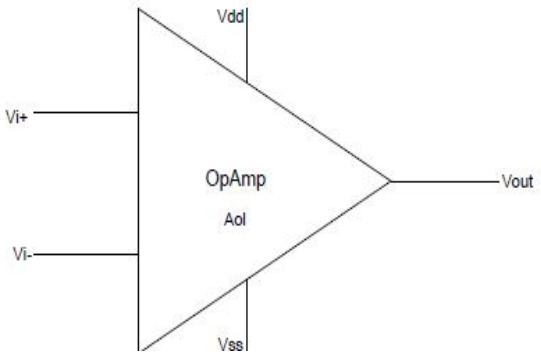

Figure 1: Op-Amp Symbol

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The designing of Op-Amps puts new challenges in low power applications with reduced channel length devices. Advancements which have appeared recently through new techniques and technologies, give us multiple alternatives in implementations. In two stage CMOS Op–Amps because of two dominant poles the phase margin could easily reach to less than the amount which is just enough for stable operation. This serious problem should be taken care of by designers, otherwise there is a good possibility that the Op-amp output will oscillate and instead of an amplifier it will become an oscillator. In some applications the gain and/or the output swings provided by cascade op-amps are not adequate. In such cases, we resort to "two stage" Op-Amps, with the first stage providing a high gain and the second, large swing. In contrast to cascode Op-Amps, a two-stage configuration isolates the gain and swing requirements as well [3]. To provide more gain and swing two-stage Op-Amps are used.

About 5-15 dB gain is provided by the second stage which is not very high. Also the higher output swing is provided by the second stage which is crucial to some applications, especially in today's technologies with lower supply voltages. So, the second stage is a simple amplifier like a CS stage.

2. OP-AMP ARCHITECTURE

Amplification is an essential function in most analog (and many digital) circuit [3]. The block diagram of two stage Op-Amp is

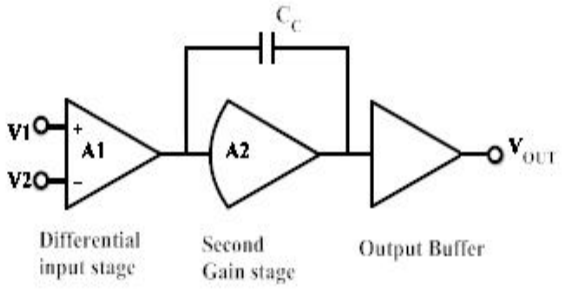

Figure 2 : Op-Amp architecture

It consists of two stages in which first is differential stage and second is the gain stage. Output buffer is also used. In CMOS Op-Amp compensation network is used to which a feedback network is applied around the amplifier in virtually all Op-Amp applications. Therefore, to obtain stable performance the amplifier must be compensated. There are many types of compensation network used but we used miller compensation. In miller capacitance is used for feeding back around a high-gain, inverting stage. Miller capacitor used with a unity gain buffer block the forward path and also eliminates the RHP zero. Also miller with a nulling resistor is used which is similar to miller but a series resistance is added which control the gain over the RHP zero [4].

The circuit is designed using Tanner S-edit tool and Tspice code is written in T-edit. Waveforms are obtained from W-edit. The circuit of two stage Op-Amp using Tanner is

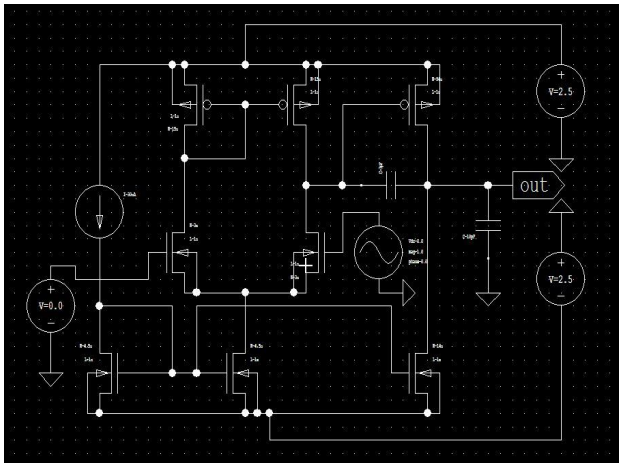

Figure 3: P-spice schematic of Op-Amp

It consists of 8 transistors. The n-channel transistors *M*1 and *M*2 form the input differential pair, and the p-channel transistors *M*3 and *M*4 form the active load. The diff-amp input stage is biased by the current mirror *M*5 and *M*6, in which the reference current is supplied by I_{Bias} which is 30uA. The second stage, which is also the output stage, consists of the common-source connected transistor *M*7. Transistor *M*8 provides the bias current for *M*7 and acts as the active load. An internal compensation capacitor is included to provide stability.

3. STEPS OF OP-AMP DESIGN

Step 1: Calculate the minimum value of compensation capacitor (C_C) which is given by

$$C_C > (2.2/10)\, C_L$$

Step 2: Calculate current value I_5

$$I_5 = (\text{Slew rate}) * C_C$$

also, $I_5 = 10 * \frac{Vdd + |Vss|}{2Ts}$ where T_s is settling time

Step 3: Calculate S_3 using ICMR requirement i.e.

$$S_3 = \left(\frac{I5}{K'3[Vdd - Vin(max.) - |Vto3|(max.) + Vt1(min.)]2}\right)$$

Step 4: Calculate g_{m1}

$$g_{m1} = GB * Cc$$

$$\text{So, } (W/L)1 = (W/L)2 = \frac{g_{m1}^2}{2K'N\,I1}$$

Step 5: Now calculate V_{DSS}

$$V_{DSS} = V_{IN}(\text{min.}) - V_{SS} - \left(\frac{I5}{ß1}\right)^2 - V_{J1}(\text{max.})$$

Using V_{DSS} Calculate $(W/L)_5$

$$S_5 = (W/L)_5 = \frac{2(I_5)}{kr_5(V_{dss})^2}$$

Step 6: Calculate S_6

$$S_6 = (W/L)_6 = \frac{g_{m6}}{K'_6\, V_{ds6}\ (sat.)}$$

Step 7: Calculate I_6

$$I_6 = \frac{g_{m6}^2}{2\ K'_6\ \left(\frac{W}{L}\right)_6}$$

Step 8: Calculate S_7

$$S_7 = (W/L)_7 = (W/L)_5 * \frac{I_6}{I_5}$$

Step 9: Calculate the Overall Gain A_V

$$A_V = \frac{2\,(g_{m2})\,(g_{m6})}{I_5\,(\lambda 2 + \lambda 4)\ \ I_6\,(\lambda 6 + \lambda 7)}$$

The design of two stage Op-Amp was done with the following specifications;

Model parameters;

- $K'_N = 50\mu$
- $K'_P = 110\ \mu$
- $V_{TN} = 0.7$ V
- $V_{TP} = -0.7$ V
- $\lambda_n = 0.04$
- $\lambda_P = 0.05$

For 1µm technology Parameters are are shown in Table I

Table 1: W/L Parameter for Transistor

MOSFET	W/L ratio(µm)	MOSFET	W/L ratio(µm)
M1	3/1	M5	94/1
M2	3/1	M6	14/1
M3	15/1	M7	4.5/1
M4	15/1	M8	4.5/1

- I_{dc}=30µA
- C_c=3pF, C_L=10pF
- $V_{dd}=V_{ss}$=2.5V

4. WAVEFORM FOR AC ANALYSIS OF OP-AMP

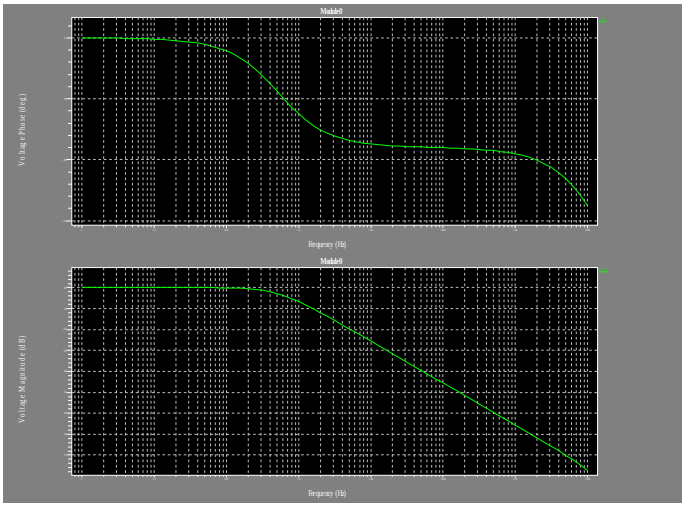

Figure 4 :Gain and Phase margin of Op-Amp

5. CMOS OP-AMP AS COMPARATOR

The comparator is a circuit that compares one analog signal with another analog signal or a reference voltage and outputs a binary signal based on the comparison. The comparator is basically a 1-bit analog-to-digital converter.

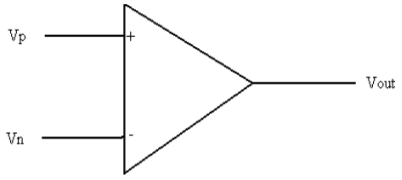

Figure 5: Comparator Symbol

The output of comparator is high (VDD) when the difference between the non inverting and inverting input is positive, and low (VSS) when this difference is negative.

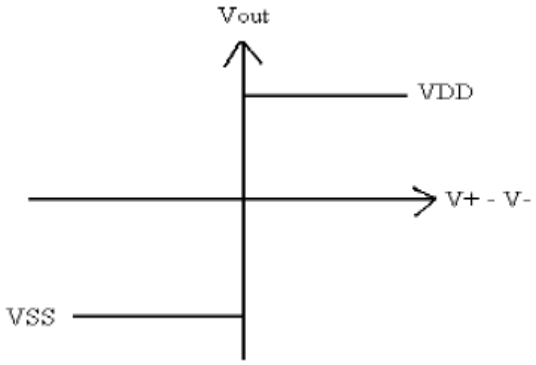

Figure 6 : Output of comparator

The comparator is a critical part of almost all kind of analog-to-digital (ADC) converters [2]. Depending on the type and architecture of the comparator, the comparator can have significant impact on the performance of the target application. The speed and resolution of an ADC is directly affected by the comparator input offset voltage, the delay and input signal range. Ideally the gain of the comparator is infinite and the offset voltage is zero volts. But practically the gain of the comparator is finite.

The PSPICE simulations are done for the comparator based on 1um CMOS technology. The statistic information (VTHn, VTHp, Kn, Kp) provided by the foundry of 1um CMOS technology is used. The transient analysis is shown in the fig.

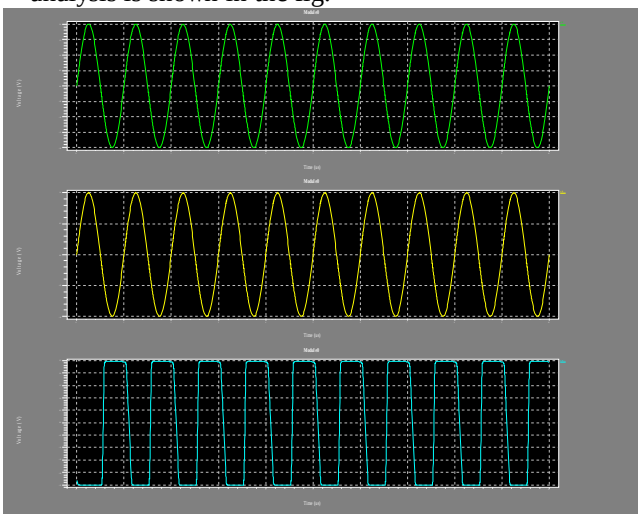

Figure 7: Transient analysis of Comparator

6. **CONCLUSION**

The amplifier presented in this paper operates in saturation mode and regulates its bias current. When a signal is applied the current in the amplifier increases so that these amplifiers have very high driving current. The op-amp has low power as well as low voltage. Its slew rate is higher than reported. Low power low voltage amplifier is designed at 1µm technology whose gain is 80dB and phase margin assuming a feedback factor of 0.5 is obtained 60 degrees. The unity gain bandwidth is obtained 400MHz. The maximum differential output swing was between 2.5V to -2.5V.

REFERENCES

1. Ayush Gupta, Aditya Bhansali, Swati Bhargava, Shruti Jain "Configuration of Operational Amplifier using CMOS "
2. Sima Payami "Design of an Operational Amplifier for High Performance Pipelined ADCs in 65nm CMOS ", June 2012
3. Rajkumar S. Parihar Anu "Design of a Fully Differential Two-Stage CMOS Op-Amp for High Gain, High Bandwidth Applications"
4. P.K.SINHA, ABHISHEK VIKRAM and DR. K.S.YADAV " Design Of Two Stage CMOS Op-Amp With Low Power And High Slew Rate" IJERT Vol. 1 Issue 8, October – 2012
5. Gupta P.E.Allen and D.R.Holberg, CMOS Analog Circuit Design, first Indian edition, 2010.
6. Microelectronics - Circuit Analysis and Design (4th Edition) by DONALD A. NEAMEN.