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Simulink Model of Elimination of Harmonics By Using Multilevel - Inverters Through Hysteresis Control

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Abstract: **- - In this paper, a hysteresis current control technique for a single-phase five-level inverter with cascaded H-bridge topology is proposed. The basic study to implement the logic for correct voltage-level selection, various schemes available in the literature have been described and will provide a useful framework and point of reference for the future development of hysteresis modulation for multilevel converters. By using the recently developed multilevel hysteresis modulation approaches, the advantages of using several accessible dc potentials in a multilevel inverter have been fully exploited. All of these hysteresis modulation approaches are tested for tracking a current reference when applied to a five-level inverter.**

Index terms: - Hysteresis control, multiband, multi-offset band, time-based.

1. INTRODUCTION

The various techniques are described and compared for tracking the reference signal in order to attain an adequate switching optimization, excellent dynamic responses and high accuracy in steady-state operation. To generalize the existing MHM techniques for higher level inverters, their modified versions have been also discussed. The advantages of using various dc voltage levels by using these schemes. these can further be extended to any multilevel inverter structure, even in the case of *n*-level voltage waveforms and three-phase systems. The objective of two-level hysteresis current control is to switch the converter transistors in such a manner that the converter load current tracks a reference within a specified hysteresis band. Consider a single-phase half-bridge inverter, as shown in Fig. 1(a) for two-level hysteresis current control. In Fig. 1, two dc sources of magnitudes *V*dc/2 are considered at the dc link of inverter and their common point (n, neutral point) is grounded.

The net controllable output voltage of the inverter is uVdc /2, where u is the control input and represents the switching logic of inverter. It assumes the values +1 and −1 for the two-level inverter of Fig. 1(a). The inverter output voltage van can be represented as follows:

$van = uVdc/2 = Ria + Ldia/dt + vback$ ……(1)

where ia -load current, vback is back EMF voltage, and L and R are the load inductance and resistance. As vback increases as larger reference current slopes are required, larger average values of van need to be used. Since the voltage across the load resistance is often small, this value can often be neglected. Introducing a term diref /dt, where iref is the current reference to be tracked, becomes as follows:

$d(ia- iref)/dt \approx uVdc/2 - vback / L - diref/dt$ …..(2)

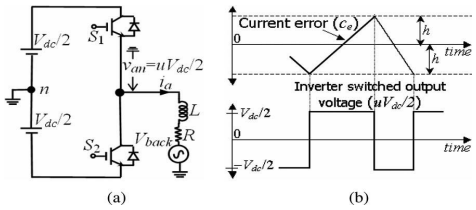

Fig1. (a)Two-level Half-bridge inverter,(b)Two-level hysteresis control.

It is evident from (2) that the current error (ce = ia − iref) can be reduced by increasing or decreasing van , depending on the polarity of ce . Fig. 1(b) represents the implementation logic for this correct voltage-level selection for a two-level inverter using hysteresis control. It can be seen that as the measured current (ia) becomes greater than its reference (iref) by the hysteresis band "h," the inverter output voltage (uVdc /2) is switched to its lowest level (−Vdc /2, u = −1) in order to decrease the current [according to (1)]. Likewise, when ia becomes less than iref by "h", uVdc /2 is switched to its highest level (Vdc /2, u = +1) in order to increase the current. For the inverter of Fig. 1(a), u assumes the value +1 for the switching logic S1 = 1, S2 = 0 and −1 for S1 = 0 and S2 = 1,Based on the two-level hysteresis control logic described earlier, the control input u can be defined as follows:

if (ce (t) ≥ +*h*), then u (t) = -1
else if (ce (t) < -*h*), then u(t) = +1 ……(3)

However, for multilevel converters, as a larger number of output voltage levels are available, the task is to select a particular voltage-level output to force the control variable to zero on an instantaneous basis once it exceeds certain bounding limits. Therefore, a multilevel hysteresis modulator (MHM) requires additional logic to select the appropriate voltage level at any time instant so as to confine the control signal within a specified hysteresis band. For a five-level inverter, van in (1) may be defined as van = nVdc , where n = 1/2, 1/4, 0, −1/4, and −1/2, as a five-level

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inverter may select between voltage levels Vdc /2, Vdc /4, 0, −Vdc /4, and −Vdc /2 for the net dc-link voltage of Vdc . Then, in a similar manner as described earlier, ce can be kept limited to a specified band by selecting a higher or lower voltage level than its present output depending on the polarity of ce. The logic for correct voltage-level selection, various schemes available in the literature have been described in the following sections on the basis of a single-phase five-level inverter. In Section II, the multiband (MB) MHM scheme is presented, which has the feature of floating voltage levels at the boundaries of the band with symmetric inner bands placement.

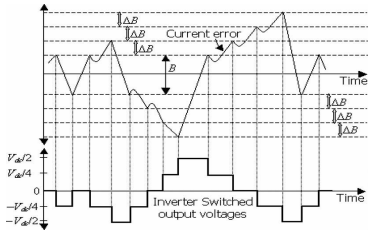

Fig.2. MB five-level hysteresis current control.

In Section III, the multioffset-band (MOB) approach is presented, which allots fixed voltage levels at the band boundaries and needs to check the slope In Section III, the multioffset-band (MOB) approach is presented, which allots fixed voltage levels at the band boundaries and needs to check the slope as well as the band region of the current error. A modification to this approach is also presented, so that it can be easily extended for higher level inverter systems and tracks the reference more efficiently. Further, a time-based (TB) approach for MHM is presented in Section IV, which can be used to put a limit on maximum switching frequency as well as to achieve improved performances. The detailed simulation and experimental results for all these techniques have been presented.

II. MB HYSTERESIS MODULATION

The MB hysteresis modulation scheme for the multilevel converters uses symmetrical hysteresis bands to control the switching so that the inner band causes switching between adjacent levels, while the outer band causes an additional switching level change whenever necessary. The process, first proposed in [15] and later used is shown in Fig. 2 in the form of current regulation. Whenever the current error crosses the inner boundary *B*, the inverter output is decreased or increased by one level .Generally, this voltage change will cause the current error to reverse its direction without reaching the next outer band. However, if the error does not reverse, it will continue through the boundary of *B* to the next outer boundary (placed at Δ*B* out of *B*). At this point, next higher or lower level voltage will be switched.

This process continues as discussed earlier until the current error direction reverses. It is important to note that if the voltage level applied at a boundary crossing of the current error is insufficient to force the error back, no next voltage level is applied the error again crosses this boundary next time after the previous voltage level change with the same slope. the principle of MB scheme, simulation studies are performed on a five-level inverter, supplying an *RL* load of $R = 35\ \Omega$ and $L = 30$ mH with the dc-link voltage of 80 V. The back EMF voltage (*v*back) is taken as zero and the inverter devices are assumed nearly ideal. The output current of inverter (*ia*) is controlled using the MB hysteresis scheme to follow a sinusoidal reference having peak-to peak values of ±1.0 A. Corresponding to Fig. 2, the hysteresis band sizes are taken to be $B = 0.04$ A and $B1 = B2 = 0.02$ A. These values are taken for simplicity by following the considerations presented in [16].

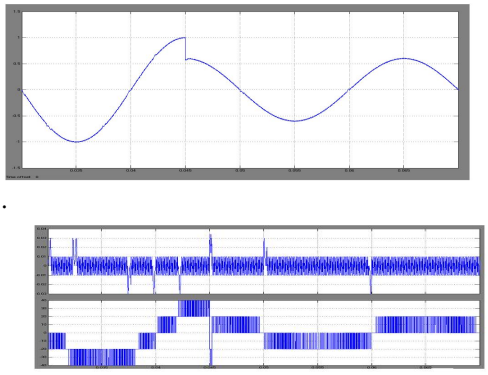

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Fig.3. Transient performance of MB scheme. (a) Reference and measured load current. (b).Current error and hysteresis band plots. (c) Inverter output voltage.

A. Experimental Setup

The main power circuits consist of a single-phase five-level voltage source diode clamped inverter, load, and dc-link circuit. The inverter dc bus is supported by a separately controllable dc supply obtained from a single-phase transformer and diode rectifier circuit. The dc link voltage and load parameters of the inverter are kept same as considered earlier in the simulation studies, i.e., *V*dc = 80V and $R = 35\ \Omega$, $L = 30$ mH, respectively.

The presence of back EMF would serve to create more variation in switching frequency, but without affecting the nature of the current error trajectory. Therefore, for simplicity, back EMF voltage source has not been used. This chopper circuit keeps the dc-link capacitor voltages balanced so that the inverter is able to generate five different and correct voltage levels. It is also important to mention here that the chopper action is unaffected by the different hysteresis modulation methods used in this paper. The dc-link capacitors are $Cd1 = Cd2 = Cd3 = Cd4 = 220\ \mu$F and the chopper circuit parameters are $R1 = R2 = 2.0\ \Omega$ and $L1 = L2 = 20$ mH., the current reference and hysteresis band sizes are considered same (1.0 A, $B = 0.04$ A, and $B1 = B2 = 0.02$ A) as considered earlier in the simulation studies presented. Fig. 3 shows the performance of the MB hysteresis current controller.

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III.MOB HYSTERESIS MODULATION

The MOB scheme uses the bands placed with an offset around the zero current error line. The advantage of using the offsets is that different bands can be easily implemented. As opposed to the previously presented scheme, fixed voltage levels are applied in MOB scheme as the current error crosses a boundary of the band with a certain slope. In this we have two modulation techniques first the conventional MOB scheme is presented, and then, its modified version is presented.

A. Conventional MOB Hysteresis Modulation

In this, the current can be controlled using $n - 1$ offset bands for an n-level inverter. Fixed voltage levels are switched at each of the offset boundaries when the current error crosses the boundary of an offset band in a direction, away from the zero error line. A possible two-offset band arrangement ($B1$, $B2$) for controlling a three-level inverter the error (Ce) touches the corresponding boundaries of $B1$ and $B2$, fixed output voltage levels are switched. The switching takes place when sign of the error and its slope at the boundary of a band are same, and the previous switching had not taken place at the Same boundary of the same band. A five-level multi offset hysteresis current regulation in Fig.5 showing a possible current error trajectory along with the offset-band arrangements and corresponding switched output voltage levels. By following the scheme of [17], it requires four bands ($B1 - B4$) and as the current error touches the corresponding boundaries of $B1 - B4$, fixed output voltage levels are switched. It can be followed that 0 V is switched at the lower limits of$B1$,$B3$ and upper limits of$B2$,$B4$,$-V$dc/4 at the upper limit of $B1$, $+V$dc/4 at the lower limit of $B2$, $-V$dc/2 at the upper limit of $B3$ and $+V$dc/2 at the lower limit of $B4$. The limitation, when using this scheme for a higher level inverter can be seen by looking at the current error path from F to G. It is evident that a voltage-level transition from $-V$dc/2 to 0 V occurs at G, thereby, skipping the level $-V$dc/4. This results in inverter output voltage with large steps and large voltage stress across the devices at the switching instants.

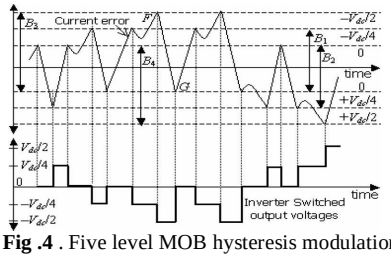

Fig .4 . Five level MOB hysteresis modulation.

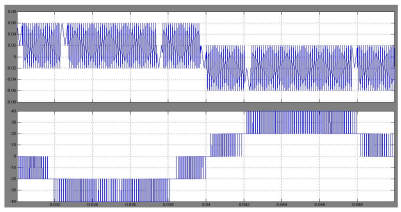

Fig. 5. MOB five-level hysteresis current control with fixed voltage applied at the band crossings of the current error. (a) Current error trajectory along with the allotted bands. (b)Inverter switched output voltage.

B. Modified MOB Hysteresis Modulation

To overcome the drawbacks of the multilevel control of Fig.5 a modified MOB (MMOB) hysteresis control is presented [16]. The band placement and functioning of MMOB scheme for a Five-level inverter is shown in Fig. 6. In this scheme, the current error is required to be bounded mainly between the bands $B1$ and $B2$, which are displaced by a small offset ΔB. Further, two additional offsets of the same width ΔB are placed out of $B1$ and$B2$ to provide a reliable and robust control.

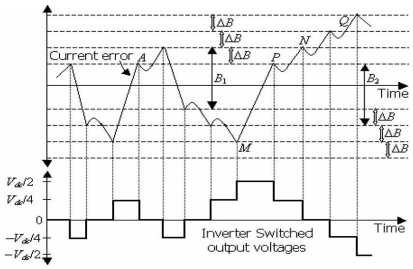

Fig. 6. MMOB five-level hysteresis modulation**.**

In general, a total number of $n - 2$ offsets are required for an n-level inverter in both the positive- and negative-current-error regions. It differs from the MOB method in the decision logic of output voltage levels at the crossing points of current error and corresponding boundaries of the hysteresis bands and also in the total number of bands required. In the MMOB approach, the applied output voltage at the band crossing points of current error is not fixed, but depends on the previous voltage level, i.e., just before the crossing point. In this scheme, the next voltage level is applied if a positive/negative boundary of $B1$ or $B2$ or ΔB is crossed with positive/negative slope for the first time. If this action is insufficient, the error will cross the same boundary second time. In such a situation, no action is taken until the next higher or lower boundary of another band is reached. This reduces the number of switching. If the current error crosses the positive boundary of a band with positive slope, next lower (than the previous) voltage level is switched. Similarly, if the error crosses the negative boundary of a band with negative slope, next higher (than the previous) voltage level is switched, with the earlier stated constraints applied. The advantage of MMOB method of Fig. 6 over the MOB method is evident in the manner that

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with MMOB method, output voltage quality is improved and the current follows its reference with minimum change in voltage levels needed. Another simulation study is performed using the MMOB scheme with the same inverter parameters as considered earlier and hysteresis band sizes as $B1 = B2 = 0.06$ A and $\Delta B = 0.02$ A. Fig. 7 shows the results. Similar current error trajectory analysis can be performed in Fig. 7 to justify the better waveforms using the control scheme of Fig. 6.

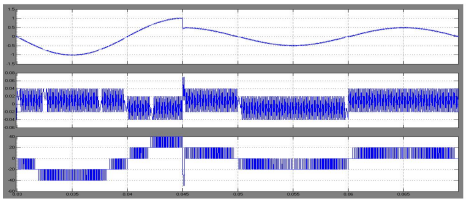

Fig .7. Transient performance of MMOB modulation.

A comparison of Fig. 7 with Fig.5 shows that in the new scheme, the switching always occurs between adjacent levels and no voltage level is skipped. Also, as opposed to MOB scheme, the current tracking performance remains uniform throughout a complete load current cycle in MMOB scheme, as the current error is mostly bounded within the hysteresis bands of same width. It should be noted that, in Fig. 5, the controller acts as desired when switching between +Vdc/4, 0, and −Vdc/4 and degrades when higher voltage levels (±Vdc/2) are needed to be switched. This indicates that fixed voltage-level switching as in [17] works fine for the three-level inverter and needs modification (as in Fig. 7) for higher level inverters. Fig. 7 shows the simulation results, obtained under the same transient condition, as considered in the previous sections. It is evident from Fig. 7(a)that the control technique is self-adapting in an automatic and natural way in the same manner as discussed earlier The fast-transient response of the current regulator can be appreciated from the results shown in Fig. 7(b). As the band sizes are small, it is difficult to distinguish between the load current and the alternating reference [dashed line in Fig. 7 (b)], which also confirms that the tracking is exact.

IV. TB HYSTERESIS MODULATION

The MB scheme, presented earlier in Section II, does not suffer from this steady-state-tracking error problem, but may still not have evenly symmetric current error waveform, especially for non sinusoidal current references. The MOB schemes are easy to implement [15], it requires offset compensation signals to be added to the controlled system variable, since the bands are not symmetric about zero. In the following, a TB MHM is first described, which works on the principle of controlling the system variable within a single band so that any type of current offset can be avoided. Then, a modified TB approach for MHM is discussed, which shows much better performances in terms of tracking as well as can be used with a limit on the maximum allowable switching frequency.

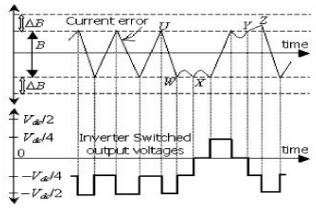

Fig.8.TB five-level hysteresis current control.

A. TB Multilevel Hysteresis Modulation

The TB multilevel hysteresis control scheme was proposed in [15] to use only one hysteresis band to detect an out-of bounds current error. But if the new inverter switched state is inadequate to reverse the error back to zero, the output is switched further down (or up) until the current-error direction reverses. A possible current error trajectory and inverter switched output for a five-level inverter are shown in Fig. 8. Referring to Fig. 8, the objective of this method is to force the current error in a manner so that it remains within band *B*. It is evident that the inverter output is switched one level up or down as the current error touches the boundary of *B*. If this changed output is insufficient to force the error back toward zero (as at*W*), next higher or lower voltage level is switched at the next crossing point of the error and the band limit (as at *X*). From Fig. 8, it is obvious that the technique does not create the steady-state tracking error of the MOB approach. To improve the performance and robustness of this technique, a current error slope detection algorithm was used in [18] to switch the voltage levels .An outer band was also placed to allow switching to the extreme voltage levels for rapid current error reduction during transient conditions (at ΔB out of *B*, Fig. 8). An additional band placement was also introduced in [19] for higher level inverters. Further, a lockout delay (TB control) was proposed to be added (in [20]) in the switching process for a fixed duration (say, $t1$) immediately after an inverter state changes to compensate for short delay between the generation of gating signals and sensing of the current error and its derivative. This TB approach can be seen in Fig. 8 between the instants *Y* and *Z*. It is evident that as the error keeps on increasing even if a voltage level change has occurred at *Y* , after a certain time delay ($t1$, between the instants *Y* and *Z*), another voltage level change at *Z* forces the error in the opposite direction. To further illustrate the principle and functioning of the scheme of Fig. 8, simulation studies are performed using this scheme with the same system conditions as considered earlier and $B = 0.04$ A and $\Delta B = 0.02$ A. fig. 9. Shows the results obtained. With the system parameters under consideration, it is evident that the current error is confined within band *B* by selecting the voltage levels one after another in the manner discussed earlier. the functioning of this scheme and observing the TB control, another simulation study is performed With the same parameters and two small-step changes in the reference current magnitude.

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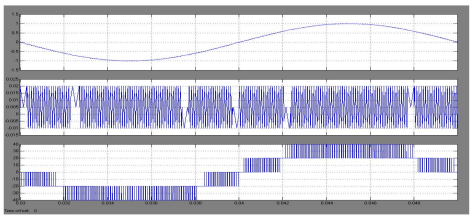

Fig.9. TB five-level hysteresis modulation.

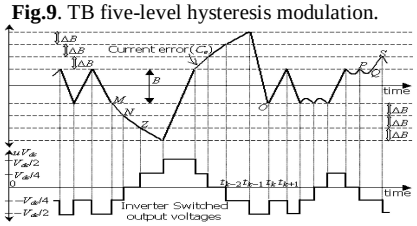

Fig.10. Modified TB five-level hysteresis current control.

Under certain loading conditions and/or for very narrow hysteresis band sizes, the current error variations are rapid. In these cases, the error may not reverse suddenly at the boundaries of *B* (if it has to), but may take some finite time (say, *t*2) depending on the applied voltage level, hysteresis band size, and the load parameters. This type of phenomena may also occur under synchronous detuning problem, which may occur in hysteresis control operation [21]. For these cases, let us suppose *t*3 be the time interval for which the current error slope is positive (or negative). Now, if *t*3 is more than the fixed delay *t*1 (defined earlier), the next higher or lower voltage level is switched after *t*1 according to the switching logic of [20]. This means that unnecessary voltage-level transition has taken place as the voltage level appearing just at the boundary of *B* was sufficient enough to force the current error direction (though, after *t*2). Therefore, it can be said that the current error slope detection with TB control may affect the hysteresis controller performance depending on various factors. A possible solution is to set a value of fixed delay *t*1 , which is large enough for any *t*3 . This means that the switching process is ceased for a large *t*1 , each time after the inverter output voltage is switched. However, the value of *t*1 is required to be tuned based on the parameters of the selected sensing device and differentiator logic [20]. Further, it has to be sufficiently small considering the size of Δ*B* (e.g., for the case when the error moves from the boundary of *B* toward outer boundaries at Δ*B*, Fig. 10). These considerations result in a very small value of *t*1 . Therefore, for varying load and under high-switching frequency operation, this is not a reliable solution. switching the voltage level if the current error slope is still positive (negative) after *t*1 from a voltage level change at *B*, are locked through *t*1 .

Modified TB Hysteresis Modulation

An efficient modified TB multilevel hysteresis control scheme was proposed in [16] and is shown in Fig. 10. This approach requires ($n-2$) outer bands at Δ*B* from their inner ones for an *n*-level inverter. Further, the current error slope-detection-based control is replaced by the algorithm of detection of only sign of the current error slope. The use of extra bands in the modified scheme implies that,. For example, as shown in Fig. 10, the time interval between the instants *P* and *Q* is considered smaller than *t*1 , and therefore, another voltage level change does not occur at *Q*. Subsequently, the error reaches at *S* so that a change in voltage level causes its reversal. Therefore, in effect, this method replaces the current error derivative detection control by a number of fixed-width bands. Defining the modified scheme of Fig. 10 with respect to the method of Fig. 8, it can be said that, the modified method replaces the combined monitoring of the vertical movement of the current error and horizontal movement of the time (of [20]) by only the single monitoring of the vertical movement of the current error in deciding to switch the next voltage level out of *B*. This replacement is logical as the main aim of all the hysteresis control remains to check the vertical movement of the switching decisions are taken only at the boundaries of the bands when the current error moves away from the zero line. At each such crossing, the inverter output is changed by one step (e.g., from 0 to +*V*dc/4, or to −*V*dc/4, etc.). In the lower boundary regions, the output voltage state changes from lower to higher (i.e., −*V*dc/2 to −*V*dc/4,−*V*dc/4 to 0, 0 to+*V*dc/4, nd+*V*dc/4 to+*V*dc/2) and in the upper boundary regions, from higher to lower (i.e., *V*dc/2 to *V*dc/4, *V*dc/4 to 0, 0 to −*V*dc/4, and −*V*dc/4 to −*V*dc/2). At the outermost boundaries, the corresponding extreme output voltage levels (+*V*dc/2 and −*V*dc/2) are applied for rapid current error reduction during transient conditions. These voltage level transitions ensure that the controlled current follows its reference with minimum control force needed. The switching strategy can be further understood from Fig. 10. At point *M*, the current error crosses the lower boundary of *B*. Before this point, the output voltage state was −*V*dc/2. Therefore, the next higher voltage level (−*V*dc/4) is applied at *M*. The current error then follows the path as shown, and at the crossing points shown in the figure ,voltage state transition takes place as mentioned earlier. A total number of ($n-1$) bands required for an *n*-level inverter in this scheme can be justified by following the current error trajectory in Fig. 10 and the discussions presented in the earlier presented schemes. It is also clear that it can efficiently work under varying load conditions as well. Based on the earlier discussion, the switching decisions under this scheme can be defined with respect to Fig. 10. for an *n*-level inverter as follows:

$$\text{if } \left\{C_e \geq 0 \text{ and } \frac{dC_e}{dt} > 0\right\}, \text{then } u(t_k) = u(t_{k-1}) + \frac{1}{n-1}$$
$$\text{if } \left\{C_e < 0 \text{ and } \frac{dC_e}{dt} < 0\right\}, \text{then } u(t_k) = u(t_{k-1}) - \frac{1}{n-1}.$$

In above equation, $u(t_k)$ is the current value of the switching decision, while $u(t_k-1)$ is its immediate past value. This can be justified from Fig. 10 in which, t_k-1 , t_k , etc., shown on the horizontal axis are the time instants at which *Ce* crosses the earlier defined boundaries of the

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bands. It can be seen that depending on the sign of Ce and dCe/dt , the output voltage level is either increased or decreased by *V*dc/4, at the crossing points. Note that, the inverter holds its output voltage level until *tk* , which it attained at *tk*−1. It is also to be noted that with *Ce* > 0, *dCe/dt* < 0, and with *Ce* < 0, *dCe/dt* > 0, no voltage transition takes place at the crossing points. This is because, in these regions, the control signal is heading toward zero line, which implies that the error between the controlled current and its reference value is reducing with the present output voltage level. Hence, no voltage transition is required for this. Another point to be noted is that, no exact evaluation is needed for the current error slope, as only the sign of the current error slope is needed at its crossing points with the band limits. At each sampling instant in the measurement process, the current value of the error is compared with its previous value. A positive value of this difference indicates a positive slope, while the negative value indicates a negative slope [16]. Therefore, this scheme does not suffer from noise amplification problem as in [20].
The value *t*1 (delay in the TB control) is taken to be 200μs. This value of *t*1 is purposely taken to be almost equal to the minimum time interval between two consecutive switching decisions under the given system conditions to have a better viewing of the controller performance. The simulated waveforms are shown in Fig. 11. It is evident that at *tq* , the error touches the upper boundary of *B* and the voltage level +*V*dc/4 is switched at the output of inverter to force the error in the opposite direction. However, at *tr* , when the error crosses the lower boundary of *B*, the next higher voltage level is not switched as the time interval between the instants *tq* and *tr* is less than *t*1 = 200 μs. Therefore, the error crosses *B* at *tr* and is forced back in the opposite direction at *ts* , i.e., at Δ*B* from the lower boundary of *B*, where voltage level +*V*dc/2 is switched. In this way, the current is controlled to follow its reference by using the four bands for a five-level inverter and a five-level output voltage waveform is obtained [see Fig. 11] for a sinusoidal reference current.

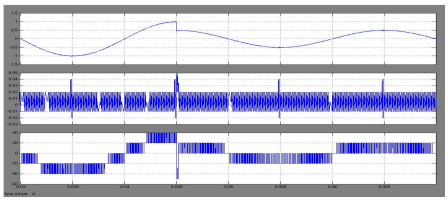
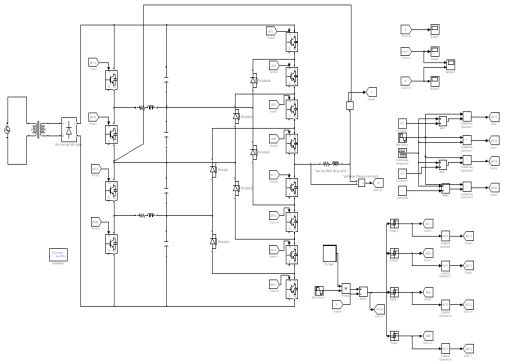


Fig. 11. Transient performance of modified TB scheme.

the experimental results correspond to the hysteresis band sizes of *B* = 0.04 A and Δ*B* = 0.02 A as considered earlier, while in Fig. 11, The results correspond to *B* = 0.06 A and Δ*B* = 0.03 A. The results have been obtained with two different band sizes to generalize the performance evaluation. It is evident from the figures that the current control is achieved by using the five voltage levels in the manner discussed earlier. The value of *t*1 = 200 μs is taken to be the same as used in the simulation studies.

V. Simulink Diagram:



VI. CONCLUSION

This includes, in general, the MB, MOB, and TB modulation techniques. The advantages of using various accessible dc voltage levels have been fully exploited by using these schemes. The various schemes considered in this paper have been further investigated using simulation and experimental studies for a five-level inverter system. However, these strategies can easily be extended to any multilevel inverter structure, even in the case of n-level voltage waveforms and three-phase systems.

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