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Electrostatic Mechanisms Responsible for Device Degradation in AlGaN/GaN HEMTs

Naveen kumar[1], Sunita Malik[2] , Amit Kumar[3], Parveen Kumar[4]
[1,2,3] *Electronics & Communication Engineering Department*
DCR University of Science & Technology Murthal, (HR), India
[4]*National Institute Of Technology (NIT)Kurukshetra, India*
[1] n.dahiya20@gmail.com
[2] sntmlk76@gmail.com
[3] *amitchaudharyji@gmail.com*
[4]*parveen.sura85@gmail.com*

ABSTRACT

The various factors that are responsible for device degradation are examined. The interplay between Non-Idealities in GaN HEMTs, traps, polarization, Origin of 2DEG, Current Collapse, Virtual gate, is analyzed and quantified. The various factors that helps in getting desired device characteristics regarding performance are studied and methods for achieving their satisfactory values are reviewed.

Key words: GaN, High Electron Mobility Transistor (HEMT), Polarization Charge, 2 Dimensional Electron Gas (2DEG).

1. DEVICE FUNDAMENTALS

The AlGaN/GaN HEMTs also known as the modulation doped field effect transistors (MODFET). Channel formation from carriers accumulated takes place along a junction between a lightly doped low bandgap region and a heavily doped high bandgap[1].Two dimensional electron gas (2DEG) is formed at the heterointerface. To achieve proper operation of the device, the barrier layer AlxGa1-xN must be at a higher energy level than the conduction band of the GaN channel layer. This conduction band offset transfers electrons from the barrier layer to the channel layer. The electrons that are transferred are limited to a small region in the channel layer near the heterointerface. This layer is called the 2DEG. Quality of the 2DEG is determined by type of substrate, growing method, and level of doping of the carrier supply layer [2].

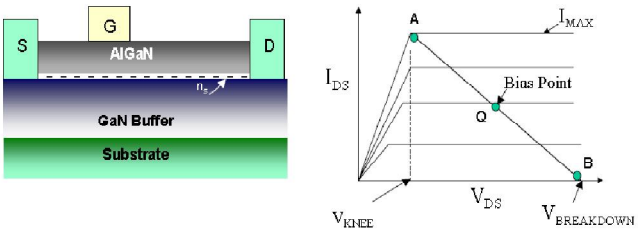

Figure 1: Biasing and load line graph for maximum power output

1.
2.
3.

MAX POWER = $[I_{MAX} * (V_{BREAKDOWN} - V_{KNEE})]/8$
$I_{MAX = k} * n_s * \mu$, where k is constant of proportionality, n_s are surface states, μ is mobility of carriers.
To make a good HEMT, we have to maximize current. To maximize current n_s and μ should be maximized. To maximize n_s, spontaneous and piezoelectric fields have to be maximized and to do so we have to maximize Al mole fraction without strain relaxation. To maximize μ, dislocations have to be minimized.

2. FACTORS RESPONSIBLE FOR DEVICE DEGRADATION

There are various factors such as traps, surface states, polarization, 2DEG formation etc. that are responsible for device degradation.

2.1 NON IDEALITIES IN HEMT [3]

Traps and dislocations present degrades the device performance. Due to trapping effects, the voltage swing, current swing reduces and knee voltage increases. Maximum output power decreases as voltage and current swing reduces. Drain Efficiency (DE) = (Vmax - Vknee) / (Vknee + Vmax). Thus Drain efficiency decreases as knee voltage increases. PAE = (1-1/G)(DE). Thus with decrease in drain efficiency, the power added efficiency (PAE) decreases. The traps can be present in S.I. substrate (if SiC), and GaN buffer interface, S.I. GaN buffer, AlGaN bulk, free surface of AlGaN.

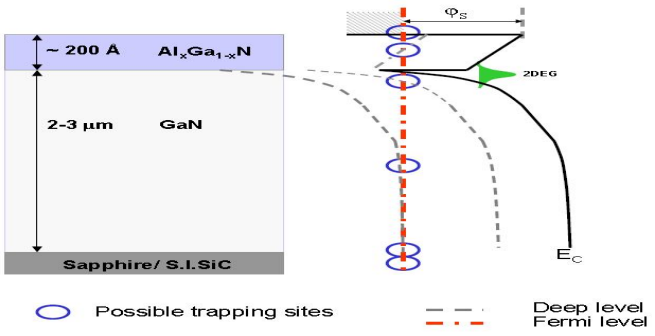

Figure 2: Possible trap sites

Due to non idealities present in the devices, the ideal I-V characteristics changes i.e. maximum current decreases and knee voltage increases.

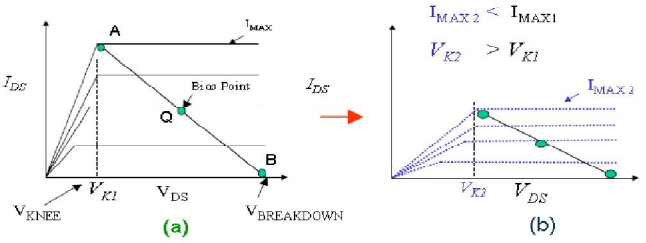

Figure 3: Effect of non-idealities on I-V graph

Figure 3 shows the effect of non idealities present in the devices.

2.2 POLARIZATION [4]

Due to large lattice mismatch between GaN and AlGaN, the piezo-electric polarization coefficient is large and hence piezoelectric polarization dipole and electric field are present in strained crystal.

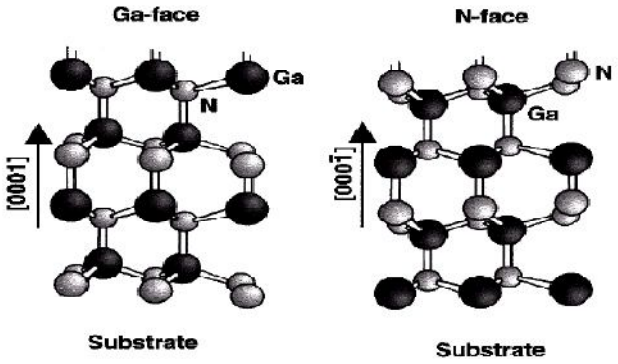

Figure 4: Crystal structure of GaN

Crystal structure of GaN shows difference in spontaneous polarization coefficients and hence spontaneous polarization charge sheet get induced in AlGaN. Lattice mismatch between GaN and AlGaN results in piezoelectric polarization induced charge sheet in AlGaN.

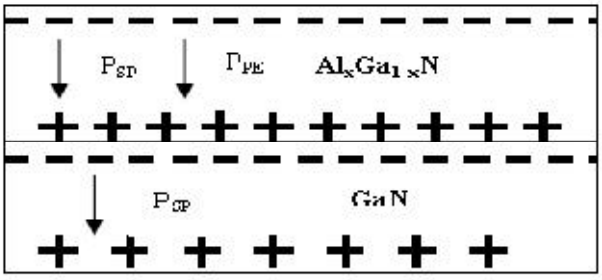

Figure 5: Combined piezoelectric and spontaneous fields for AlGaN grown on GaN

2.3 CURRENT COLLAPSE [5, 6]

Traps can directly trap electrons in channel i.e depletes the 2DEG density or can Trap charge elsewhere, creating a potential barrier to current flow or can trap charge underneath the metal gate, effectively changing the gate bias. These effects depicts that collapse should not be affected by surface treatment, a virtual gate spatially distinct from the metal gate and pinch-off voltage changes.

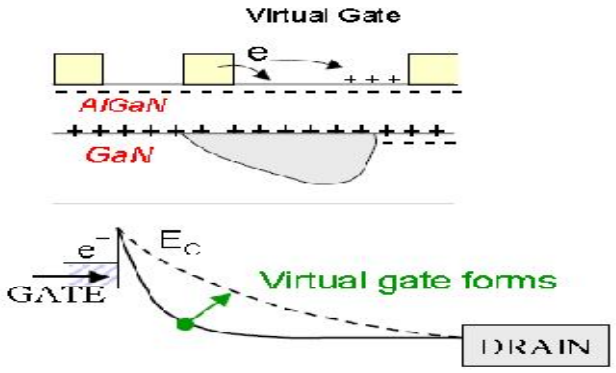

Figure 6: Virtual gate formation.

Bias and drive conditions cause the formation of virtual gate.V_{VG} is potential on virtual gate and controls drain current. After virtual gate is formed, the surface negative charge compensates the surface donor and 2DEG channel is depleted. Formation of virtual gate can be prevented by surface passivation.

2.4 2DEG FORMATION [7, 8]

In undoped AlGaN/GaN structures there exists a 2DEG at the AlGaN/GaN interface. Presence of polarization charge is not sufficient for 2DEG to form, thus polarization is not directly responsible for the 2DEG at AlGaN/GaN interface. There is no 2DEG formation until surface states empty into GaN. Thus surface states give rise to 2DEG formation.

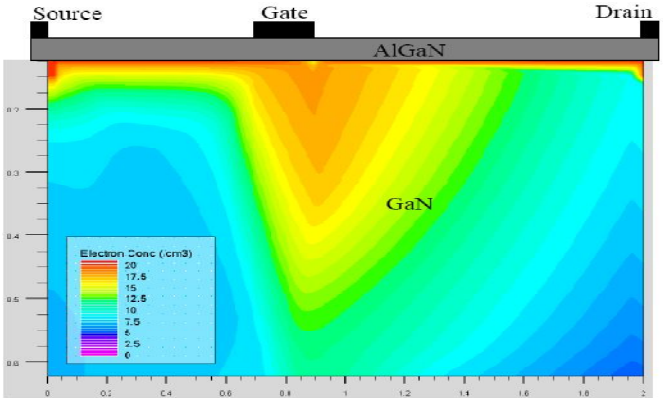

Figure 7: 2-D contours of electron concentration in an AlGaN/GaN HFET (*Vg* = 1V, *Vds* = 50V)

Figure 7 shows the electrons in GaN are distributed extremely close to the AlGaN/GaN heterojunction. There is a depletion

layer under the Schottky gate where the channel electrons right below the gate edge on the drain side are mostly depleted; therefore, the density of electrons in the bulk GaN exhibits a "V" shape.

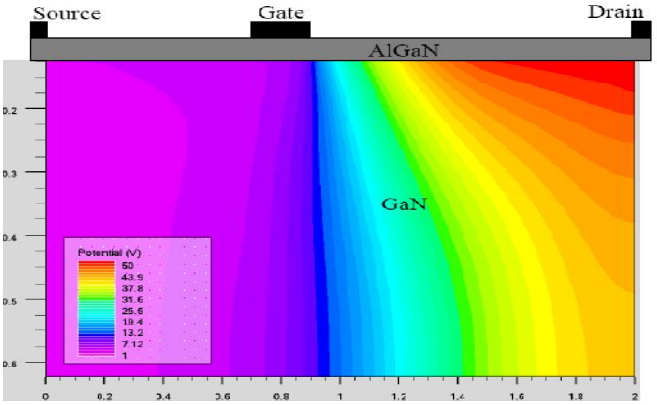

Figure 8: 2-D contours of potential in an AlGaN/GaN HFET (*Vg* = 1V, *Vds* = 50V)

Figure 8 shows that the voltage drop region increases and extends to the drain side as gate bias becomes more negative and drain bias becomes larger.

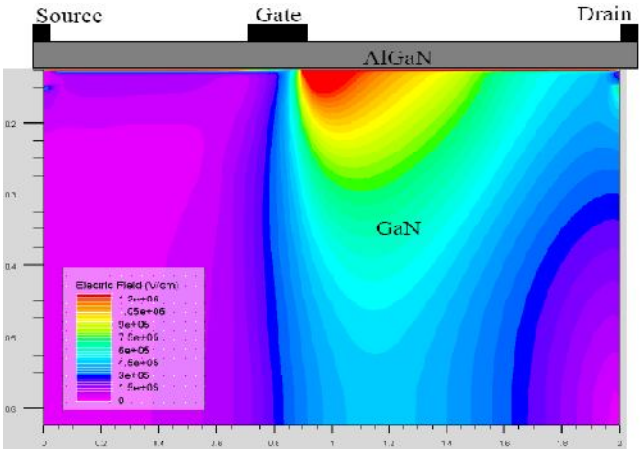

Figure 9: 2-D contours of lateral electric field in an AlGaN/GaN HFET (*Vg* = 1V, *Vds* = 50V)

Figure 9 shows that the field distribution is peaked at the gate edge of the drain side. The peak electric field increases as the gate voltage approaches pinch-off, and also as drain voltage increases. Therefore, high field conditions are attained at the lower right end of the load line when the instantaneous bias point sweeps the load line during RF operation.

3. CONCLUSION

Existence of a polarization dipole induces surface donor-like states. Surface donors give rise to the 2DEG and accept electrons making surface potential negative. Accumulation of negative charge in gate drain region creates a virtual gate. The spatial extent and potential of the virtual gate depends on bias and drive conditions. Current collapse is due to inability to modulate the virtual gate. Passivating the surface prevents formation of virtual gate, hence reducing current collapse.

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ABOUT THE AUTHORS

[1]***Naveen Kumar*** is pursuing his M.Tech Degree in Electronics & Communication Engineering from Deen Bandhu Chotu Ram University Of Science and Technology, Murthal, Sonepat, Haryana (INDIA). He received his B.Tech degree in Electronic & Communication Engineering from B.M.I.E.T, Sonipat (Affiliated to M.D.U Rohtak) in 2011. His research interest

includes Semiconductor Materials, Antenna And Wireless Communication.

[2]***Sunita Malik***, Assistant professor in the Department of ECE, Deen Bandhu Chhotu Ram University of Sci. & Tech. (DCRUST), Murthal (Haryana), India, has received her M.Tech. (ECE) from DCRUST, Murthal and B.Tech (ECE) from B.M.I.E.T, Sonipat (Affiliated to M.D.U Rohtak) in 2008 and 2005 respectively. Her main research interests are in Semiconductor devices and wireless communication. She has more than three years experience in academics.

[3]**Amit Kumar** is pursuing his M. Tech. from DCRUST, Murthal, Sonepat (India) in ECE. He recived his B. Tech Degree in ECE from Doon Valley Institute Of Engineering and Technology, Sonipat (Affiliated to KUK, Kurukshetra) in 2008. His current research interests include Semiconductor Materials, Antenna and wireless Communication.

[4]**Parveen Kumar** is pursuing his M. Tech. from National Institute Of Technology (NIT) Kurukshetra, (India) in VLSI DESIGN. He received his B. Tech Degree in ECE from B.M.I.E.T, Sonipat (Affiliated to MDU, Rohtak) in 2011. His current research interests include Low Power VLSI Design, Semiconductor Materials, Analog IC Design, Modeling Of Semiconductor Devices, RF Microelectronics Materials.