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Design and Implementation of Fault Tolerant FFT using Original Modules and Redundant Modules

Naganaik Mudhavathu [1], Dr.P.Karpagavalli [2]

[1] Research Scholar, [2]Associate Professor
[1,2] Department of Electronics and Communication Engineering
[1,2] Sri Satya Sai University of Technology & Medical Sciences, Bhopal, Sehore (M.P.)-466001
naganaik505@gmail.com

ABSTRACT

Fast Fourier Transformation (FFT) algorithm is a frequency transformation technique. The FFT method has a low complexity. The major parameters of a VLSI design are minimization in power consumption, delay and area. The conventional FFT technique has more hardware complexity because it has more computational elements. So this structure requires more look up tables (LUT) than other structures. The integration of large FFT architecture into a single chip will possible with the approach of deep submicron VLSI technology. The effective testing and fault tolerance methods are essential since a practical FFT chip is usually large. In this paper fault tolerated FFT network design will be proposed. The FFT circuit architecture with a spare-row will be proposed. The modern electronic devices will be get reliability threat from soft errors. So this indicates that, soft errors need protection to use it for various applications such as signal processing and communication system. In this technique to process a signal without soft errors with help of original module (OM) and redundant module (RM).This technique will be much useful fields like signal processing and communications. FFT is the major building block in many systems since it can be employed with various error detection and corrections (EDC) coding technique. So in this paper the design of a fault tolerant FFT will be implemented with original module, redundant module and error detection with correction technique.

Key words : Original module, fault tolerance, FFT, soft errors, VLSI, redundant module, LUT, and EDC.

1. INTRODUCTION

The FFT network design is much essential in the fields like communications and digital signal processing circuits. It has a great design approach for developing the any software or hardware fields. The various functions can be implemented in VLSI circuits based on single-path delay feedback (SDF) arrangement. Initially it's concentrate only on single radix computation. Recently this technique extends its computation capability to a multiple radix processing. This FFT method is broadly utilized in several signal processing and communication related applications. This system needs efficient operational speed, low power utilization, diminished truncation error and minimized chip size. By utilizing FFT numerical idea can be effortlessly developed in real time applications. It is likewise fit for changing the information starting with one mode then onto the next mode. OFDM is a emerging technique which can able implement so many practical life applications. The OFDM stands for orthogonal frequency division multiplexing. By using VLSI and system-on-chip (SoC) design technology in which millions of components were implemented on a single chip so it's possible to fabricate huge FFT network on a single chip. This technology can bring remarkable challenges and diagnosis. Especially the cost of the diagnosis increased rapidly with the complexity of the chip. So it's a very important to control the cost of a circuit design. Hence it's essential to implement a technique which works on fault detection. The fast growth of these VLSI technologies increases the complexity and decreased the feature size the components. So it's a highly complicated to get better accuracy and standards of chip. Therefore a technique called fault-tolerance will be required. Various testable structures and fault-tolerant design methods was developed to improve the exhibition of the chip testability and reliability of FFT systems.

The floating point based fault- tolerant FFT processor comprises of butterfly units with defect discovery circuit, switching circuit and control circuit as appeared in figure 1. This arrangement can make a perfect connection with shuffle. The control circuit can be able to control the switching circuit and it also arranges a transition which can be useful to determine the connections between output and input of butterfly units. There is a another method called modular redundancy (MR) which is used triples a block and select among three output in view of detecting and correcting errors. The soft errors mitigation techniques give a less system performance because it gives huge overhead in terms development of system. A method to detect and correct the

errors based on algorithmic properties of the circuit is known as algorithm-based fault tolerance (ABFT). This technique can limit the overhead that needs to ensure a network. ABFT technique will be well opted in the fields like VLSI and communication. To protect digital filters from overhead several methods were implemented.

The information about the distribution of the output of the filter is also utilized to detect and correct faults with lower overheard. It's also very important to protect FFT filters from overhead, because FFT will be used various applications.

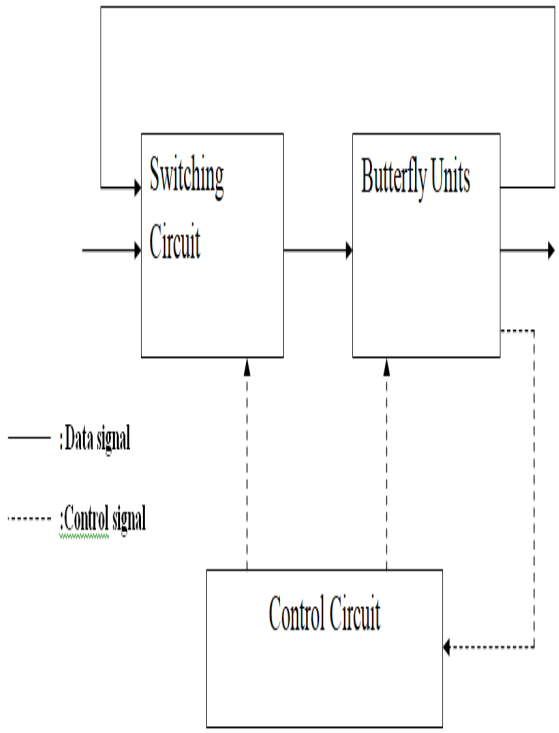

Figure 1: Block diagram for Floating Point- FFT.

A system will be proposed, that simply dependent on the error detection and correction codes (EDC). In this technique each filter can be considered as identical of a bit in an EDC and by utilizing addition operation the redundant bits are determined. The discrete Fourier transform (DFT) is one of the practical examples of this technique..In practical, to execute this procedure it is imperative to anticipate that there can be simply single fault on the system at any snapshot of time. For an assurance against radiation actuated soft errors, this is the basic expectation.

2 . LITERATURE SURVEY

It's a very essential to maintain better computing accuracy and deriving large discrete Fourier transform (DFT) while designing a digital signal processing circuit. This can be achieved by a FFT design. The FFT circuits are most preferable because this circuit gives better throughput and performance. Choi and Malek proposed a fault model scheme which was developed based on re-computation via another path. This is fault tolerance method implemented for FFT [4]. This technique decreases the throughput of a system so its requires maximum time overhead to protect the circuit. It's essential to determine FFTs or digital filters in parallel because the signal processing or communication circuits are became more complex. In digital filters or in communication based systems in which the circuits consist of MIMO structure. The MIMO stands for multi-input and multi-output. The OFDM was effectively used in various communication circuits. These two techniques are used together in FFT design for modulation and demodulation. This technique reduces power consumption, area and errors occurred in a circuit. The soft error mitigation method is used to reduce soft errors while designing any circuit. This technique requires a huge overhead for circuit development. The error detecting and correcting codes are needed to make a system as fault tolerant by the way of detecting and correcting the errors. At present a technique will be proposed to maintain a fault -free system, called error detection and correction codes (EDC). The technique that mostly uses the term butterfly for the computational issues is called Cooley–Tukey FFT algorithm. In this algorithm, the most frequently the large FFT can be broken into smaller.

In this method the sum of individual output is equal to the sum of some inputs. This is faithful to any operation that based on linearity. There are two redundancy methods to reduce the error in FFT network [5]. The NMR (N-module redundancy) is capable to definite error detection and correction. Though it's a optimized technique in terms of fault tolerance, but it consumes high rate of power. The overhead becomes doubled in typical triple modular redundancy (TMR) when compared to the conventional design techniques. A new technology was developed in 2006 by Snodgrass known as Reduced Precision Redundancy (RPR), the main idea of behind this technique is maintain a good balance in between calculation accuracy and power consumption. Another technique that was based on information redundancy is additionally, ABFT is capable to reducing the fault tolerance and errors in the circuit to better extent. Concurrent error detection (CED) is also a better information redundancy method to reduce the overhead [6]. For FFT design circuit computation, two conventional techniques are implemented. First Parseval's theorem based on sum of squares (SOS) check bit and convolution theorem. These two techniques has capable of reduce the overhead of the circuit and in turn protect the circuit in a effective way. The architecture of conventional FFT consists of three components such as Butterfly (BF2) architecture, Delay unit and commutator (C2) block. This architecture is most efficient proposal for better implementation of FFT algorithm for radix -2. This can rearrange the data easily for FFT/IFFT algorithm. In this technique, the FFT circuits with hybrid radix can be computed. For different FFT sizes the better reading and writing of data for data storage can be implemented by 2D-FIFO arrangement.

In this paper, an advanced technique called error detection and correction (EDC) will be developed for FFT based on original modules (OM) and redundancy modules (RM) with help of twiddle factor. In the fields like FFT and adaptive filters for linear operations the EDC will be much suitable.

3. FAULT TOLRENANT -FFT

Since there a drastic growth in the communications and signal processing fields, concept of IC technology evaluated and by using this technology millions of transistors are designed on a single chip. It decreases power consumption, size and area but in turn it is more sensitive to errors. So those faults or errors are minimized by using fault tolerance methodology. Two redundancy techniques are available. They are software redundancy or hardware redundancy and information redundancy. The coding that related to error correction or fault detection can be mainly processed with binary data. The binary data has two values such as binary 0 and binary1. So it is very easy to identify the faulty location. In computers the information is transferred by means of binary data. In the computers the special error correction techniques will be used to detect and then correct the errors with a great accuracy and precision. After correct the errors it can able to activate the operator in the sense that there exists a errors in the system. The input data is generally in binary form .The data in binary form will be derived from analog data using ADC. This conversion requires sampling and quantization operation to convert analog signal into digital signal. Original modules can transfers the same information to comparison section. Similarly input is also fed the comparison block but after it is passed through redundant module. The redundant modules filter the unwanted data so that its output is data without unessential data. The comparison block consists of two types inputs, one is original data and another one is a redundant data. After performing the comparison operation it sends the data to a butterfly unit. Both the FFT and Inverse FFT are almost same in terms of their mathematical notation with a small variation [1].

By applying the conjugate of the twiddle factors and with help of divide by N-point, the inverse FFT can be designed. Since FFT techniques are much useful in a advanced fields like communications, wireless designs and signal processing circuits design. Based on type of butterfly (BF) units are utilized for design, it will give different designs. The implementation of fast Fourier transform algorithms is purely based on the kind of butterfly unit chosen for development. A butterfly has a computational capability that merges the results larger FFT into a smaller discrete Fourier transforms (FTs) or vice versa. This can be made possible by splitting a FFT into smaller parts. Based on the appearance of the data flow diagram in the radix-2 representation, its name is butterfly [2]. A twiddle factor is any of the mathematical consistent coefficients and these are increased by the information over the span of the calculation. This factor used in signal processing fields especially in FFT. This factor can be represented as data-independent multiplicative constant in an FFT.

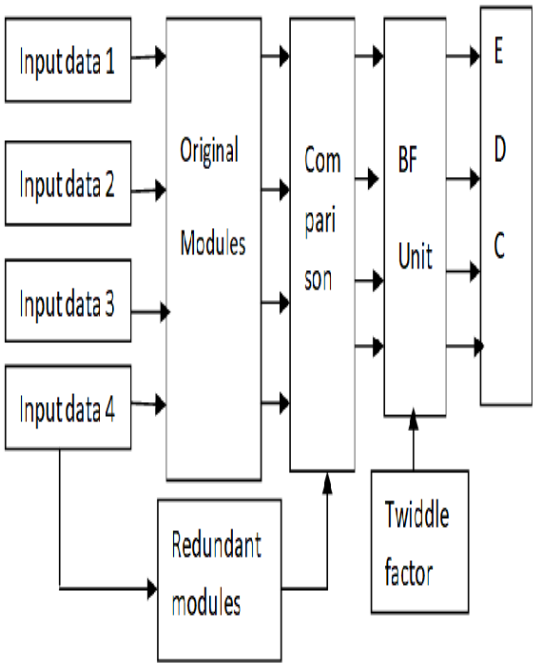

Figure 2: Block diagram of Fault tolerant FFT.

The protection is very useful in digital filters which are performed with help of error detection and correction (EDC) method. A hamming code which is a single bit error correction code is the example of EDC. The system with some inputs and one redundant module is given to determine errors. Here the input FFTs are directly given to inputs of the redundant module and implemented to verify linear combination of outputs [3]. In this process the FFT will have a linear operation and it is known as check bit, denoted with c_1. Similarly rest of the redundant modules will be generated a check bits, denoted with c_2 and c_3. Based on changes observed on each of the checks, it can easily determine the module with error. It is simple to detect and correct the errors by knowing the module with error.

4. RESULTS

In this section the fault tolerance fast Fourier transform (FT-FFT) design based on original modules and redundant modules related information like schematic diagrams, tables, output waveforms and various graphs that shows the relationship between different parameters , both in existed system and proposed FT-FFT will be described. The RTL schematic and technology schematic will be represented as shown in figure 3 and figure 4 respectively. The various parameters like number of slices, number of 4 Input LUTs (Look up table), number of bonded IOBs ((input/output block), delay for logic, delay for route and finally total delay can be decreased in FT-FFT system when compared to existed system. All these improvements can be possible by using fault tolerance method in FFT.

Table1: Experimental Parameters

Parameter	Existed System	FT- FFT
Slices	1376	1123
4 Input LUTs	2398	1941
Bonded IOBs	4772	3694
Delay for logic(ns)	26.30	22.48
Delay for route(ns)	25.74	21.62
Total delay(ns)	52.04	44.13
Total memory usage(MB)	376544	293726

Figure 3: RTL schematic of FT-FFT

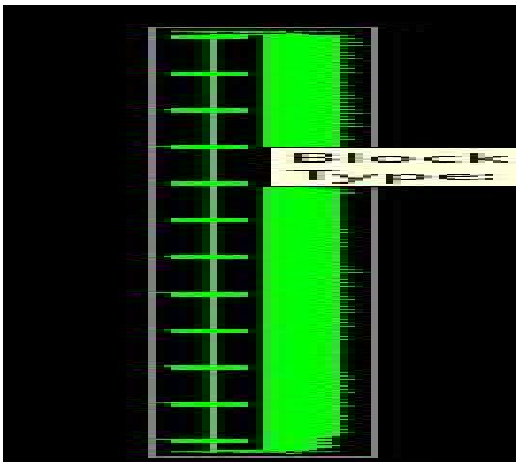

Figure 4: Technology schematic of FT-FFT

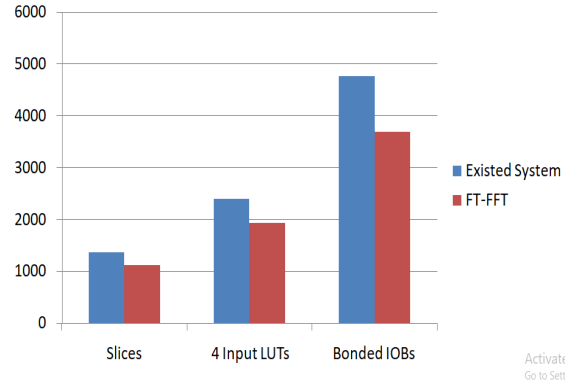

Figure 5: Comparison b/w slices, 4 input LUTs and Bonded IOBs

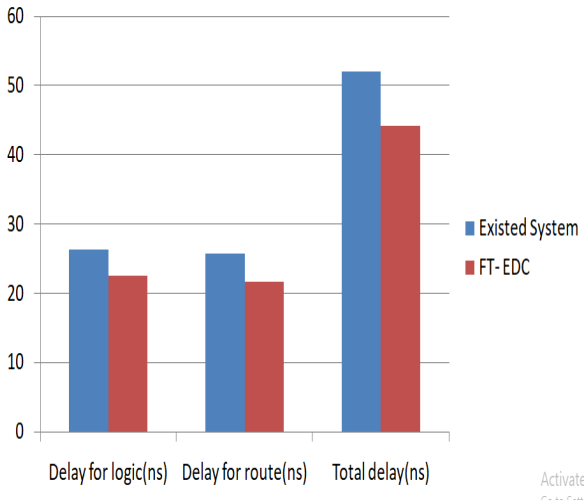

Figure 6: Delay comparison b/w Logic, Route and Total

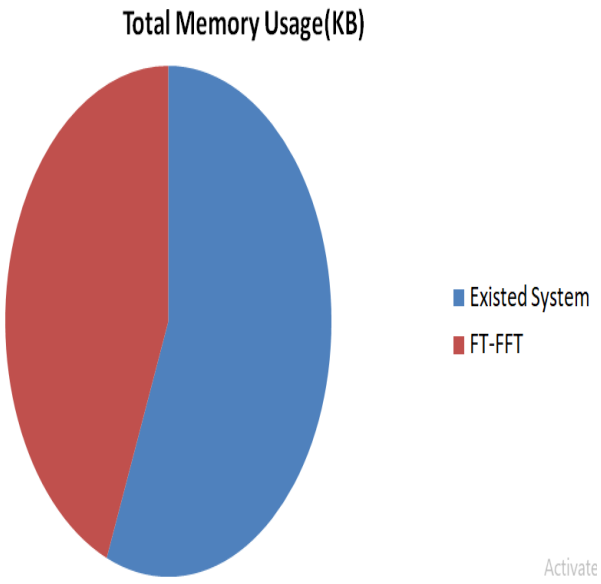

Figure 7: Memory Usage for Existed system and FT-FFT

The Comparison between slices, 4 input LUTs and Bonded IOBs with respect to the existed system and present FT-FFT are shown figure 5. By observing this graph, it can be concluded that compared with existed system in FT-FFT

system the number of components required to implement or develop an error free FFT device was reduced .This was possible by using error detection and correction technique. The variations with respect to the time delay for different parameters like delay for logic and delay for route is shown in figure 6. The total time delay is nothing but the sum of the logic and route delay. In the present FT-FFT system the total delay was much reduced over a existed one. This reduction was possible by reducing the delay time for logic and route by using efficient fault tolerance method like EDC. Finally the memory used is also reduced in FT-FFT system over existed system shown in figure 7.

5. CONCLUSION

The major parameters of a VLSI design are minimization in power consumption, delay and area. Fast Fourier Transformation (FFT) algorithm is a frequency transformation technique. The conventional FFT technique had more hardware complexity. All these problems were resolved by using fault tolerant FFT design. A fault-tolerant FFT network design technique has repaired a faulty row in the multiply–subtract–add module. This method was given more reliability, lower hardware. The integration of large FFT architecture into a single chip was possible with the approach of deep submicron VLSI technology. The error detection and correction (EDC) techniques with help of algorithmic rules was used to protect the circuit from more time overhead, with help of original module and redundant module. So in this paper the design of a fault tolerant FFT was implemented with original module and redundant module i.e. error detection and correction technique.

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