ISSN 2347 - 3983
Volume 9. No. 3, March 2021
International Journal of Emerging Trends in Engineering Research
Available Online at http://www.warse.org/IJETER/static/pdf/file/ijeter24932021.pdf
https://doi.org/10.30534/ijeter/2021/24932021

A Study of Different SRAM Cell Designs

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ABSTRACT

Presently, huge advancements are being witnessed in the electronics sector like AR, AI, driverless cars, smart homes, portable devices like mobile phones, etc. that requires the improvement of memory technology for efficient working. Memory plays a major role in the present scenario of improvements and growth. Out of different forms of memory devices, the most popular and presently used type of form is the semiconductor MOS memory, specifically SRAM (Static Random-Access Memory) that plays a very important role in the microprocessor domain as it covers a large portion of the chip. But with the increased scale of integration, leakage power, leakage current, and delay becomes a problem in the designing of an SRAM cell. This paper is a review of SRAM cells that have been proposed in the past for achieving improvement in SRAM cell parameters like power consumption, delay, leakage current, read and write stability, better cell operations, etc.

Key words : Cell area, low power, MOS, SRAM Cell, SRAM stability.

1. INTRODUCTION

SRAM (static random access memory) is a type of semiconductor random access memory that uses latches or flip-flops to store data, and the data in it is stored indefinitely provided the power is applied continuously. The other type of random access memory is the DRAM (dynamic random access memory), also a semiconductor MOS memory, that uses a capacitor and a transistor to store data. Both SRAM and DRAM are volatile memories. SRAM is more popular despite its high cost and low packing density as compared to DRAM because of its high speed, i.e., data can be read from the cell at a much faster rate from SRAM compared to DRAM. Also, SRAM does not need periodic refreshing like the DRAM. Thus, SRAM is a choice for designers in applications where high speed is a must, and the high cost of the cell is tolerable as in the case of cache memory designing.

In the present time, where portable battery-operated devices have become very common, power dissipation and area have become major concerns leading to the demand for small and low power consuming devices. Day by day, the scale of integration is increasing to meet the small-sized and high-density chips. This technology scaling results in instability in SRAM cell operations. Conventional SRAM cell suffers from various problems at smaller-scaled technology like leakage current, read stability, etc. To achieve a design that can work at smaller-scaled technology, various SRAM cells have been developed. Since there exists a trade-off between different parameters of an SRAM cell, so achieving all the aspects in a single design is not possible. Therefore, different designs depending upon different requirements in different applications are developed by focusing on the optimization of one or more parameters. This paper discusses various SRAM cells that consist of a different number of transistors and have some improved factors as compared to one another and the advantages and disadvantages of different SRAM cells are also seen.

2. DIFFERENT SRAM CELL DESIGNS

2.1 Conventional 6T SRAM Cell

The conventional SRAM cell [1] made of 6 MOSFETs is the most basic SRAM cell. Figure 1 shows the conventional 6T SRAM cell schematic. This cell consists of two access transistors and two cross-coupled inverters with a common read and write port. Asserting a high value to WL enables the access transistors for both read and write operations. For hold operation, WL is set to a low value.

ADVANTAGES: This cell is simple in design and consumes less area and thus can be used to design high-density memory chips.

DISADVANTAGES: This cell fails to maintain its stability at smaller-scaled technology. It suffers from read and write instability, has high power consumption, and increased access time when voltage scaling is done.

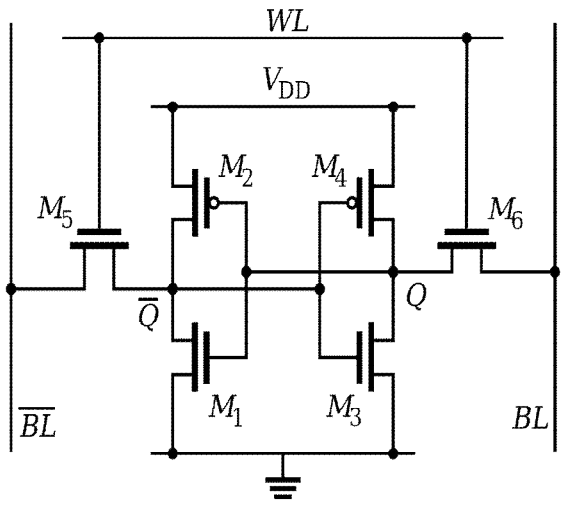

Figure 1: Conventional 6T SRAM Cell [1]

2.2 4T SRAM Cell

The 6T SRAM cell although being the basic SRAM cell still consumes more area as compared to the DRAM that has only one transistor and one capacitor. So, to achieve a reduction in area consumption by SRAM cell, a simpler design, i.e., 4T SRAM cell was designed as shown in Figure 2. The 4T SRAM consists of four NMOS and two poly-load resistors. The PMOS transistors of the 6T cell are replaced by very high polysilicon resistors to reduce transistor count and area consumed by the cell [2].

ADVANTAGES: This cell comprises of lesser number of transistors as well as consumes lesser area compared to the 6T cell.

DISADVANTAGES: This cell is sensitive to noise and soft error because of the very high resistances involved in the design.

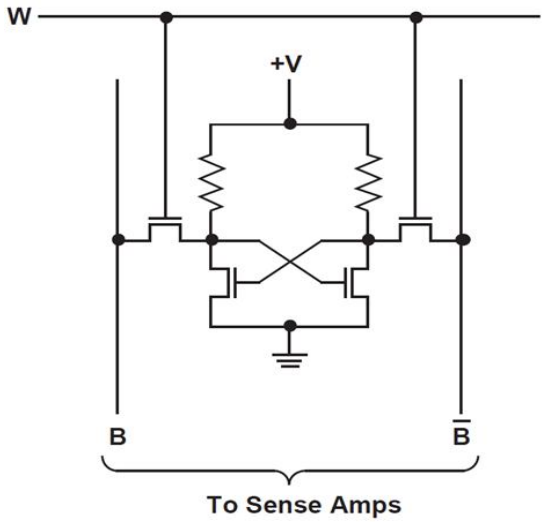

Figure 2: 4T SRAM Cell Schematic [3]

2.3 5T SRAM Cell

Figure 3 shows another SRAM cell designed to achieve area reduction and is obtained by removing one access transistor from the 6T SRAM cell giving a 5-transistor cell. This 5T cell has a single bit-line 'BL' [4].

ADVANTAGES: This cell has a significant area and power reduction as compared to 6T cell.

DISADVANTAGES: This cell suffers from difficulty in write '1' operation and relies on a particular cell sizing strategy to ensure correct write operation.

2.4 7T SRAM Cell

Figure 4 shows a 7T SRAM cell [5] that has an additional NMOS transistor N5 as compared to the conventional 6T SRAM cell. The write operation in this cell depends on removing the feedback connection between the two inverter pairs before the write operation, and the transistor N5 serves the purpose of feedback connection and disconnection. For writing in this cell, N5 is turned OFF. During the read operation, the cell behaves like a conventional 6T SRAM cell with N5 in ON state.

ADVANTAGES: This cell has better cell operation, and lower write power dissipation as compared to the conventional SRAM cell.

DISADVANTAGES: Due to the additional transistor, the cell area is 12.25% more than the 6T cell.

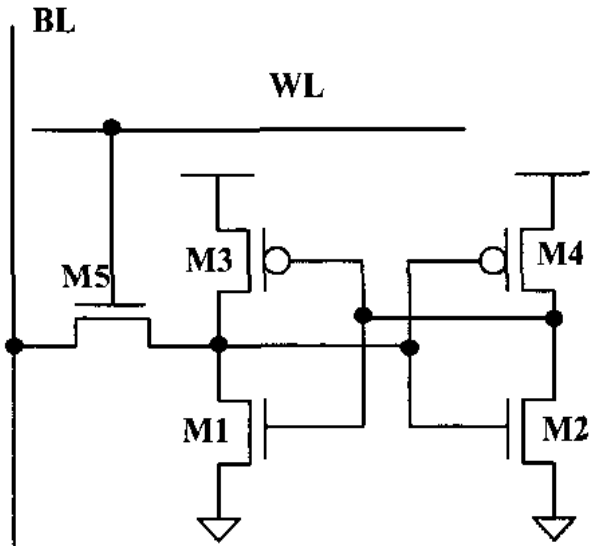

Figure 3: 5T SRAM Cell Schematic [4]

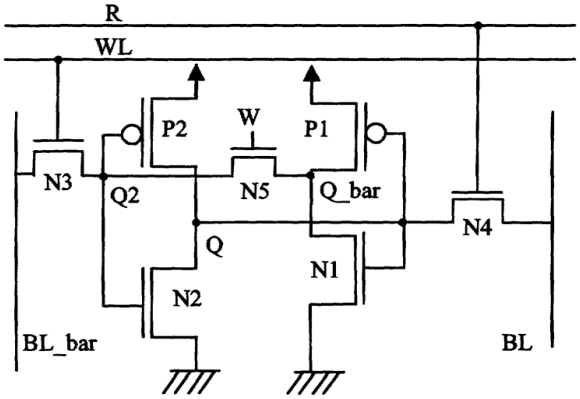

Figure 4: Schematic of 7T SRAM Cell [5]

2.5 8T SRAM Cell

Figure 5 shows the circuit diagram of the 8T SRAM cell. This cell consists of a separate circuit consisting of two additional NMOS transistors for the read operation. This read circuit provides a read mechanism that does not disturb the internal nodes of the cell and thus improves the stability of the cell. This cell has separate read and write word lines and accommodates dual-port operation with separate read and write bit lines [6].

ADVANTAGES: The 8T cell has better stability, higher SNM, and lower power consumption. This cell also allows for continued scaling compared to 6T cell that suffers from various issues when scaled down.

DISADVANTAGES: The 8T cell consumes 30% more on the chip as compared to the conventional 6T cell.

2.6 9T SRAM Cell

Figure 6 shows the schematic of a nine transistor SRAM cell. This cell is designed with the aim of improving stability and reducing power consumption. It can be viewed as a combination of two sub-circuits – the upper and lower sub-circuits. The upper sub-circuit is responsible for data storage, and the lower sub-circuit contains transistors for bit line access and read access. This cell uses a separate read signal that controls the read access transistor N7 [7].

ADVANTAGES: This cell has 7.7% less leakage power and also has better read stability as compared to the typical 6T SRAM cell.

DISADVANTAGES: The area consumed by this cell is 37.8% more than the 6T cell, and the presence of three stacked transistors in the read circuit increases the read access time.

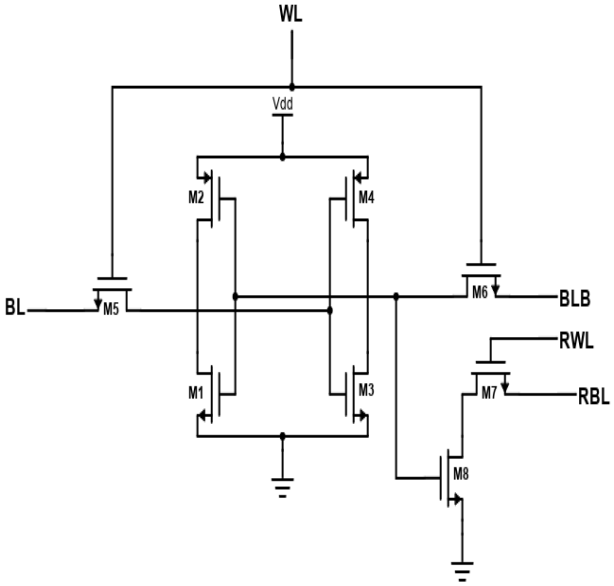

Figure 5: Conventional 8T SRAM Cell schematic [6]

2.7 DE PPN10T SRAM Cell

Figure 7 shows the differential-ended PPN10T SRAM cell that consists of ten transistors and uses a different version of the read path to achieve a reduction in the read access path's leakage current. As compared to the 6T cell, this cell has an additional signal VGND that is attached to GND only during read operation else it is connected to VDD. This cell uses PPN inverters. This design has two different storage nodes- the pseudo storage nodes (pQ and pQb) and the actual storage nodes (Q and Qb). These pseudo storage nodes present between the two series-connected PMOS transistors are responsible for providing an isolation mechanism between the bit line pair and the actual storage nodes during the read operation [8].

ADVANTAGES: This design has low power dissipation as compared to 6T cell and also works better at low sub-threshold voltage. Moreover, the separate read path in this cell increases the read stability of the cell.

DISADVANTAGES: Since the number of transistors is more as compared to the conventional SRAM cell so the area covered by the cell is more and the presence of two series-connected transistors in its write path, the write stability is degraded.

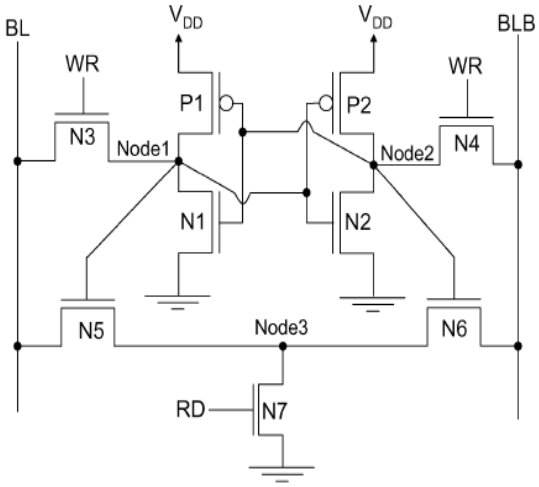

Figure 6: Schematic of 9T SRAM Cell [7]

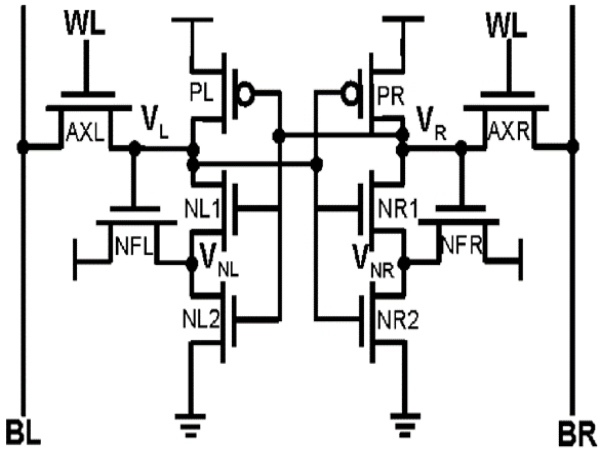

Figure 8: ST1 SRAM Cell [9]

2.8 ST1 SRAM Cell

Figure 8 shows the circuit diagram of the ST1 SRAM cell. ST1 cell is a Schmitt-trigger-inverter based SRAM cell consisting of ten transistors. A Schmitt-trigger-based inverter has a sharp transition as it has a feedback path and also offers higher SNM. ST1 is a differential 10T cell that has feedback transistors in its pull-down network. The positive feedback from NFL/NFR adaptively alters the switching threshold of the inverter based on the direction of input transition. The Schmitt trigger action is applied to preserve the logic "1" state of the memory cell [9].

ADVANTAGES: The ST1 cell has better noise immunity and does not require any change in the architecture compared to the 6T cell. Thus, it can be used as a drop-in replacement in designs based on 6T cell.

DISADVANTAGES: This cell suffers from read upset issue that is caused due to the voltage division between the Schmitt trigger inverter and the access transistors.

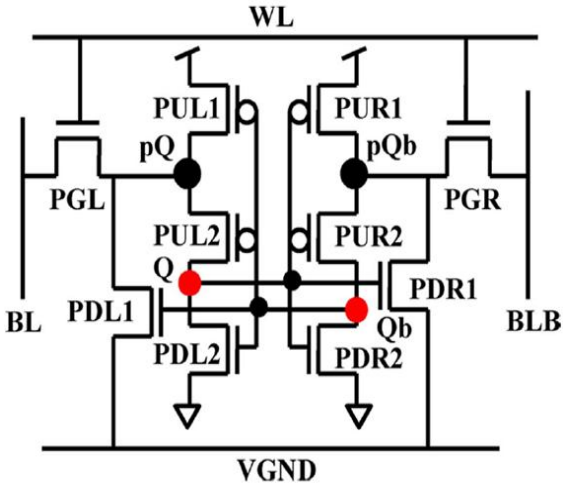

Figure 7: DE PPN10T SRAM Cell [8]

2.9 ST2 SRAM Cell

The ST2 cell is also a Schmitt-trigger-inverter based SRAM cell and consists of ten transistors. Figure 9 shows the schematic of the ST2 cell. This cell consists of an additional control signal to get stronger feedback for resolving the read upset issue that was present in the ST1 cell. This cell exploits differential sensing by the use of ten transistors, two word-lines, and two bit-lines. Both the word lines are activated for the write operation, and only WL is activated for the read operation [10].

ADVANTAGES: This cell resolves the read-upset issue present in the ST1 cell by using an additional control signal giving stronger feedback. It has enhanced read SNM and hold SNM as compared to the 6T cell.

DISADVANTAGES: This cell has two access transistors connected to the same bit lines that increase the load capacitance on bit lines. This higher load results in increased read access time.

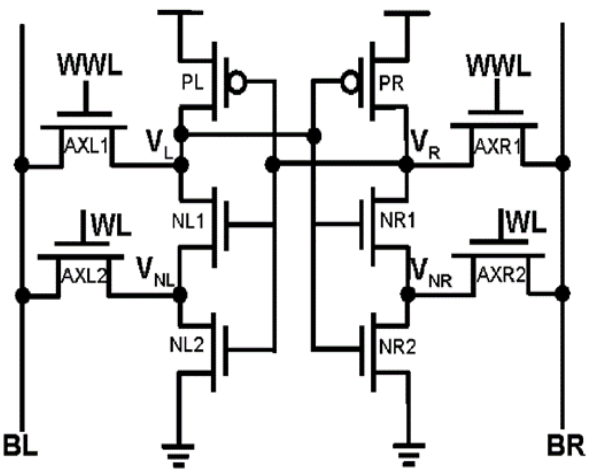

Figure 9: ST2 SRAM Cell Configuration [10]

2.10 LP10T SRAM Cell

Figure 10 shows LP10T SRAM Cell. LP10T or low power 10T SRAM cell is low leakage and low power SRAM cell that consists of 10 transistors and a XOR gate that takes write word line (WWL) and read word line (RWL) as input and its output controls the gate electrode of the tail transistor (MN7). The series connection of a tail transistor i.e. MN7 is the critical design strategy of this low power cell. To avoid read instability that could occur due to XOR gate and transistor MN7, read buffer made of transistors MN2, MN4, and MN8 is used [11]. The introduction of virtual ground path and differential decoupled read causes improvement in leakage power and noise margins respectively.

ADVANTAGES: This cell overcomes the problem related to read delay and static noise margin that is present in Schmitt triggered SRAM Cell.

DISADVANTAGES: This cell has meta-stability issue (caused by stack transistor MN8) that causes change in state of the cell even for a small gain in storage node voltage.

2.11 ST11T SRAM Cell

ST11T is another ST based cell consisting of 11 transistors, and it has a separate read decouple circuit with single-ended cell operation. Figure 11 shows the ST11T SRAM cell. This cell consists of cross-coupled ST inverters, a read path comprised of two transistors, and a write-access transistor. The internal storage nodes Q and QB are responsible for controlling feedback transistors of Schmitt Trigger, MNFL, and MNFR, respectively, with their drains attached with a control signal Wordline_bar (WLB) (complement of write enable signal) [13].

ADVANTAGES: Due to the feedback mechanism, this cell has increased data holding capacity. Also, this cell has reduced power and leakage current and improved read stability.

DISADVANTAGES: This cell has a failure to write '1' operation. Being a single-ended cell, it suffers from write access time and require write assist circuits to minimize write '1' access time.

3. SRAM CELL COMPARISON

Different cells are designed with different design goals and have different cell features. A comparison of cells based on different cell features is done and is shown in Table 1.

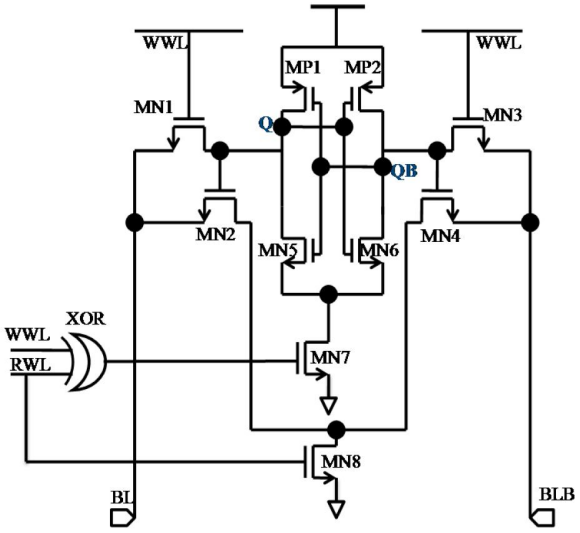

Figure 10: LP10T SRAM Cell Configuration [12]

4. CONCLUSIONS

The various SRAM cells have been studied. All the cells are different from each other. It is observed that in the designing of SRAM cells, there exists a trade-off between different cell parameters, and while cell designing these must be kept in mind. In the designing of SRAM cells, there are four very important design criteria which are cell density, access time, noise margin, and power consumption. Because of the trade-off between them, achieving all of these constraints at the same time becomes difficult. So, depending upon the application, the designing of the cell is focused on optimizing one or more of these design parameters [14]. We have observed that different cells are designed with different design goals like some are area-efficient, some are power-efficient, etc.

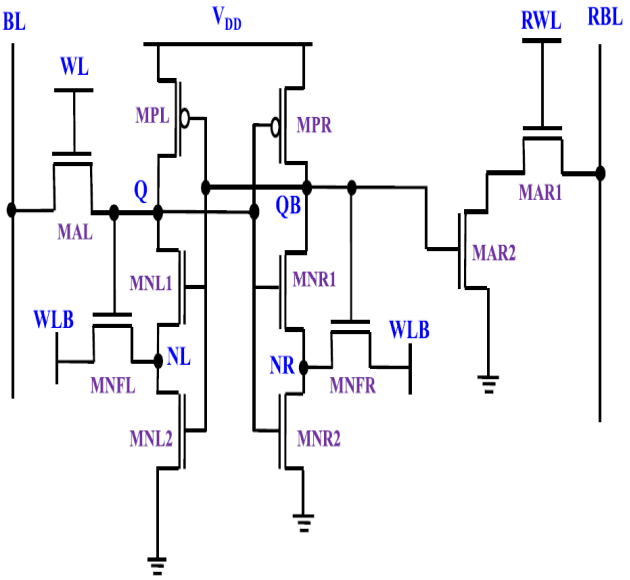

Figure 11: Single-Ended ST11T SRAM Cell [13]

Table 1: Comparison of SRAM cells based on different features

Features / Cell	Reading/ Writing	Bit lines	Control Signals	No. of NMOS in read path	Total no. of transistors
4T	Diff./Diff.	2-BL	1-WL	2	4
5T	SE/SE	1-BL	1-WL	2	5
6T	Diff./Diff.	2-BL	1-WL	2	6
7T	Diff./Diff.	2-BL	1-WL,1-W,1-R	2 or 3	7
8T	SE/Diff.	2-WBL,1-RBL	1-WL,1-RWL	2	8
9T	Diff./Diff.	2-BL	1-WR,1-RD	2	9
DE PPN10T	Diff./Diff.	2-BL	1-WL,1-VGND	2	10
ST1	Diff./Diff.	2-BL	1-WL	3	10
ST2	Diff./Diff.	2-BL	1-WL, 1-WWL	2	10
LP10T	Diff./Diff.	2-BL	1-WWL, 1-RWL	5	10
ST11T	SE/SE	1-BL,1-RBL	2-WL,1-RWL,1-VGND	2	11

Diff.-Differential, **SE**-Single-ended, **BL**-Bit Line, **WBL**-Write Bit Line, **RBL**-Read Bit Line, **WL**-Word Line, **W/WR**-Write, **R/RD**-Read, **RWL**-Read Word Line, **VGND**-Virtual Ground, **WWL**-Write Word Line.

5. FUTURE SCOPE

Apart from the different SRAM cells studied here, various other SRAM cells utilizing 7, 8, 9, 10, and even more number of transistors have also been designed to meet different design goals according to the requirement of the device. In the future, analysis of existing designs by applying various techniques for power reduction, voltage scaling, and stability improvement is possible. Also, since the present-day need is the designing of low power dissipating devices, so the optimization of designs, to achieve power consumption reduction can be done. The device area is also an important parameter nowadays, and thus, designing of new SRAM cells that consume low power and consists of less number of transistors can be done.

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