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HIGH-FREQUENCY CMOS DIGITAL CIRCUITS WITH EFFICIENT POWER UTILIZATION USING REPLICA BIAS SCHEME

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ABSTRACT

Computerized circuits displaying rail-to-rail voltage swings show vast spreads in current utilization and delay over varieties in procedure, voltage and temperature (PVT). A circuit method is proposed to empower ideal current utilization and low delay appropriation in high frequency advanced circuits. A common RF application is picked at 5 GHz recurrence, for which a divider is outlined and reenacted in an UMC 130nm CMOS process. With the proposed scheme, the circuit shows up to 52% reduction in current, while the relative variation in delay over PVT reduces by 70%.

Key words: CMOS, Digital Circuit, Frequency, rail-to-rail voltage, UMC.

1. INTRODUCTION

Radio frequency (RF) transceiver styles favor customary CMOS processes for easy integration and to cut back price and power consumption. With ever-reducing gate delays, increasingly larger range of high frequency digital functions like CMOS circuits that swing fully between the rails. These circuits scale without delay and lend themselves to easier implementation compared with people who work underneath restricted swings. Whereas achieving the desired functions with bottom power dissipation is often fascinating, this is often extremely vital over all operative conditions in mobile RF applications to cut back recharge cycles.

Variations in method corners cut back the benefits gained through technology scaling and this is often foretold to urge worse within the future [1]. Changes in temperature and provide voltage additionally have an effect on cell delays considerably. Raising the present consumption to accommodate the big unfold in cell delays is that the simple however inefficient resolution.

This work proposes a circuit technique that reduces the unfold in delay and power consumption and applies it to a frequency divider employed in RF frequency synthesizers. In general, any commonplace CMOS digital circuit can be created economical and sturdy through the projected approach. During this paper, section II introduces a typical application for the projected technique and explains the standard implementation of the digital circuit. Section III explains the variations in key parameters over PVT and section IV introduces the projected design and discusses the results.

II. FEEDBACK DIVIDER IN RF FREQUENCY SYNTHESIZERS.

A. Conventional Divider Design

The chosen RF application targets the two.4 gigacycle per second philosophical system band. this needs the VCO and divider to work nominally at four.8 gigacycle per second (to generate I and Q parts at two.4 GHz), that the divider is fixed to operate at five.6 gigacycle per second over corners to permit for loop transients together with some margin.Fig.1 shows the divider design supported [2].

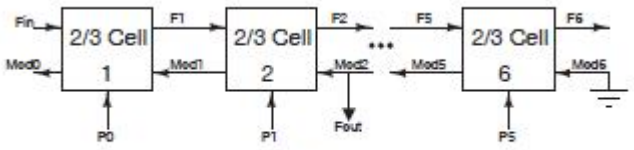

Fig. 1: Divider architecture.

The synthesizer input frequency comes from a forty megahertz oscillator. The specified division issue (N) is nominally a hundred and twenty; therefore the style needs six divide-by-2/3 cells. The circuit style deviates to a small degree from [2] because of the employment of True single part continuance (TSPC) flops instead of Source-coupled logic (SCL) flops. The interior topological details of the 2/3 cell square measure are shown in fig. 2 and 3. The combinable logic, aside from AN electrical converter, is absorbed within the flop to scale back propagation delay and current consumption. Solely the primary 2 2/3 cells use TSPC logic; whereas the succeeding cells use static CMOS flops to scale back power.

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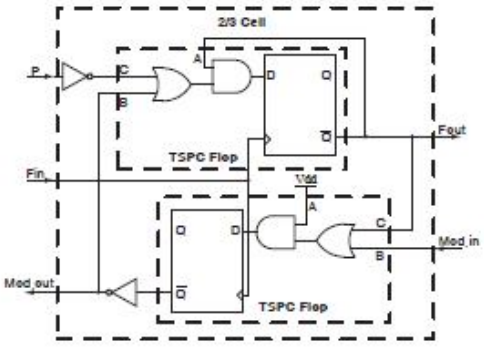

Fig. 2: Implementation of 2/3 cell.

B. Conventional Divider Simulation Results

The power dissipation and the clock-to-output delay

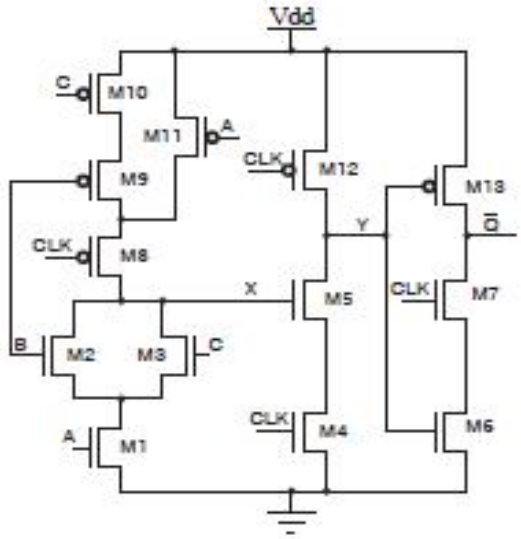

Fig. 3: Implementation of TSPC flop.

Show 2x and 2.5x variation over PVT respectively. The sensitivity of current consumption to PVT reduces because the frequency of operation decreases, as a result of the rise in idle time between transitions. If the whole circuit were to figure at the utmost frequency, the spreads full-fledged would be a lot of larger.

III. POWER AND DELAY OPTIMIZED DIVIDER

A reference is needed to form the availability voltage of the divider track the method and temperature variations. Fig. five shows a self biased electrical converter and a hoop generator each biased with a temperature and method freelance current (IBG). The voltage Vref generated by IBG would behave just like the desired reference. once the method corner or temperature reduces the drive strength of the devices, Vref will increase. If this Vref is employed to provide the divider through a regulator, the ensuing offer voltage might catch up on the variations in method and temperature. this can be a replica-bias theme wherever the electrical converters area unit forced to work on a set current owing to a master inverter biased at a continuing current because the inverters work on a current that's freelance of PVT, they're expected to own constant delays too. This work focuses on the utilization of reproduction bias derived offer for digital circuits. Similar works are reported before for analog circuits however targeting offer rejection [3],[4]. Sensitivity to method and temperature primarily comes from the bias current in circuits performing arts analog functions. Therefore, offer generated through replica-bias wouldn't be effective in dominant process and temperature-induced variations. Prosperous implementations of styles amendment the bias current in accordance with the availability [5].

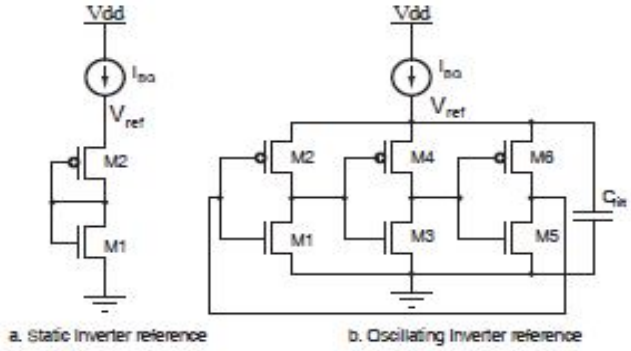

Fig. 5: Supply reference options.

A. Reference choice so as to cut back the unfold, the I-V characteristic of the reference ought to match that of the inverters within the flop and should conjointly track any variations arising from offer and temperature changes.Fig.6 shows electrical converter current planned against input voltage at a continuing power offer (Vdd). The profile of current drawn by the electrical converter for a complete undulation at the input1 is additionally shown because the inverters swing, they get biased at a mean current of I1 (Vdd two , I1). However, the transistors within the reference branch in fig. 5(a) area unit static and bias the electrical converter at (Vdd two , I0), creating it ineffective in providing a decent match with the inverters within the flop.

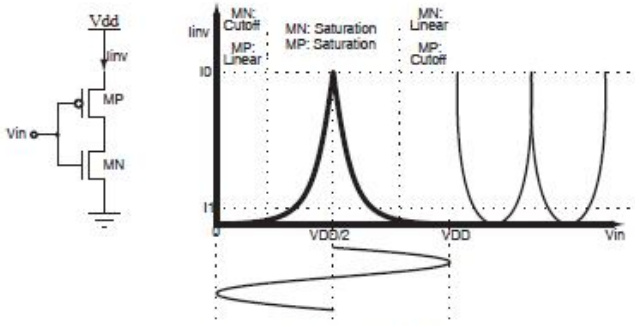

Fig. 6: Inverter I-V characteristic.

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The ring generator primarily based reference in fig. 5(b) doesn't suffer from the issues represented on top of and their inverter is created to match the characteristics of these within the flop fairly well the entire theme is illustrated in fig. 7. The ring generator bias current is chosen such the generated offer voltage (V DDDIV) permits the divider to control over the desired frequency vary, whereas providing enough drop-out voltage for the regulator semiconductor to stay in saturation. The ring generator is meant to minimize this current whereas maintaining smart match with the inverters within the flop.

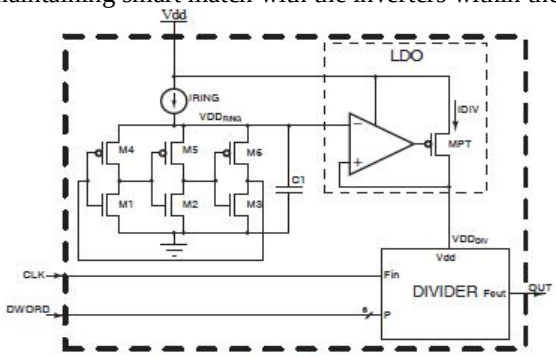

Fig. 7: Proposed power efficient divider.

A level shifter is also wont to translate the output (OUT) to VDD levels. However, during this application, it'd be useful to work the phase-frequency detector and charge- pump on an equivalent regulated provide. The delays in those modules too would be tightly controlled, resulting in low reset path delays ultimately leading to tighter static part error distribution.

B. Regulator design

The low drop-out regulator (LDO) has associate degree NMOS input stage and PMOS common supply second stage attributable to the input voltage vary and drop-out voltage limitations severally (fig.8).The dominant and initial non-dominant poles square measure placed at the gate of the pass semiconductor (MPT) and therefore the output node severally. Miller electrical condenser Cc performs pole-splitting to supply a section margin of 50◦.As the dominant pole isn't at the output, the load transient response is comparatively poor, however is taken into account adequate for this application (fig. 9). Cbypass denotes the parasitic capacitance on the provision of the divider it's assumed to be restricted to 50pF within the simulations.

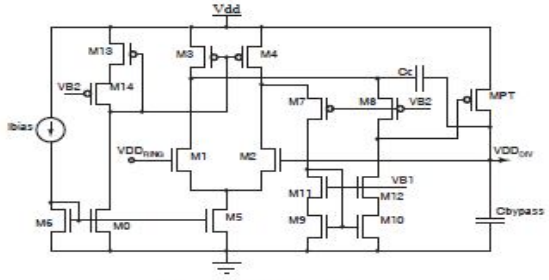

Fig. 8: LDO schematic.

The ring generator consumes 100uA whereas the LDO consumes solely 10uA. Therefore, the facility overhead for the extra blocks isn't terribly important. The start-up transient of the regulated provide voltage is shown in fig. nine for 3 representative cases within the typical transistor corner with the facility provide and temperature set to one.2V and 27◦C respectively, the regulated voltage settles to 867mV. within the slow semiconductor unit corner, 1.08V power provide and 100◦C temperature, the transistors show poor drive strength, that the regulator output voltage will increase to 1V to take care of an equivalent delay within the inverters. Within the quick semiconductor unit corner, 1.32V power provides and -40◦C temperature, the regulated voltage reduces to 767mV befittingly. C. Results and outline the results for the planned divider square measure shown in Table III. This consumption and clock-to-output delay square measure shown across the everyday and worst-case corners in fig. 10. The reduction in current consumption is forty third and sixty seven within the typical and extreme case severally. The variation in clock-to-output delay within the original divider was -39% to fifty three. This reduces to a variation of -11% to nineteen within the planned circuit.

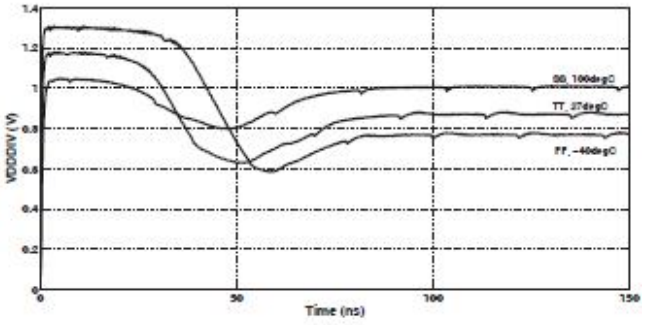

Fig. 9: Divider supply voltage transient across PVT.

It should be noted that because the offered provide voltage for the divider is reduced during this theme, the warranted most frequency of operation falls slightly. The current consumption is premeditated across input clock frequency for identical division magnitude relation (120) within the typical semiconductor corner (1.2V, 27◦C) in fig. 11(a). The currents increase linearly with frequency, obviously. The potency of the planned circuit over the traditional divider is portrayed in fig. 11(b).This potency improves as circuit activity will increase, either through increase in shift rate or by shift a lot of nodes at a set rate. Therefore, because the needed optimum current will increase, the planned circuit seems progressively engaging, creating it well-suited for top power or high frequency digital circuit applications. The benefits of the planned divider could also be summarized as below:

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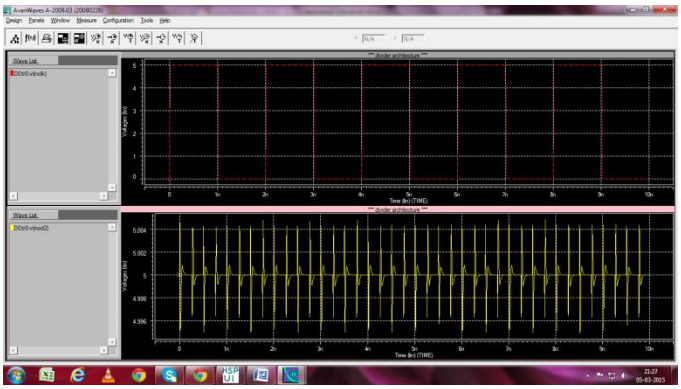
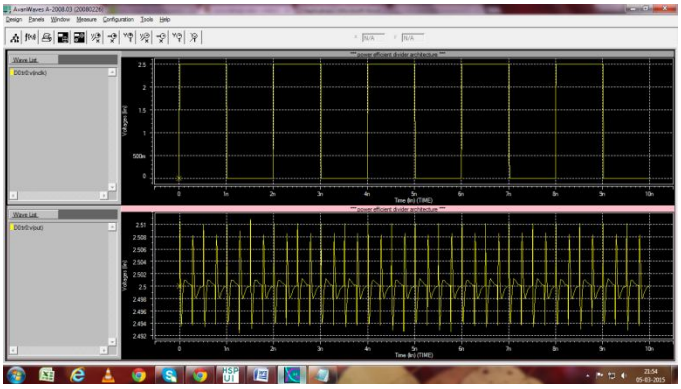
IV. ADVANTAGES

1) Current consumption is decreased across variations in PVT. This reduction gets higher if a bigger portion of the circuit switches at high frequencies.
2) The variation in delay over PVT becomes smaller. This ends up in higher utilization of the offered time in those applications wherever temporal arrangement is important.
3) The divider module works beneath a regulated provide and is so secure from noise on the external provide. This leads to low provide induced disturbance. in addition to low delay variation, this translates to a linear divider that is very fascinating during a fractional-N synthesizer.
4) The power potency over the standard divider in- creases linearly with the specified current consumption.
5) The divider encapsulates a method monitor; the LDO output is associate analog live of the method. This in- formation may well be used for different functions like trimming associate analog module or serving as a record throughout take a look at.



frequency division with rmspwr-= 1.0915E 03W



rmspwr= 2.1924E-04

The average power reduced by 79%

V. CONCLUSION

The sub-optimal utilization of power in normal CMOS digital circuits was analyzed. A way to boost power potency was incontestable exploitation the instance of the frequency divider in associate RF frequency synthesizer. It absolutely was shown that an operative digital circuit with reproduction bias derived from the same low-power module manages to stay the ability consumption near the minimum doable over producing and operational variations. An extra favorable result was improvement in immunity from offer noise.

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