Variable Body Biasing (VBB) Based VLSI Design Approach to Reduce Static Power

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Abstract— **In CMOS integrated circuit design there is a swap among static power consumption and technology scaling. Recently, the power density has improved due to combination of higher clock speeds, greater functional integration, and smaller process geometries. As a result static power consumption is becoming more dominant. This is a challenge for the circuit designers. However, the designers do have a few methods which they can use to reduce this static power consumption. But all of these methods have some drawbacks. In order to achieve lower static power consumption, one has to sacrifice design area and circuit performance. In this paper, we propose a new method to reduce static power in the CMOS VLSI circuit using Variable Body Biasing technique without being penalized in area requirement and circuit performance.**

Keywords— *variable body biasing, state saving technique, stack effect, dual V-th, static power reduction.*

I. INTRODUCTION

CMOS technology feature size and threshold voltage have been scaling down for decades for achieving high density and high performance.Because of this technology trend, transistor leakage power has increased exponentially. As the feature size becomes smaller, shorter channel lengths result in increased sub-threshold leakage current through a transistor when it is off. Low threshold voltage also results in increased sub-threshold leakage current because transistors cannot be turned off completely. For these reasons, static power consumption, i.e., leakage power dissipation, has become a significant portion of total power consumption for current and future silicon technologies. There are several VLSI techniques to reduce leakage power. Each technique provides an efficient way to reduce leakage power, but disadvantages of each technique limit the application of each technique. We propose a new approach, thus providing a new choice to low-leakage power VLSI designers. Previous techniques are summarized and compared with our new approach presented in this paper.

II. PREVIOUS WORKS

We here review previously proposed circuit level approaches for sub-threshold leakage power reduction.

A. Sleep Transistor Approach

The most well-known traditional approach is the sleep approach [1] [2] (Fig. 1). In the sleep approach, both (i) an additional " sleep" PMOS transistor is placed between VDD and the pull-up network of a circuit and (ii) an additional " sleep" NMOS transistor is placed between the pull-down network and GND. These sleep transistors turn off the circuit by cutting off the power rails. By cutting off the power source, this technique can reduce leakage power effectively. However, the technique results in destruction of state plus a floating output voltage in sleep mode.

B. Sleepy Stack Approach

The sleepy stack approach combines the sleep and stack approaches [3] [4] (Fig. 2). The sleepy stack technique divides existing transistors into two half size transistors like the stack approach. Then sleep transistors are added in parallel to one of the divided transistors. During sleep mode, sleep transistors are turned off and stacked transistors suppress leakage current while saving state. Area penalty is a significant matter for this approach since every transistor is replaced by three transistors.

C. Sleepy Keeper Approach

Sleepy keeper utilizes leakage feedback technique [5] (Fig. 3). In this approach, a PMOS transistor is placed in parallel to the sleep transistor (S) and a NMOS transistor is placed in parallel to the sleep transistor (S'). The two transistors are driven by the output of the inverter. During sleep mode, sleep transistors are turned off and one of the transistors in parallel to the sleep transistors keep the connection with the appropriate power rail.
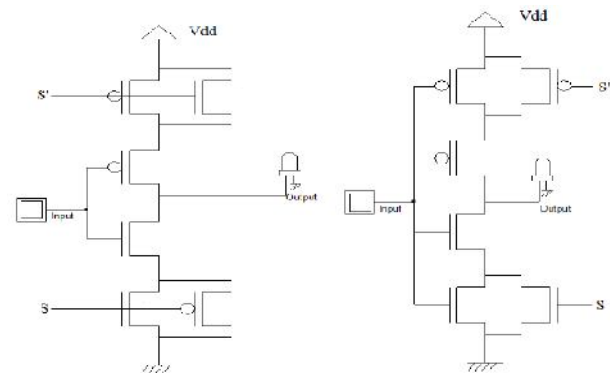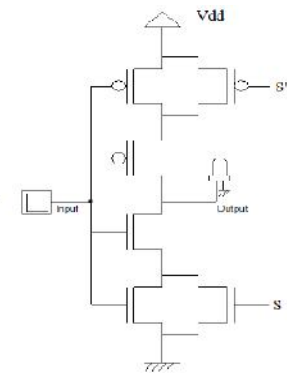

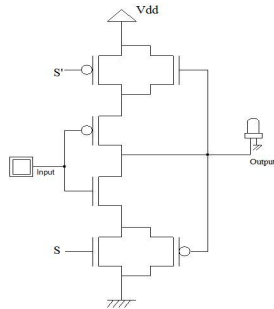Fig. 1 Sleep Approach   Fig. 2 Sleepy Stack

Fig. 3 Sleepy Keeper

D. Dual Sleep Approach

Dual sleep approach [6] (Fig. 4) uses the advantage of using the two extra pull-up and two extra pull-down transistors in sleep mode either in OFF state or in ON state. Since the dual sleep portion can be made common to all logic circuitry, less number of transistors is needed to apply a certain logic circuit.

E. Dual Stack Approach

In dual stack approach [7] (Fig. 5), 2 PMOS in the pull-down network and 2 NMOS in the pull-up network are used. The advantage is that NMOS degrades the high logic level while PMOS degrades the low logic level. Compared to previous approaches it requires greater area. The delay is also increased.
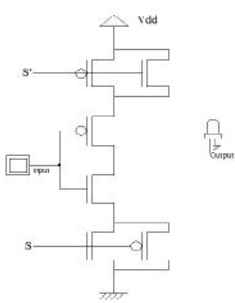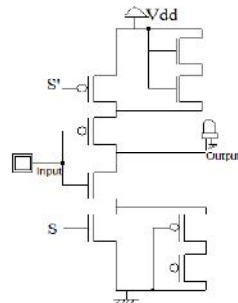

Fig. 4 Dual Sleep

Fig. 5 Dual Stack

III. VARIABLE BODY BIASING APPROACH

To reduce the leakage current in the sleep mode we ensured that the body to source voltage of the sleep transistor is increased. To do that we added a PMOS(M2) and a NMOS (M5) in the previously discussed sleepy keeper circuit (Fig.6). During sleep mode PMOS (M2) is OFF so the body to source voltage of the pull up PMOS (M1) is higher than in the active mode. For a turned off single transistor leakage current (Isub0) can be expressed as follows:

$$I_{sub0} = Ae^{\frac{1}{nv_\theta}(v_{gso}-v_{th0}-\gamma v_{sbo}+\eta v_{dso})}(1 - e^{\frac{-v_{dso}}{v_\theta}})$$

Where, $A=\mu_0 C_{ox}(W/L_{eff})V_\theta^2 e^{1.8}$;n is the sub-threshold swing coefficient, and $V\theta$ is the thermal voltage. Vgs0, Vth0, Vsb0 and Vds0 are the gate-to-source voltage, the zero-bias threshold voltage, the base-to-source voltage and the drain-to-source voltage, respectively,γ is the body-bias effect coefficient, and η is the Drain Induced Barrier Lower-

ing (DIBL) coefficient, μ is zero-bias mobility, C_{ox} is the gate-oxide capacitance, W is the width of the transistor, and L_{eff} is the effective channel length [8]. From equation (1) we see that leakage current (I_{sub0}) decreases as V_{sb0} increases. As a result of Body effect, V_{th} also increases which lowers the performance. During the active mode, the performance is improved as the PMOS (M2) is ON which makes the V_{th} of the pull up PMOS (M1) lower again. The same discussion is applicable for the pull down NMOS (M4) and NMOS (M5). The remaining NMOS (M3) and PMOS (M6) works together for retaining the state in the sleep mode. If the output is high, in the sleep mode, the NMOS (M3) will keep the output high. Similarly, the PMOS (M6) will maintain the state in sleep mode if the output is low.
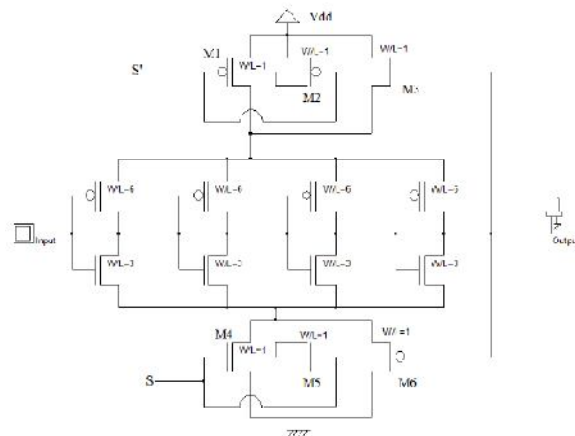

Fig. 6 Variable body Biasing Approach (Chain of 4 inverters)

IV. SIMULATION METHODOLOGY

We compare the variable body biasing technique with four of the previous approaches explained earlier namely; sleep transistor, sleepy stack, dual sleep and dual stack. Thus, we compare five design approaches in terms of power consumption (dynamic and static), delay and area. To show that the variable body biasing approach is applicable to general logic design and memory, we choose a chain of 4 inverters (Fig. 6) and a SRAM cell (Fig. 7). We use HSPICE [8] for simulation purpose to estimate delay and power consumption. Area is estimated with the help of MICROWIND. All considered approaches are evaluated for performance by using a single, low-Vth for all transistors. Dual Vth technology is applied and tested only for the sleep, dual sleep, dual stack and proposed approaches since applying high-Vth. For the dual Vth technique, high-Vth is used for leakage reduction transistors and low-Vth is used for the other transistors. The high-Vth is set to have 0.1V higher Vth than the Vth of a normal transistor (low-Vth).The inverter chain uses four inverters each with W/L=6 for PMOS and W/L=3 for NMOS for the base case.Sleep transistors used in the pull-up and pull-down networks of the base case inverter chain have W/L=6 and W/L=3. The variable body biasing approach transistor size is shown in Fig. 7
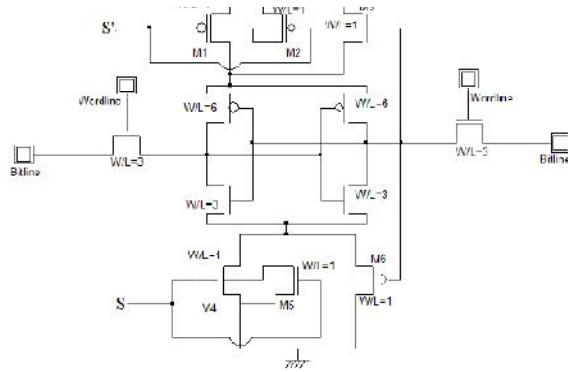
Fig. 7 Variable Body Biasing Approach (SRAM Cell)

The chosen technologies are BSIM4 PTM Model [9] and their supply voltages are given in Table I.

TABLE I
CHOSEN TECHNOLOGY AND VDD VALUE

130nm	90nm	65nm	45nm	32nm
1.2	1.1	1.0	0.9	0.8

V. SIMULATION RESULTS

We measure static power consumption, dynamic power consumption, propagation delay and area for five design approaches, which are sleep, sleepy stack, dual sleep, dual stack and variable body biasing approach. Fig.8 shows the static power consumption, Fig.9 shows the dynamic power consumption, Fig.10 shows the propagation delay comparison and Fig.11 shows area consumed for a chain of four inverters.
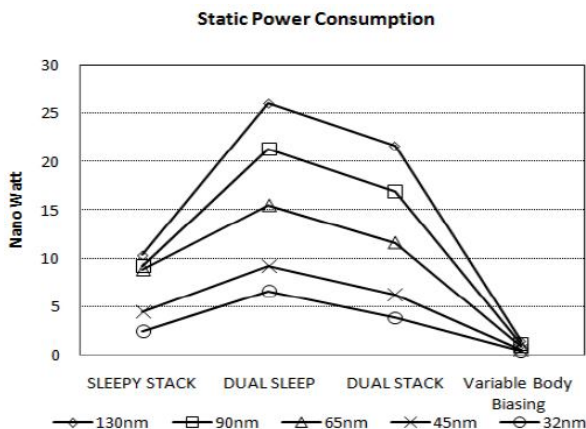

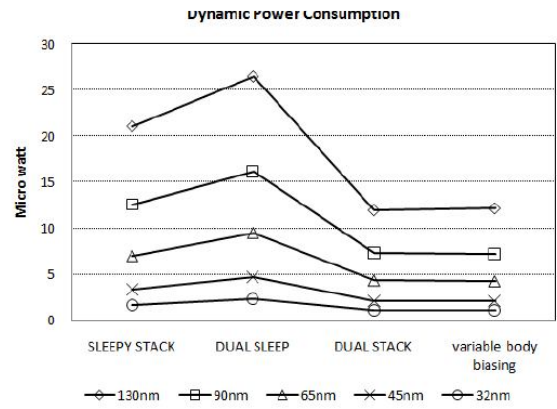Fig. 8 Static Power Comparison (Chain of 4 Inverters)

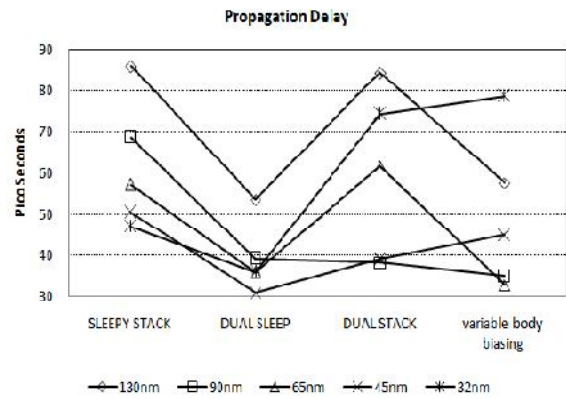Fig. 9 Dynamic Power Comparison (Chain of 4 Inverters)

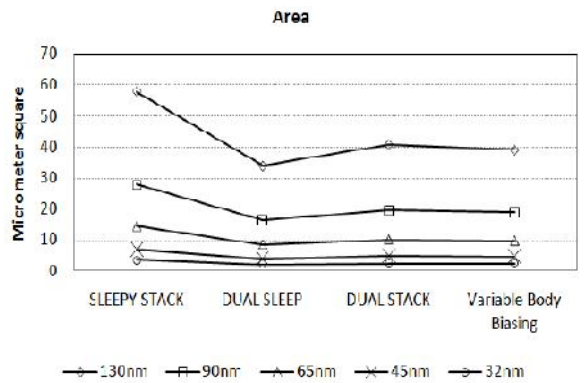Fig. 10 Propagation Delay Comparison (Chain of 4 Inverters)

Fig. 11 Area Comparison (Chain of 4 Inverters)

The static power consumption, dynamic power dissipation, propagation delay and area consumed for a SRAM cell are shown in fig.12, fig.13, fig.14, and fig.15 respectively
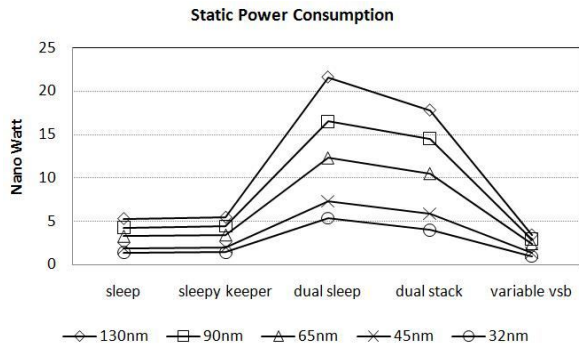
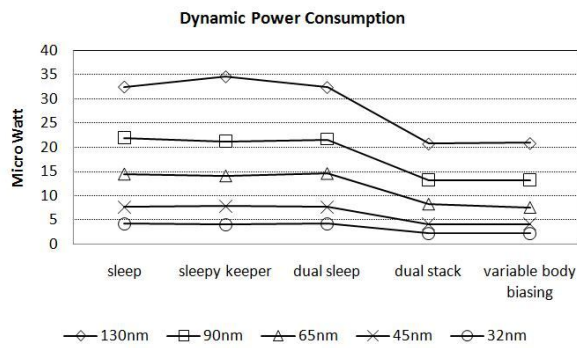Fig. 12 Static Power Comparison (SRAM Cell)

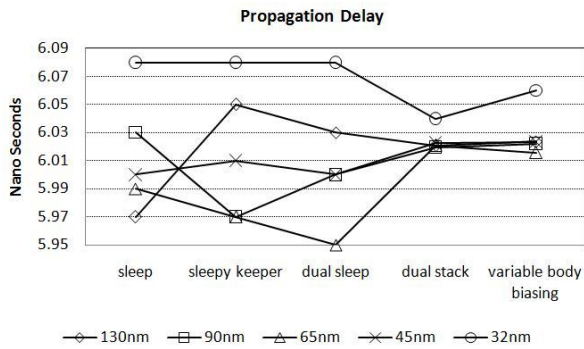Fig.13 Dynamic Power Comparison (SRAM Cell)

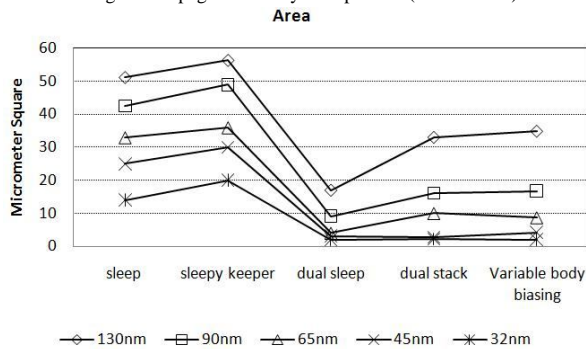Fig. 14 Propagation Delay Comparison (SRAM Cell)

Fig. 15 Area Comparison (SRAM Cell)

The comparisons of Variable body biasing approach using 65 nm technology with the existing methods for a chain of four inverters and for a SRAM cell are summarized in Table II and Table III, respectively. Here '+' denotes improved and '-' denotes degraded performance.

TABLE II
Comparison of V_{BB} Approach for a chain of FOUR Inverter

Methods	Delay	Static Power	Dynamic Power	Area
Dual sleep	+8.73%	+94.7%	+55.4%	-15.61%
Dual stack	+46.76%	+92.39%	+2.9%	+4.9%

TABLE III
Comparison of V_{BB} Approach for a SRAM Cell

Methods	Delay	Static Power	Dynamic Power	Area
Dual Sleep	-1.11%	+80.94%	+47.98%	-74.82%
Dual Stack	+0.08%	+77.41%	+8.62%	+12.68%

Power delay products for a chain of four inverters are 0.34fJ, 0.266fJ and 0.139fJ for dual sleep, dual stack and Variable Body Biasing, respectively. Hence, the Variable Body Biasing approach shows the least power delay product among all.

VI. CONCLUSION

Miniaturization of CMOS technology achieving high performance has resulted in increase of leakage power dissipation. We have presented an efficient methodology for reducing leakage power in VLSI design. Our Variable Body Biasing approach shows improved results in terms of static power, dynamic power and power delay product. It gives the CMOS circuit designers another option in designing integrated circuits more efficiently.

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