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Minimization power and non-linearity errors with split SAR ADC

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ABSTRACT

This paper introduces the linearity analysis of a progressive successive approximation registers (SAR) simple to- advanced converters (ADC) with part DAC structure taking into account two exchanging techniques: conventional charge-redistribution and Vcm-based switching. The static linearity execution, in particular the fundamental nonlinearity and differential nonlinearity, and in addition the parasitic impacts of the part DAC, are dissected hereunder. What's more, a code-randomized adjustment strategy is proposed to minimize the the transformation nonlinearity in the ordinary SAR ADC, which is confirmed by behavioral simulation, and measured results. Exhibitions of both exchanging conventional are shown in 90 nm CMOS. Estimation consequences of power, speed, and linearity plainly demonstrate the profits of utilizing Vcm-based exchanging.

Index Terms—Linearity analysis, linearity calibration, SAR ADCs, split DAC, Vcm-based switching**.**

I. INTRODUCTION:

Successive approximation registers (SAR) analog-to-digital converters (ADCs) [1]–[4], as an alternative to the pipelined ADCs [5] has become popular for battery-powered mobile applications, such as DVB-T, DVB-H and TDMB which require medium speed (10 MS/s–100 MS/s) and medium-resolution (8–10 b). SAR ADCs [2]–[4] achieve very low power consumption due to their simple architecture and operation. However, the SAR conversion relies basically on the performance of a capacitive DAC that subtracts the reference voltage from the input signal. The kT/C noise, capacitor mismatches, and parasitic of the split DAC affect the conversion accuracy. As for medium resolution, the kT/Cnoise requirement is fulfilled with small capacitance, while other non idealities like parasitic and nonlinearity, whose effect depends on the structure and the switching approach of the DAC, becomes significant.

The binary-weighted capacitive DAC is widely used in SAR ADCs. However, the capacitance of the DAC array increases exponentially with the resolution, which imposes larger consumption of switching energy, area, and settling time. A valuable substitute is the split capacitive DAC, which has been recently reconsidered for medium resolution . Its key limitation lies in the parasitic capacitors that destroy the desired binary ratio of the capacitive DAC array, thus degrading the conversion linearity. However, by using the metal-insulator-metal (MIM) capacitor /and DAC mismatch calibrations the split structure can become suitable for a medium-resolution target. On the other hand, the conversion linearity is also directly correlated with the switching sequences of the DAC array, where the conventional charge-redistribution switching results in worse conversion linearity and more energy losses. A *V*cm-based switching technique has been recently proposed, which achieves a significant switching energy saving when compared with set-and-down [3] and charge-recycling switching approaches. This paper analyzes the conversion nonlinearities, induced by supply noise, switching methods, and parasitic effects in SAR ADCs. The static nonlinearities based on the conventional and *V*cm-based switching methods are theoretically analyzed, and the mathematical models are developed to verify the effectiveness of the *V*cm-based approach. Experimental results on a 90 nm CMOS 10 b 65 MS/s SAR ADC with conventional switching and a 10 b 100 MS/s SAR ADC with *V*cm-based switching demonstrate the performance benefits in terms of speed, power, and linearity by using *V*cm-based switching.

In addition, the internal node parasitic in the split DAC is also analyzed, as it degrades the conversion linearity. The above limitation can be fixed by a code-randomized digital calibration technique proposed here to improve the differential nonlinearity (DNL) and integral nonlinearity (INL).

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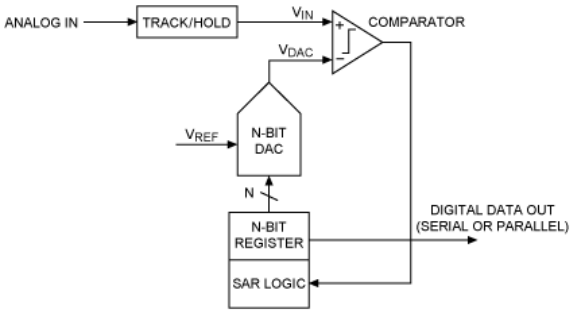

Fig. 1. Block diagram of the ADC architecture.

2. OVERALL ADC ARCHITECTURE

Fig. 1 shows the architecture of the 10 b ADC. It is a conventional SAR ADC consisting of a differential capacitive network a comparator and SA control logic. The SAR logic includes shift registers and switch drivers which control the DAC operation by performing a binary-search algorithm during the conversion cycle. The capacitive DAC array is the basic structure of the SAR ADC, which serves both to sample the input signal and subtract the reference. A reference-buffer-free technique [24] is used to improve the power dissipation and DAC settling..

3. SWITCHING METHODS:

When using the supplies as reference, the switching power is dynamic, which is correlated with the switching sequence Fig. 2(a) shows a conventional single-ended *n*-bit split [*k*-bit most significant bit (MSB) and *i* -bit LSB sub-array] DAC structure and its switching timing diagram. During the global sampling phase, the input signal *V*in is stored in the entire capacitor array. The algorithmic conversion then begins by switching only the MSB capacitor to *V*DD and the others to Gnd. Accordingly, *V*out settles to −*V*in and the comparator output Out_{comp}in the first MSB decision will be

$$out_{\{comp\}} = \begin{cases} 0 & v_{in} > 0 \\ 1 & v_{in} < 0 \end{cases} \quad (1)$$

The comparator output decides the switching logic of the MSB capacitor. If Out_{comp} is low *S*m,k is switched back to Gnd If Out_{comp}is high, then *S*m,k is kept to *V*DD. For either decision, simultaneously, the *S*m,k−1 (the MSB/2) switches to *V*DD for the next bit comparison. The above process will be repeated for $n - 1$ cycles. The conventional charge-redistribution method is not very power effective [25], especially when discharging the MSB
and charging the MSB/2 capacitor is required (bit decision back from "1" to "0") This is unnecessary in general, but it is required for that specific technique to operate properly. However, it would be beneficial if it can be avoided to save switching energy. The *V*cm-based switching method proposed in [24] halves the array capacitance leading to around 90% energy saving when compared with the conventional one. Fig. 2(b) details the *V*cm-based switching algorithm. In the global sampling phase _1, *V*in is stored in the capacitor array. During the conversion phase _2, all the capacitors' bottom-plates are switched to the *V*cm first, to give rise to the voltage −*V*in at the output. The sign of *V*out determines the MSB as the logic properly controls *S*m,k−1. If −*V*in < 0, *S*m,k−1 goes to Gnd while the other switches *S*m,k−2, …, *S*l,0 remain connected to *V*cm. If *V*in > 0, *S*m,k−1 is switched to *V*DD. The cycle will be repeated for $n - 2$ times. The *V*cm-based approach performs the MSB transition by connecting the differential arrays to *V*cm. The power dissipation is just derived from what is needed to drive the bottom-plate parasitic of the capacitive arrays, while in the conventional charge-redistribution where the necessary MSB "up" transition costs significant switching energy and settling time. Moreover, as the MSB capacitor is not required anymore, it can be removed from the *n*-bit DAC array. Therefore, the next $n - 1$ b estimation is done with an $(n - 1)$ bit array instead of its *n*-bit counterpart, leading to half capacitance reduction with respect to the conventional method. Using supplies as reference voltages prevents static power dissipation from reference buffers [3], although the conversion becomes very sensitive to the supply ripple due to the switching effect. For 10-b accuracy the supply variation needs to be suppressed within ±0.049% of the full supply rail, or the supply ripple ±588 μV for a 1.2 V supply. The detailed analysis of conversion sensitivity to supply noise is presented in the Appendix. As the *V*cm-based switching charges 75% less capacitance, simultaneously, when compared with the conventional switching, it can effectively reduce the under-shoot of the supply or reference buffer (when used). The inductive ringing effect can be well suppressed by minimizing the bonding inductance, e.g., multiple bonding, through the addition of a damping resistor and an on-chip decoupling capacitor *C*decp. On the other hand, to overcome this problem an effective approach might be the use of a SA searching algorithm like non binary conversion that relaxes the settling accuracy requirement during large switch transients.

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3. LINEARITY ANALYSIS:

3.1 Effect of Switching Schemes on the Linearity:

To analyze the conversion linearity of the conventional and the *V*cm-based switching methods in a binary-weighted DAC (shown in Fig. 3) each of the capacitors is modeled as the sum of the nominal capacitance value and the error term

$$c_n = 2^{n-1}c + \delta_n \quad (1)$$

considering that all the errors are in the unit capacitors, whose values are independent-identically distributed Gaussian random variables, and have a variance of

$$E[\delta_n^2] = 2^{n-1}\sigma^2 \quad (2)$$

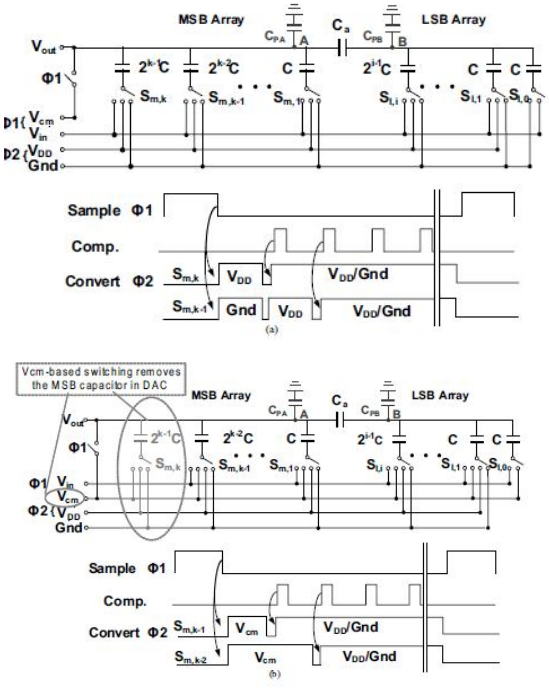

Fig. 2. Single-ended *n*-bit and (*n* − 1)-bit split capacitive DAC arrays with their switching timing diagrams (*n* = *k* + *i*). (a) Conventional switching. (b) *V*cm-based switching.

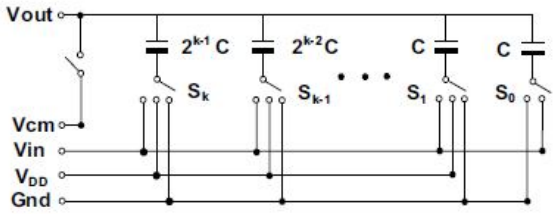

Fig. 3. *k*-bit binary-weighted DAC.

and where σ is the standard deviation of the unit capacitor. The *V*cm-based method achieves half capacitance reduction when compared with the conventional one, while the switching linearity comparison between the two switching methods should be addressed in the same capacitive DAC, with the same value of capacitor mismatch as well as predictable gain errors caused by unbalanced array capacitance. Accordingly, to perform the *V*cm-based switching method in the *k*-bit DAC array of Fig. 3, both *S*0 and *S*1 are kept connected to *V*cm during bits cycling. To calculate a given digital input *X* with its corresponding DAC output *V*out (*X*), the array is considered initially discharged (*V*in = 0). The analog output of the *k*-bit capacitive DAC with conventional switching can be calculated as

$$v_{out}(X) = \frac{\sum_{n=1}^{k}(2^{n-1}c+\delta_n)s_n+(c+\delta_0)s_0}{2^k c+\sum_{n=0}^{k}\delta_n}\, v_{DD} \quad (4)$$

where the DAC digital input *X* = [*Sn*…*S*0], with *Sn* equal to 1, 1/2 or 0 represents the DAC connecting *V*DD, 1/2 *V*DD (i.e., *V*cm) or Gnd for bit *n*. For a single channel SAR ADC, the comparator offset and linear gain error in the DAC are acceptable, thus closed form calculations of INL and DNL are specified with respect to a bestfit line. In the SAR conversion, the comparator offset appears as an offset error and does not cause nonlinearity, therefore, excluding the offset term, the

$$\mathrm{INL} = \frac{V_{\mathrm{out}}(X)/A - V_{\mathrm{idl}}(X)}{\mathrm{LSB}} \quad (5)$$

$$\mathrm{DNL} = \frac{[V_{\mathrm{out}}(X) - V_{\mathrm{out}}(X-1)]/A - \mathrm{LSB}}{\mathrm{LSB}} \quad (6)$$

$$A = \frac{\sum_{X=0}^{2^n-1} V_{\mathrm{out}}(X)\cdot V_{\mathrm{idl}}(X)}{\sum_{X=0}^{2^n-1} V_{\mathrm{idl}}^2(X)} \quad (7)$$

where *A* indicates the linear gain error of the DAC, *V*idl*(X)* is the nominal value for the digital input *X* and LSB = 1/2*k*VDD. From (7), it can be deduced that the linear gain error *A* is input *X* dependent, which implies that the gain error *A*con for

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conventional switching and *A*CM for *V*cm-based one are not equivalent. However, *A*con and *A*CM values are quite close as 1000-time Monte Carlo simulations running in a 10-b DAC, where unit capacitors are Gaussian random variables with standard deviation of $\sigma(\_C/C$ = 1%), lead to variances of gain δAcon = ± 41e−5 and δACM = ± 4.2e−5. Hence, to simplify the analysis, it will be assumed that the prospective linear gain *A* and the δ terms in the denominator of (4) will be neglected.

The INLs of the two switching methods represent the conversion error that combines together all the errors in each bit. Considering that in *V*cm-based switching, the transitions are *V*cm related (with capacitors connected to *V*cm*)*, it follows that the INLs of the two switching methods must be different. First, the worst INL in conventional switching happens at the MSB transition [23], where only the MSB is pre-charged to *V*DD, leaving other capacitors to Gnd. For the *V*cm-based switching MSB transition is performed by level shifting all capacitors to *V*cm, which is input independent and ideally always achieves an INL of 0 LSB in the middle. The worst INL of *V*cm-based switching happens at the step below the MSB transition, where the input digital code is *X* = [10…0]. The corresponding input digital code of conventional switching is *X* = [10…1] The DAC output*Vout(X)* and INL of the conventional method INLcon are calculated ·

$$v_{out}(x) = \frac{2^{k-1}c+\delta_k+c+\delta_1}{2^k c}\, v_{DD} \quad (8)$$

$$INL_{con} = \frac{\delta_k+\delta_1}{2^k c} \cdot \frac{v_{DD}}{lSB} \quad (9)$$

With variance

$$E[\delta^2_{INLcon}] = \frac{(2^{k-1}+1)\sigma^2}{c^2} \quad (10)$$

The INL of the *V*cm-based method INLCM and its variance *E*[δ2 INLCM] can be similarly derived as follows:

$$INL_{CM} = \frac{\delta_k}{2^k C} \cdot \frac{v_{DD}}{LSB} = \frac{\delta_k}{C} \quad (11)$$

$$E[\delta^2_{INLCM}] = \frac{2^{k-1}\sigma^2}{C^2} \quad (12)$$

Comparing the results of (10) and (12) it proves that the conventional and *V*cm-based switching have similar INLs at the step below MSB transition. In reality, *V*cm-based switching is insensitive to the input common mode noise. The maximum DNL for the conventional method is expected to occur at the step below the MSB transition. With *X* = [10…0] and (*X* − 1) = [01…1], the difference between the voltage errors can be calculated .

$$V(X) - V(X-1) = \frac{C + \delta_k - \sum_{n=1}^{k=1}\delta_k}{2^k C}$$

$$.V_{DD} = LSB + \frac{\delta_k - \sum_{n=1}^{k=1}\delta_k}{C}.\text{LSB} \quad (13)$$

thus, its DNL yields

$$DNL_{con} = \frac{\delta_k - \sum_{n=1}^{k-1}\delta_n}{C} \quad (14)$$

and with its variance

$$E[\delta^2_{DNLcon}] = \frac{(2^k-1)\sigma^2}{C^2} \quad (15)$$

In the *V*cm-based switching the MSB “up” transition is replaced by an initial reset of all the capacitors to *V*cm (with the middle digital input *X* equal to [1/2…1/2]). There exist two consecutive worst DNLs occurring at the steps above (*X* + 1) = [0, 1…1] and below (*X* − 1) = [1, 0…0] the MSB transition. One of the worst DNLCM with two digital inputs *X* = [1/2…1/2] and (*X* − 1) = [0, 1…1] is obtained similarly as *V (X)* − *V (X* − 1) = LSB + ½ _ kn=0 δn − _ k−1 n=0 δn C · LSB (16) DNLCM = 1/2δk ½ _ *k*−1 *n*=0 δn *C* (17) with variance *E*[δ2 DNLCM] = 2*k*σ2 4*C*2 . (18) Equations (15) and (18) show that the proposed method can achieve a DNL that is two times better in comparison to conventional switching. It can also be found that the error terms are decreased by half, which can be attributed to the cancellation of the terms _ *k*−1 *n*=0 δn in (16). In fact, this happens because the capacitors contributing to two-bit transitions are correlated, which are switched from *V*cm to *V*DD. In contrast, in the conventional method the capacitors connected to *V*DD in two-bit transitions are completely different, and the error terms in (13) are summed together instead of being cancelled.

4. DNL AND INL CALIBRATION TECHNIQUE:

In practice, the conversion nonlinearity gets worse when the conventional switching is used. Since there is a large switching transient in its “down” transition, caused by

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switching two capacitors simultaneously, the large switching transient causes the excessive supply voltage undershoot as well as potentially exacerbates an overdrive condition of the preamplifier, which will finally result in a wrong decision on the comparator's output. In contrast, *V*cm-based switching prevents occurrence of such large switching transient. In every bit cycle, only one capacitor is switched to obtain a voltage value by successive approximation of the input voltage without wasting energy and settling time. Moreover, the mismatches of the attenuation capacitor, as well as, the routing parasitic capacitance in the internal node of the DAC, cause conversion nonlinearity.

*D*r has discrete uniform distribution (DUD), which implies the probability (*P)* of any outcome *D*r from three possible values *Dn* − 1, *Dn*, *Dn* + 1 is 1/3. it can be seen that the nonlinearity is a static conversion error, which happens periodically corresponding to the number of bits distributed in the LSB array.

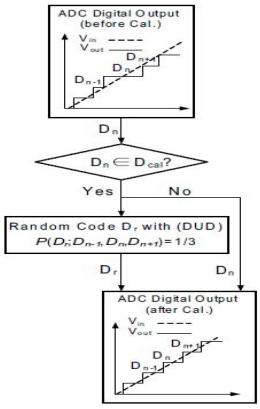

Fig. 4. Code-randomized calibration algorithm.

Therefore, the foreseeable static linearity errors can be potentially calibrated in the digital domain. Ideally all the quantization levels of the *n*-bit ADC are uniformly spaced, but due to non ideal elements in the actual circuit implementation the code transition points in the transfer function will be moved shown in Fig. 4. To calibrate the linearity error, a code-randomized calibration is proposed, which provides a plausible digital post-processing to fix the large quantization errors. This is achieved by redistributing the steps with statistically equally over the step's ± LSB range. The calibration algorithm is shown in Fig. 6. The digital outputs used to find the DNL and INL errors are compensated values, where the comparator offset and linear gain errors will not appear. First the calibration will determine whether the ADCs digital output needs to be corrected. For an *n*-bit ADC with the split DAC shown in Fig. 2(a) there are *m* (*m* = 2*n*/2*i* − 1) digital codes (*D*cal = [*D*1, *D*2, …, *D*m]) where large quantization steps happen and they are subject to be calibrated. When the ADCs digital output *D*n matches any of the digital code in *D*cal, the random number generator will outcome a new digital output *D*r . The randomized output *D*r has one of the three possible values *D*n and its two adjacent quantization levels *Dn* − 1 and *Dn* + 1, which are equally spaced with an identical probability of 1/3. The randomized solution transfers the nonlinearity into increased average quantization noise power. Therefore, the large DNL and INL errors can be calibrated with signal-to-noise distortion ratio (SNDR) of the ADC dropping slightly. Verified by a behavior simulation of a 10 b level, the SNDR with and without code-randomized calibration is 56.2 and 55.6 dB, respectively (32 768 samples are taken in a 10-b SAR ADC with 10% top-plate parasitic *C*PB, while ADC is otherwise ideal). The code-randomization calibration is used to calibrate the DNL errors shown in Fig. 5(a). For example, when the output digital code *D*31 is detected, the system will auto-generate a new digital output selected from the codes *D*30, *D*31, and *D*32. The code-randomization calibration is used to calibrate the DNL errors shown in Fig. 5(a). For example, when the output digital code D_{31} is detected, the system will auto-generate a new digital output selected from the codes D_{30}, D_{31}, and D_{32}.

5 .RESULTS:

The flowing figure shows the simulation results for the conventional SAR ADC with binary weighted capacitor DAC compared with split SAR ADC

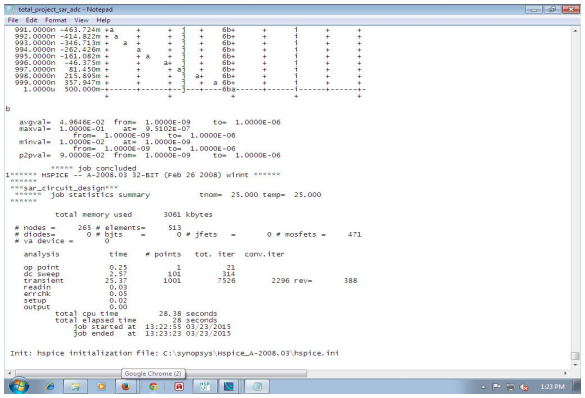

Fig.5 :power consumption for conventional binary weighted capacitors DAC.

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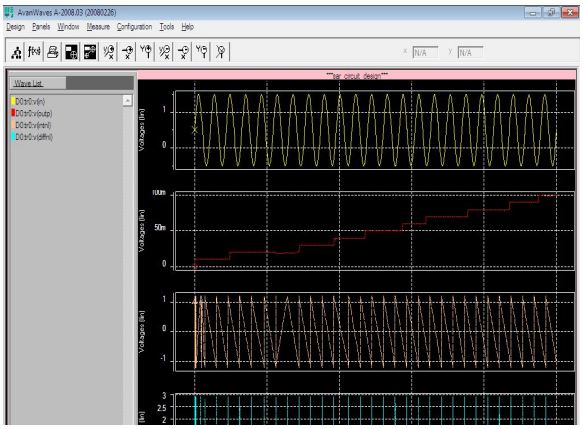

Fig .6 : Input, stair case output,INL &DNL for the SAR ADC with binary weighted capacitive DAC.

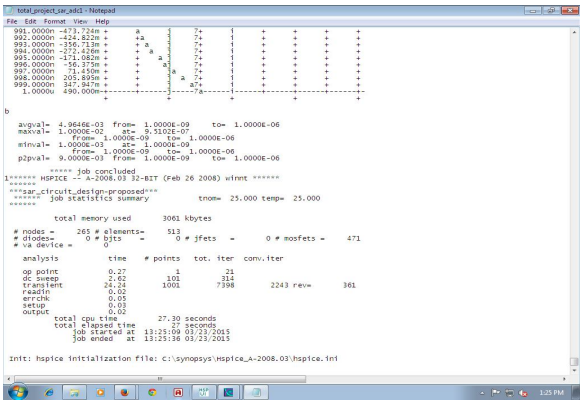

Fig.7: power consumption for proposed split SAR ADC.

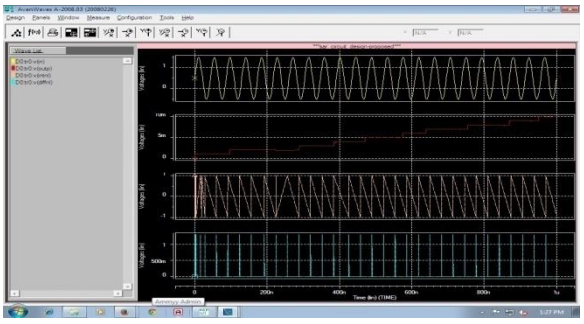

Fig.8 : Input, stair case output ,INL &DNL for the split SAR ADC

6. CONCLUSION:

Two 1.2 V 10-b SAR ADCs working at many MS/s with ordinary and Vcm-based exchanging were exhibited. The linearity practices of the DACs exchanging and structure were dissected and checked by both recreated and measured results. The Vcm-based exchanging procedure gives predominant transformation linearity when contrasted and the traditional technique as a result of its exhibit's capacitors relationship amid every bit cycling. The proposed code-randomized adjustment can dispose of the expansive DNL and INL lapses in the ordinary exchanging. Measured results exhibited that both higher speed and lower force is attained to by utilizing Vcm-based exchanging. DAC for traditional and Vcm-based exchanging.

7. FUTURE SCOPE:

Calibration technique here used is code randomized calibration technique which is good for calibrating a capacitance mismatch which is optimal here but not very accurate. As mismatch here is calibrated before chip operated on any bit but in actual every bit has different capacitance mismatch which can be calculated while DAC is operated on a particular bit and then adding mismatch value corresponding to that bit at the end of operation. With this calibrating circuitry design becomes little complex as memory would be required to store each bit mismatch and hence will increase the power consumption. But the overall accuracy of DAC will be improved to a large extent.

One of the main advantages of this type of conversion technique is its power efficiency and an investigation into the practicality of using such an ADC for a hand held mobile device implementation would be useful in future. However this is not the limit of this type of ADCs performance capabilities. Higher speeds and higher resolutions can be obtained through future research.

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