ISSN 2347 - 3983

International Journal of Emerging Trends in Engineering Research (IJETER), Vol. 3 No.6, Pages : 195- 199 (2015)
Special Issue of NCTET 2K15 - Held on June 13, 2015 in SV College of Engineering, Tirupati
http://warse.org/IJETER/static/pdf/Issue/NCTET2015sp38.pdf

IMPLEMENTATION OF FM0 AND MANCHESTER ENCODING FOR DSRC APPLICATIONS IN VLSI

G.Thriveni[1], D.Jyothi[2]

[1]M.Tech(VLSI D), Department of ECE, SV College of Engineering, Tirupati, India, thri91091@gmail.com

[2]Assistant Professor, Department of ECE, SV College of Engineering, Tirupati, India, jyothidevineni.vlsi@gmail.com

***Abstract*—The dedicated short-range communication is a one- or two-way medium range communication that can be divided into two categories: automobile-to-automobile and automobile-to-roadside. The safety issue consists of blind-spot, forewarning about accident of vehicles, intercars distance, and buzzer or warning alarm before collision. The automobile-to-roadside mainly focuses on the intelligent transportation service i.e, electronic toll collection (ETC) system. In automobile-to-automobile, the DSRC technique is used for message transfer and broadcasting among automobiles for security issues. The DSRC ideology generally requires FM0 and Manchester encodings to maintain the zero mean value. But the coding assortment between the two programming technique critically confines the latent to design a fully reused architecture in Very Large Scale Integration. Hence similarity oriented logic simplification technique is proposed. This practice improves the hardware utilization rate.**

Keywords: Dedicated short range communication,ETC

(Electronic Toll Collection)

I. INTRODUCTION

The DSRC values have been recognized by several organizations in various countries. These DSRC values of America, Europe, and Japan are shown in table 1. The data rate alone targets at 500 kb/s, 4 Mb/s, and 27 Mb/s with carrier frequency of 5.8 and 5.9 GHz.The modulation methods incorporate ASK,PSK and OFDM.

TABLE I

	Europe	**America**	**Japan**
Organization	CEN[1]	ASTM[2]	ARIB[3]
Data rate	500 kbps	27 mbps	4 mbps
Carrier Frequency	5.8 Ghz	5.9 Ghz	5.8 Ghz
Modulation	ASK,PSK	OFDM	ASK
Encoding	FM0	Manchester	Manchester

Normally, the waveform of transmitted signal is predictable to have zero mean for toughness issue, and this is also called as dc-balance. The transmitted signal consists of arbitrary binary sequence, which is hard to get dc-balance.The Manchester and FM0 codes are used to provide the zero mean value of the transmitted signal. These two codes are mostly used for encoding. This theory also proposes a Manchester encoding architecture for ultrahigh frequency (UHF) RFID tag emulator. This hardware architecture is possible from the finite state machine (FSM) of Manchester code, and is realized into FPGA prototyping system. However, the coding-diversity between both seriously limits the potential to design a VLSI architecture that can be fully reused with each other. The VLSI architectures of FM0 and Manchester encoders are given as follows. This architechture needs CMOS inverter and the gated inverter as the switch to develop Manchester encoder. It is implemented by 0.35-μm CMOS technology and its frequency of operation is 1 GHz. This literature further replaces the architecture of switch in by the NMOS device. It is realized in 90-nm CMOS technology, and the maximum operation frequency is as high as 5 GHz. The theory develops a high-speed VLSI architecture almost fully reused with Manchester and Miller encodings for radio frequency identification (RFID) applications. In this VLSI architecture design using similarity-oriented logic simplification (SOLS) technique is proposed. The SOLS consists of two core methods: area-compact retiming and balance logic-operation sharing. The area-compact retiming relocates the hardware resource to reduce 22 transistors. The balance logic-operation sharing efficiently combines FM0 and Manchester encodings with the fully reused hardware architecture. With SOLS technique, this paper constructs a fully reused VLSI architecture of Manchester and FM0 encodings for DSRC applications.

ISSN 2347 - 3983

International Journal of Emerging Trends in Engineering Research (IJETER), Vol. 3 No.6, Pages : 195- 199 (2015)
Special Issue of NCTET 2K15 - Held on June 13, 2015 in SV College of Engineering, Tirupati
http://warse.org/IJETER/static/pdf/Issue/NCTET2015sp38.pdf

II. FM0 CODE AND MANCHESTER CODE

In the next conversation, the clock signal and the input data are abbreviated as CLK, and X. With these parameters, the coding principles of FM0 and Manchester codes are discussed as follows.

A. FM0 Encoding

As shown in Fig. 1, for each X, the FM0 code consists of two parts: one for former-half cycle of CLK, A, and later-half cycle of CLK, B.

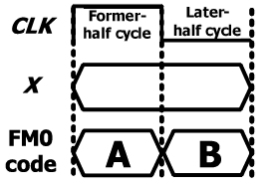


Fig. 1. Codeword structure of FM0

The coding rule of FM0 is given below
1) If X is the logic-0, the FM0 code must exhibit a transition between A and B.
2) If X is the logic-1, no transition is allowed between A and B.
3) The transition is allocated among each FM0 code no matter what the X is.
A FM0 coding example is shown in Fig.2. At cycle 1, the X is logic-0; therefore, a change occurs on its FM0 code, according to rule 1. For ease, this change is firstly set from logic-0 to -1. According to rule 3, a shift is owed among each FM0 code, and thereby the logic-1 is changed to logic-0 in the start of cycle 2. According to rule 2, this logic-level is seize without any change in entire cycle 2 for the X of logic-1.

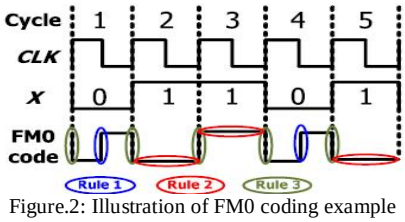


Figure.2: Illustration of FM0 coding example

B. Manchester Encoding

The Manchester coding model is realized with XOR operation of CLK and X.

$$X \oplus \text{CLK}.$$

The clock always has a transition within one cycle, and so does the Manchester code no matter what the X is.

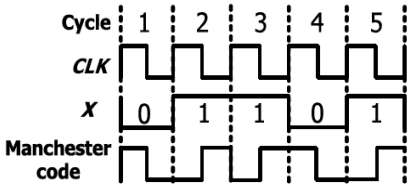


Fig. 3. Manchester coding example.

III BASIC CONCEPTS OF VERILOG

Verilog HDL has been successfully applied in all the major accomplishments in the field of digital design in the last decade. It is a language that is today IEEE standard 1364, is open and has activities under Open Verilog International umbrella, has annual International Verilog Conference (IVC) and is used in a vast majority of electronics and computer industry projects as well as research in academics in areas such as formal verification and behavioral synthesis. It also has spawned an industry of CAD tool vendors and consulting/support experts creating a movement to participate in the world of electronics today.
Traditionally a counter is designed with flip-flops and gates. The flip-flops in turn are designed with gates. To test the counter we connect clock and reset signals. Verilog retains the capability of describing structural level descriptions, as shown below, and adds the register transfer level and the behavioral capabilities over traditional methods of design. These abstraction capabilities can be seen in the following models and in comparing the traditional methods versus the Verilog approach.

The following example describes the gate-level description of a D edge-triggered flip-flop.

```
module d_edge_ff_gates(q, qBar, preset, clear, clock,
d);
inout q, qBar;
input clock, d, preset, clear;
nand #1 nl (ol, preset, o4, o2),
n2 (o2, clear, clock, ol),
n3 (o3, clock, o2, o4),
n4 (o4, d, o3, clear),
n5 (q, preset, o2, qBar),
n6 (qBar, q, o3, clear);
endmodule
```

Verilog defines a set of words to have special meaning. These words are reserved and cannot be used as identifiers or labels in a Verilog model. The type of a statement is identified by the first word in

ISSN 2347 - 3983

International Journal of Emerging Trends in Engineering Research (IJETER), Vol. 3 No.6, Pages : 195- 199 (2015)
Special Issue of NCTET 2K15 - Held on June 13, 2015 in SV College of Engineering, Tirupati
http://warse.org/IJETER/static/pdf/Issue/NCTET2015sp38.pdf

the statement that is a keyword. Examples of these will be 'always', 'and', 'assign', etc. When a statement begins with the word always, there is a special meaning of an always loop attached to that statement.

The behavioral model always uses blocks with procedural statements, while the RTL model uses continuous assignments that begin with keyword 'assign'.

Syntax
source_text
::= {description}
description
::= module_declaration
| UDP_declaration
module_declaration
::=module_keyword module_identifier
[list_of_ports];
{module_item}
endmodule
module_Keyword
::= module | macromodule
{module_item}
endmodule
module_item
::=data_declaration
||= functional_descriptions
||= module_timing_descriptions
functional descriptions
::= behavioral_descriptions
||= RTL_descriptions
||= structural_descriptions

Operators in Expressions

Operators identify the operation to be performed on their operands to produce a new value. Most operators are either unary operators that apply to only one operand, or binary operators that apply to two operands. Two exceptions are conditional operators, which take three operands, and concatenation operators, which take any number of operands. Verilog provides a rich set of operators as described in the next few pages.

The main operators under various categories are:
Unary Operators: + - ! ~ & ~& | ^| ^ ~^
Relational Operators : < > <=> = =
Arithmetic Operators : + - */ %
Logical Operators : ! && II != == === !==
Boolean Operators: & | ~ ^ ^~
Shift Operators : >> <<
Concatenation: { }
If Operator : ? :

The names for the operators individually are given below.

Operator Description
{ } concatenation
+ add
subtract
* multiply
/ divide
% modulus
> greater than
>= greater than or equal to
< less than
<= less than or equal to
= equal to
!= not equal to
! logical NOT
&& logical AND
| | logical OR
== logical equality
!= logical inequality
bit-wise NOT
& bit-wise AND
| bit-wise OR
^ bit-wise XOR
^~ ~^ bit-wise XNOR
& reduction AND
| reduction OR
~& reduction NAND
~| reduction NOR
^ reduction XOR
~^ reduction XNOR
« Left shift
» right shift
? : Conditional or if operator

The tables for the binary operators are given

3.Existing method

This design adopts the CMOS inverter and the Manchester encoder can be build by the gated inverter which is a switch. The text further replaces the architecture of switch in by the NMOS device. It is implement by 0.35-μm CMOS technology and its frequency of operation is 1 GHz. It is realized in 90-nm CMOS technology, and the utmost frequency of operation is as high as 5 GHz. This design is realize in 0.35-μm CMOS technology and the maximum operation frequency is 200 MHz. The text develops a high-speed VLSI planning almost fully reused with Manchester and Miller encodings for radio frequency identification (RFID) applications. The literature also proposes a Manchester encoding architecture for ultrahigh frequency (UHF) RFID tag emulator. The maximum operation frequency of this design is about 256 MHz The similar design methodology is further applied to individually construct FM0 and Miller encoders also for UHF RFID Tag emulator. This hardware architecture is conducted from the finite state machine (FSM) of Manchester code, and is realized into field-programmable gate array (FPGA)

ISSN 2347 - 3983

International Journal of Emerging Trends in Engineering Research (IJETER), Vol. 3 No.6, Pages : 195- 199 (2015)
Special Issue of NCTET 2K15 - Held on June 13, 2015 in SV College of Engineering, Tirupati
http://warse.org/IJETER/static/pdf/Issue/NCTET2015sp38.pdf

prototyping system. Its utmost operation frequency is about 192 MHz In addition, combines frequency shift keying (FSK) modulation and demodulation with Manchester codec in hardware realization.

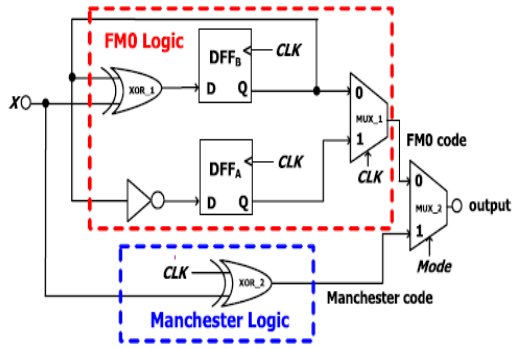


Figure.4 : FM0 and Manchester coding Hardware architecture

IV PROPOSED METHOD

The purpose of SOLS technique is to design a fully reused VLSI architecture for FM0 and Manchester encodings. There are two sub techniques involved in SOLS technique.One is area-compact retiming and the other one is balance logic-operation sharing.

A. Area-Compact Retiming

For FM0, the state value of each state is stored into DFFA and DFFB. The FM0 encoding needs a single 1-bit flip-flop to store the B(t−1). The FM0 coding in Fig. 4 is minimally shown in Fig. 5(a). The logic for A(t) and for B(t) are the Boolean functions to get A(t) and B(t), where the X is omitted for a succinct illustration. If the DFFA is directly removed, there is a option for non synchronization between A(t) and B(t) that causes the logic error of FM0 code.

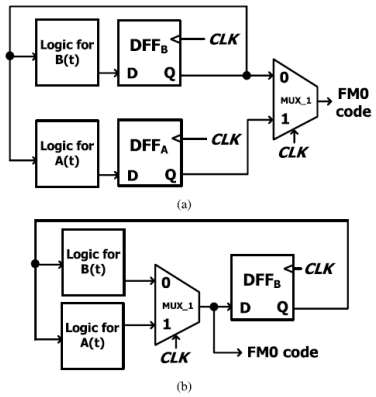


Figure.5: (a) Without area-compact retiming of FM0 encoding. (b) With area-compact retiming of FM0 encoding.

In Fig. 5(a), the Q of DFFB is directly updated from the logic of B(t) with 1-cycle latency. In Fig. 5(b), when the CLK is logic-0, the B(t) is passed through MUX−1 to the D of DFFB. Then, the upcoming positive-edge of CLK updates it to the Q of DFFB.

In order to avoid this logic-fault, the DFFB is relocated right after the MUX−1, as shown in Fig. 5(b),DFFB is assumed to be positive-edge triggered. At each cycle, the FM0 code is derived from the logic of A(t) and the logic of B(t). The FM0 code is switched between A(t) and B(t) through the MUX−1 by the control signal of the CLK. B.

4.2.Balance Logic-Operation Sharing

The Manchester encoding can be derived from X ⊕ CLK.

$$X \oplus \text{CLK} = X\,\overline{\text{CLK}} + \overline{X}\,\text{CLK}.$$

The FM0 and Manchester logics have a common point of the multiplexer like logic with the selection of CLK. As shown in Fig. 6(b), the concept of balance logic-operation sharing is to combine the X into A(t) and X into B(t), This balance logic operation sharing can be realized by using the multiplexer, as shown in Fig. 6(a). It is similar to the Boolean function of FM0 encoding.

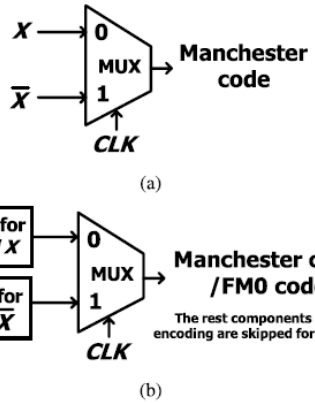


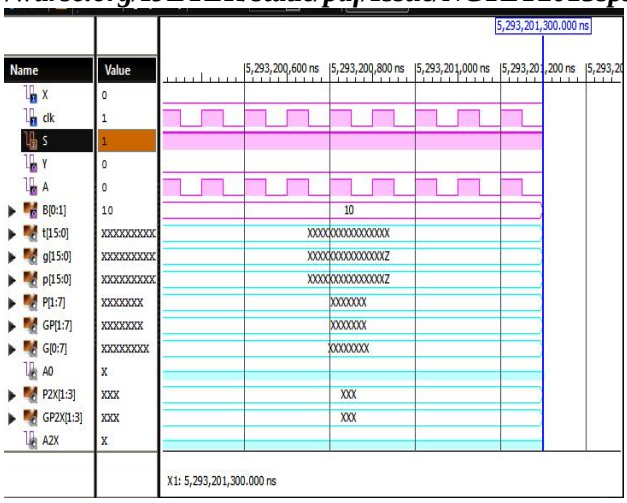
Figure.6: (a) Manchester encoding in multiplexer. (b) Combines the logic operations of Manchester and FM0 encodings.

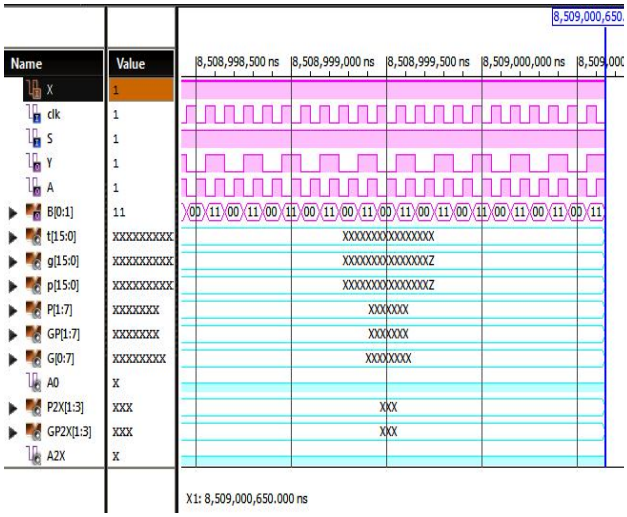
V SIMULATION RESULTS

The following figures show the simulation results. Here X, CLK, S are inputs Y, A are outputs. B represents the state value of Moore state machine and the remaining signals are internal signals.

ISSN 2347 - 3983

International Journal of Emerging Trends in Engineering Research (IJETER), Vol. 3 No.6, Pages : 195- 199 (2015)
Special Issue of NCTET 2K15 - Held on June 13, 2015 in SV College of Engineering, Tirupati
http://warse.org/IJETER/static/pdf/Issue/NCTET2015sp38.pdf





VI Conclusion

A control study on hardware utilization of FM0 and Manchester encodings is discussed in detail. In this, implementation of correspondence oriented logic generality method for dsrc applications is proposed. The coding assortment between two coding techniques causes the limitation on hardware consumption of VLSI architecture design. The SOLS practice eliminates the limitation on hardware utilization.

References

I. I.-M. Liu, T.-H. Liu, H. Zhou, and A. Aziz, "Simultaneous PTL buffer insertion and sizing for minimizing Elmore delay," in Proc. Int.Workshop Logic Synth., May 1998, pp. 162–168.

II. M. A. Khan, M. Sharma, and P. R. Brahmanandha, "FSM based FM0 and Miller encoder for UHF RFID tag emulator," in Proc. IEEE Adv. Comput. Conf., Mar. 2009, pp. 1317–1322.

III. J.-H. Deng, F.-C. Hsiao, and Y.-H. Lin, "Top down design of joint MODEM and CODEC detection schemes for DSRC coded-FSK systems over high mobility fading channels," in Proc. Adv. Commun. Technol. Jan. 2013, pp. 98–103.

IV. N. H. E. Weste and K. Eshraghian, Principles of CMOS VLSI Design: A Systems Perspective, 2nd ed., Upper Saddle River, NJ, USA: Pearson Educ. Ltd., 1993, pp. 98–103.

V. H. Zhou and A. Aziz, "Buffer minimization in pass transistor logic," IEEE Trans. Comput. Aided Des. Integr. Circuits Syst., vol. 20, no. 5, pp. 693–697, May 2001.