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Behavior of Self Timed Null Convention Logic Circuits with Threshold Variations

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ABSTRACT

Due to increasing overheads, it is more and more difficult for the clocked architectures to fulfill design challenges like high performance, complexity, ease of design reuse. To overcome these clocked issues, clock-less asynchronous design paradigms such as the NULL Convention Logic (NCL) is used. NCL is sine qua non in future semiconductor paradigms to face new design challenges. Several researches have proved that NCL has significant improvements such as power reduction and more robust to noise when compared to clocked architectures.

In this paper, we incorporate power reduction technique, Multi-Threshold CMOS (MTCMOS) to delay-insensitive self-timed NCL so called Multi-Threshold NULL Convention Logic (MTNCL) that can significantly reduce leakage power and improve performance. Quantitative analysis has been performed and compared with static CMOS, MTCMOS and NCL on Tanner EDA tools. Results show that the proposed MTNCL technique significantly reduces power when compared to all the other static designs.

Key words: CMOS, Sub-Threshold Leakage, MTCMOS, NCL, MTNCL, Threshold gates, DI.

I. INTRODUCTION

In the past, design challenges are less concerned due to scaling of semiconductor devices into deep submicron regions have now become more and more significant. Previously, in CMOS digital paradigms, dynamic and switching power has been the prime factor for power dissipation and now with the significant reduction in supply and threshold voltages, a drastic increase in leakage power demands new design techniques for integrating semiconductor devices. The main constituent of leakage power is sub-threshold leakage, caused by the current flowing through a cell (transistor) even if it is apparently turned off and rises exponentially with reducing feature size [1].

In deep submicron technology, several techniques have been proposed to reduce or control sub-threshold leakage power. Multi-Threshold CMOS (MTCMOS) is one of the very promising technique that significantly reduces leakage power by adhering high performance in active mode and separating the power supply during standby mode from the circuit. MTCMOS exploits with two or more different threshold voltage (V_t) transistors in a circuit. A Low-Vt cell offers high-speed operation but have more leakage current, whereas high-V_t cells have low-speed but less leakage. MTCMOS amalgamates these two types of transistors by exploiting low-V_t transistors for switching activity to achieve high performance and high-V_t transistors to gate the supply voltage to reduce leakage power significantly [1, 2, 11, 14, 15].

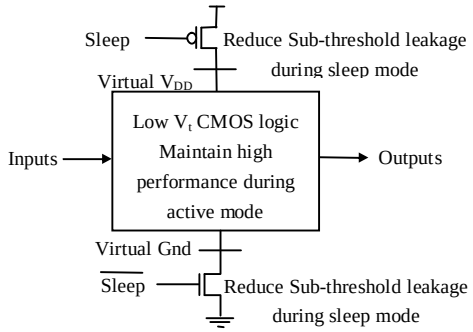

Figure 1: MTCMOS architecture

Delay-insensitive self-timed NULL Convention Logic (NCL) [1, 3, 4] paradigms designed using conventional CMOS logic exhibit an innate idle characteristics since they only switch when necessary work is being done; however, there exist a significant leakage during idle mode. Multi-Threshold NULL Convention Logic (MTNCL) incorporates the MTCMOS technique with NCL during idle mode to sleep the NCL circuit, in lieu of the NULL wave-front, to yield a high-speed ultra-low power asynchronous design methodology that necessitate less area than the conventional NCL paradigm.

In this paper, we propose a novel asynchronous MTNCL to reduce leakage power. Compared to conventional NCL the proposed MTNCL reduces leakage significantly, provides faster operation and has no area overhead. Section II provides an overview of previous work on NCL. Section III discusses the proposed MTNCL. Section IV compares MTNCL with CMOS, MTCMOS and NCL implementations and Section V provides conclusions.

II. PREVIOUS WORK

2.1. Dual-Rail Encoding

NULL convention logic makes use of multi-rail signals, such as dual-rail structures, as it is the simplest scheme with three valid states NULL, DATA0, DATA1,

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Table I: Dual-Rail Encoding

State	Rail0	Rail1
NULL	0	0
DATA0	0	1
DATA1	1	0
Illegal	1	1

where the DATA corresponds to Boolean values 0 and 1while NULL corresponds to empty value as shown in table1 and the fourth is the illegal state where the wires are mutually exclusive, such that both wires can never be asserted simultaneously. Instead of clock, the control is given by NULL to the circuits [1, 4, 10, 12].

2.2. NCL logic gates

NCL exploits 27 threshold logic gates [3-9] with four or lesser inputs and holds state information due to hysteresis property. The primary logic cell of NCL is the threshold gate. THmn is the basic threshold gate, where 1≤m≤n, have n inputs and m is the threshold where at least m inputs must be asserted before the output is asserted.

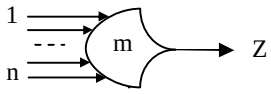


Figure 2: THmn logic gate

Whilst THmnWw1..wR is the second type of basic threshold gate with weight wR, where m≥wR>1 given to input R, where 1≤R<n and the input weights w1.... wR, each > 1.

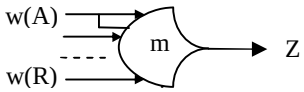
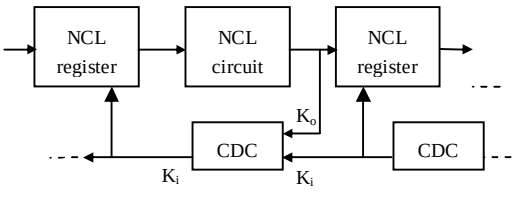


Figure 3: THmnWw1..wR gate

2.3. NCL frame work

NCL circuits exploit NULL as its control element to achieve self-timed behavior, where the circuit remains in stand-by mode means that the output propagates NULL and is ready to propagate a new DATA wave-front.



CDC: Complete Detection Circuit

Figure 4: NCL circuit

To accomplish this criterion, NCL system should consist of two DI NCL registers to prevent from over writing the current and previous DATA wave-fronts and is separated by NULL wave-front. The completion circuitry detects the incoming NULL/DATA inputs and requests signals from the subsequent stages. If the incoming signal is NULL and the stage is requesting for DATA then the detection circuit sends a signal request-for-DATA. Then the DI registers communicate with each other based on the request signals to achieve asynchronous behavior and achieves high speed operation [3, 8].

III. PROPOSED MULTI-THRESHOLD NULL CONVENTION LOGIC

NCL gates implement more complex Boolean functions with less threshold gates but consume more area overhead. Therefore, MTCMOS is incorporated in every NCL threshold gate so called Multi-Threshold NULL Convention Logic (MTNCL) to reduce area overhead [10].

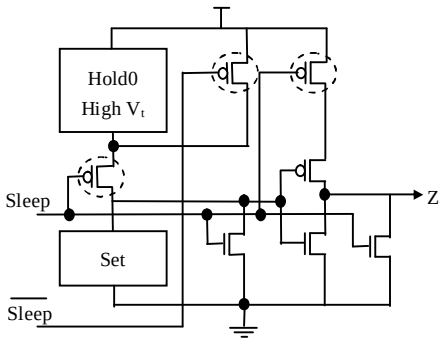


Figure 5: MTNCL architecture

This technique is to set the combinational circuit in stand-by mode (SLEEP) during NULL cycle. The sleep signal is propagated from the output signal (K_o) of the previous register stage. A request-for-NULL indicates that the stage is in active mode (DATA cycle) and a request-for-DATA indicates that the stage is in the SLEEP mode (NULL cycle). MTNCL needs lesser transistors than regular NCL per gate. The RESET circuit is not essential anymore since threshold logic gates are forced to go into sleep mode after every DATA cycle. The HOLD1 circuit when put to sleep since all threshold gates will become logic 0 in a stage; no longer hysteresis required [10-17].

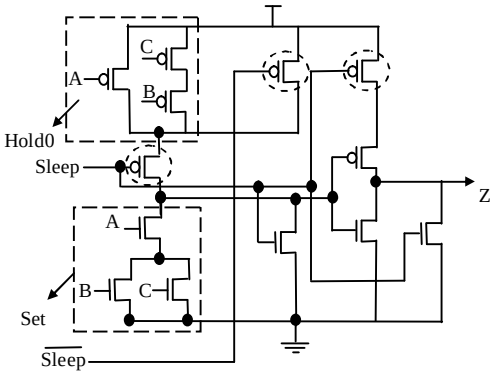


Figure 6: TH33w2 MTNCL

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The MTNCL implementation of TH33w2 is shown in figure 6 whose inputs, n=3 and threshold, m=3. Firstly assume all the inputs of the threshold logic gate are NULL. If a valid DATA is passed through input A, the output remains NULL since no threshold, m=3 is met. When the next valid DATA is given to either input B or C, the TH33w2 gate propagates the DATA value at the output of the gate since it meets the threshold, m=3 where the weight of input A is 2. Thus the complete DATA wave-front is propagated through the output of the gate insisting input DATA completeness in relation to NULL. When one of the input becomes NULL, the circuit produces DATA at the output due to its threshold value. To produce a complete NULL wave-front all the inputs of the gate must be NULL and hence the gate switches the output to NULL, ending the switching of DATA insisting input NULL completion with respect to DATA.

IV. EXPERIMENTAL ANALYSIS AND DISCUSSIONS

In this paper, MTNCL gates are designed and simulated to evaluate the average power, propagation delay and noise. The proposed MTNCL threshold gates are compared with standard CMOS, MTCMOS, and NCL designs. To compare MTNCL performance to other logic design styles, we have performed simulation on Tanner EDA tools. Each threshold gate has been analyzed in terms of average power, propagation delay, noise and power-delay product (PDP) and the values are measured. The area overhead of the proposed circuits is lower than that of conventional NCL circuits. By exploiting HVT and LVT cells, it is possible to improve the speed of the gate without significantly increasing the power consumption, and to achieve minimum power-delay product.

4.1. Average Power

Power is a key characteristic of an experimental design. Table II shows the average power simulation results of MTNCL, NCL, MTCMOS and CMOS gates. Where the average power is calculated as

$$P_{avg} = P_{dynamic} + P_{static} + P_{short\text{-}circuit} + P_{leakage}$$

Where P_{avg} is the total average power, $P_{dynamic}$ is the total dynamic power, P_{static} is the total static power while $P_{short\text{-}circuit}$ is the short circuit power and $P_{leakage}$ is the leakage power dissipated by the circuit.

The analysis shows that designs based on MTNCL principle gives superior performance when compared to traditional approaches in terms of power. So for low power and ultra low power requirements Multi-Threshold NULL convention logic is an effective alternative for traditional logic circuit designs.

Table II: Average Power Comparision (W)

Threshold GATES	CMOS	MTCMOS	NCL	Proposed MTNCL
TH12	4.9×10^{-5}	6.5×10^{-5}	6.5×10^{-5}	2.9×10^{-5}
TH22	6.0×10^{-5}	7.9×10^{-5}	7.6×10^{-5}	3.1×10^{-5}
TH13	2.0×10^{-5}	3.7×10^{-5}	2.9×10^{-5}	2.1×10^{-5}
TH23	5.1×10^{-5}	6.0×10^{-5}	3.1×10^{-5}	2.6×10^{-5}
TH33	2.9×10^{-5}	5.4×10^{-5}	3.2×10^{-5}	2.1×10^{-5}
TH23W2	3.3×10^{-5}	4.7×10^{-5}	3.1×10^{-5}	2.2×10^{-5}
TH33W2	3.0×10^{-5}	5.0×10^{-5}	3.5×10^{-5}	2.2×10^{-5}
TH14	9.0×10^{-5}	3.0×10^{-5}	1.4×10^{-5}	1.6×10^{-5}
TH24	3.6×10^{-5}	4.3×10^{-5}	2.0×10^{-5}	2.0×10^{-5}
TH34	3.7×10^{-5}	4.9×10^{-5}	1.7×10^{-5}	2.1×10^{-5}
TH44	1.5×10^{-5}	3.9×10^{-5}	1.8×10^{-5}	1.6×10^{-5}
TH24W2	2.4×10^{-5}	3.7×10^{-5}	1.7×10^{-5}	1.8×10^{-5}
TH34W2	3.0×10^{-5}	4.8×10^{-5}	1.0×10^{-5}	1.8×10^{-5}
TH44W2	2.9×10^{-5}	4.5×10^{-5}	1.1×10^{-5}	2.0×10^{-5}
TH34W3	1.6×10^{-5}	3.2×10^{-5}	1.7×10^{-5}	1.6×10^{-5}
TH44W3	1.5×10^{-5}	3.5×10^{-5}	1.8×10^{-5}	1.6×10^{-5}
TH24W22	1.7×10^{-5}	3.0×10^{-5}	1.6×10^{-5}	1.7×10^{-5}
TH34W22	2.7×10^{-5}	3.9×10^{-5}	2.1×10^{-5}	1.8×10^{-5}
TH44W22	2.6×10^{-5}	4.3×10^{-5}	1.5×10^{-5}	1.9×10^{-5}
TH54W22	1.8×10^{-5}	4.2×10^{-5}	2.0×10^{-5}	1.7×10^{-5}
TH34W32	1.7×10^{-5}	3.3×10^{-5}	1.6×10^{-5}	1.6×10^{-5}
TH54W32	1.8×10^{-5}	3.8×10^{-5}	1.8×10^{-5}	1.7×10^{-5}
TH44W322	2.2×10^{-5}	3.6×10^{-5}	1.7×10^{-5}	1.7×10^{-5}
TH54W322	2.7×10^{-5}	3.9×10^{-5}	1.9×10^{-5}	1.8×10^{-5}
THxor0	4.1×10^{-5}	4.7×10^{-5}	1.5×10^{-5}	2.0×10^{-5}
THand0	2.8×10^{-5}	7.4×10^{-5}	1.4×10^{-5}	1.9×10^{-5}
TH24comp	3.3×10^{-5}	4.4×10^{-5}	1.7×10^{-5}	1.9×10^{-5}

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4.2. Propagation Delay

The propagation delay for each transition is a measure from 50% of the input voltage swing to that of the output voltage swing.

$$T_{pd} = \frac{(T_{phl} + T_{plh})}{2}$$

The propagation delays of the proposed MTNCL gates are measured and compared with other logic gates and valuated in table III. Compared to other logic designs MTNCL offers better delay and achieves higher speed of operation but the downside is the traditional CMOS design propagates low delay.

Table III: Delay Comparison (ns)

Threshold GATES	CMOS	MTCMOS	NCL	Proposed MTNCL
TH12	20.60n	100.67n	20.79n	100.65n
TH22	19.95n	82.09n	20.71n	99.95n
TH13	46.62n	120.77n	40.81n	120.76n
TH23	623.93p	62.44n	40.81n	80.45n
TH33	40.15n	62.59n	40.45n	119.95n
TH23W2	40.44n	62.63n	40.78n	120.50n
TH33W2	39.95n	62.85n	40.83n	120.39n
TH14	80.80n	80.85n	80.90n	80.78n
TH24	776.44p	80.74n	80.93n	80.66n
TH34	380.41p	22.66n	80.91n	40.58n
TH44	80.13n	22.67n	80.87n	80.22n
TH24W2	786.59p	80.76n	80.93n	80.71n
TH34W2	40.37n	80.60n	80.91n	80.53n
TH44W2	40.53n	23.09n	80.90n	40.69n
TH34W3	80.61n	80.55n	80.92n	80.48n
TH44W3	80.41n	80.46n	80.88n	80.45n
TH24W22	80.68n	80.78n	80.93n	80.74n
TH34W22	754.54p	80.58n	80.92n	80.50n
TH44W22	419.87p	22.68n	80.91n	80.42n
TH54W22	80.22n	22.89n	80.86n	79.95n
TH34W32	80.64n	80.65n	80.92n	80.54n
TH54W32	79.95n	22.76n	80.90n	80.40n
TH44W322	767.11p	80.62n	80.92n	80.60n
TH54W322	437.29p	80.58n	80.91n	80.43n
THxor0	245.37p	22.78n	80.91n	80.42n
THand0	541.27p	80.49n	80.92n	80.44n
TH24comp	454.20p	40.68n	80.91n	40.66n

4.3. Noise

Noise is an indiscriminate fluctuation in a circuit. The standard CMOS digital design styles generates more noise in the circuit affecting the system performance. To mitigate this effect the novel MTNCL approach is exploited. From table IV the evaluated results suggest that the MTNCL generates less noise compared to CMOS and MTCMOS designs and generates more noise than the conventional NCL design due to the generation of glitches.

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Table IV: Noise Comparison (V)

Threshold GATES	CMOS	MTCMOS	NCL	Proposed MTNCL
TH12	1.70K	1.16K	73.26	400.59
TH22	1.27X	487.49K	73.11	30.24K
TH13	1.13K	865.63	165.43	300.42
TH23	823.49K	463.30K	165.28	179.23K
TH33	3.50X	1.19X	165.30	410.56K
TH23W2	393.83K	263.58K	165.51	18.15K
TH33W2	196.99K	82.32K	165.31	26.34K
TH14	852.23	690.32	524.58	240.31
TH24	31.81K	21.47K	263.10	7.80K
TH34	959.17K	578.57K	263.01	187.58K
TH44	8.10X	3.01X	263.05	821.57K
TH24W2	51.53K	36.29K	262.58	7.04K
TH34W2	115.81K	62.76K	263.10	22.16K
TH44W2	440.36K	182.05K	263.08	54.69K
TH34W3	715.20K	512.28K	262.47	224.51K
TH44W3	117.12K	76.25K	263.10	26.13K
TH24W22	232.86K	180.34K	261.62	12.97K
TH34W22	46.68K	28.17K	263.10	9.26K
TH44W22	1.23X	777.99K	263.01	236.97K
TH54W22	4.12X	2.20X	263.04	1.00X
TH34W32	78.76K	50.60K	262.23	16.47K
TH54W32	883.64K	368.97K	263.07	110.96K
TH44W322	106.57K	61.01K	263.10	20.32K
TH54W322	970.22K	631.08K	263.08	262.51K
THxor0	597.12K	340.80K	263.03	22.65K
THand0	507.28K	309.63K	262.97	20.91K
TH24comp	597.12K	340.80K	263.03	22.65K

4.4. Power-Delay Product (PDP):

The PDP is the quantitative measure of circuit efficiency and a concession between power and propagation delay.

$PDP = P.T$

The requirements are same as power and delay simulation steps. From table V the simulation results suggest that the proposed MTNCL has higher system performance than the MTCMOS design. Due to generation of more propagation delay than CMOS logic the efficiency of the system is reduced and trade-off exists between NCL and MTNCL.

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Table V: Power-Delay Product (PDP) Comparison (W.s)

Threshold GATES	CMOS	MTCMOS	NCL	Proposed MTNCL
TH12	1.02×10^{-12}	6.54×10^{-12}	1.35×10^{-12}	2.91×10^{-12}
TH22	1.19×10^{-12}	6.48×10^{-12}	1.57×10^{-12}	3.09×10^{-12}
TH13	9.32×10^{-13}	4.46×10^{-12}	1.22×10^{-12}	2.53×10^{-12}
TH23	3.23×10^{-14}	3.86×10^{-13}	1.29×10^{-12}	2.09×10^{-12}
TH33	1.17×10^{-12}	3.37×10^{-12}	1.30×10^{-12}	2.51×10^{-12}
TH23W2	1.35×10^{-12}	2.94×10^{-12}	1.26×10^{-12}	2.65×10^{-12}
TH33W2	1.23×10^{-12}	3.14×10^{-12}	1.31×10^{-12}	2.64×10^{-12}
TH14	7.32×10^{-13}	2.42×10^{-12}	1.14×10^{-12}	1.29×10^{-12}
TH24	2.60×10^{-14}	3.47×10^{-12}	1.64×10^{-12}	1.61×10^{-12}
TH34	1.41×10^{-14}	1.11×10^{-12}	1.37×10^{-12}	8.52×10^{-13}
TH44	1.20×10^{-12}	8.84×10^{-13}	1.49×10^{-12}	1.28×10^{-12}
TH24W2	1.92×10^{-14}	2.98×10^{-12}	1.40×10^{-12}	1.45×10^{-12}
TH34W2	1.22×10^{-12}	3.86×10^{-12}	8.33×10^{-12}	1.44×10^{-12}
TH44W2	1.20×10^{-12}	1.03×10^{-12}	8.97×10^{-12}	8.13×10^{-13}
TH34W3	1.35×10^{-12}	2.57×10^{-12}	1.43×10^{-12}	1.28×10^{-12}
TH44W3	1.21×10^{-12}	2.81×10^{-12}	1.46×10^{-12}	1.28×10^{-12}
TH24W22	1.37×10^{-12}	2.42×10^{-12}	1.31×10^{-12}	1.37×10^{-12}
TH34W22	2.09×10^{-14}	3.14×10^{-12}	1.69×10^{-12}	1.44×10^{-12}
TH44W22	1.10×10^{-14}	9.75×10^{-13}	1.23×10^{-12}	1.52×10^{-12}
TH54W22	1.48×10^{-12}	9.61×10^{-13}	1.65×10^{-12}	1.35×10^{-12}
TH34W32	1.37×10^{-12}	2.66×10^{-12}	1.35×10^{-12}	1.28×10^{-12}
TH54W32	1.47×10^{-12}	8.64×10^{-12}	1.52×10^{-12}	1.36×10^{-12}
TH44W322	1.73×10^{-14}	2.90×10^{-12}	1.37×10^{-12}	1.37×10^{-12}
TH54W322	1.19×10^{-16}	3.14×10^{-12}	1.55×10^{-12}	1.48×10^{-12}
THxor0	1.01×10^{-15}	1.07×10^{-12}	1.26×10^{-12}	1.60×10^{-12}
THand0	1.53×10^{-14}	5.95×10^{-12}	1.16×10^{-12}	1.52×10^{-12}
TH24comp	1.49×10^{-14}	1.78×10^{-12}	1.40×10^{-12}	7.72×10^{-13}

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V. CONCLUSION AND FUTURE SCOPE

In this paper, we present an efficient technique for low power high speed operations. As seen from the results, MTNCL offers low power compared to other designs. So the proposed low power MTNCL design consume less power and can be said that it is a power aware logic which is compatible in today's semiconductor design. There is also an improvement in the delay and offers high speed compared to the NCL and MTCMOS designs but slower than CMOS design. The proposed design is more robust to noise compared to CMOS and MTCMOS design styles and less compared to NCL due to the presence of glitches. This thesis can be extended further for the future work to reduce the delay requirements as compared to the CMOS logic designs and to further reduce the propagation of glitches to improve the system performance.

REFERENCES:

[1]. S.C. Smith and J. Di, "Designing asynchronous circuits using NULL Convention Logic (NCL)," Synthesis Lectures on Digital Circuits and Systems: Morgan & Claypool Publishers, 2009.
[2]. S. Mutoh, T. Douseki, Y. Matsuya, T. Aoki, S. Shigematsu, and J. Yamada, "1-V Power Supply High-Speed Digital Circuit Technology with Multithreshold-Voltage CMOS," IEEE Journal of Solid-State Circuits, Vol. 30/8, pp. 847-854, August 1995.
[3]. Karl M. Fant and Scott A. Brandt, .NULL Convention Logic: A Complete and Consistent Logic for Asynchronous Digital Circuit Synthesis, International Conference on Application Specific Systems, Architectures, and Processors, pp. 261-273, 1996.
[4]. J.Sudhakar, A. Mallikarjuna Prasad, Ajit Kumar Panda, " Multi Objective Analysis of NCL Threshold Gates with Return To Zero Protocols", IOSR Journal of Electronics and Communication Engineering (IOSR-JECE), Volume 10, Issue 3, Ver. II (May - Jun.2015), PP 12-17.
[5]. Farhad. A. Parsan and Scott. C. Smith, "CMOS Implementation Comparison of NCL Gates," IEEE Int. Midwest Sym. on Circuits and Systems (MWSCAS), Aug. 2012.
[6]. Farhad A. Parsan and Scott C. Smith, "CMOS Implementation of Static Threshold Gates with Hysteresis: A New Approach", IEEE/IFIP Int. Conf. on VLSI and System-on_Chip (VLSI-SoC), Oct. 2012.
[7]. Gerald E. Sobelman and Karl M. Fant, "CMOS Circuit Design of Threshold Gates with Hysteresis," IEEE International Symposium on Circuits and Systems (II), pp. 61-65, 1998.
[8]. S. C. Smith, R. F. DeMara, J. S. Yuan, D. Ferguson, and D. Lamb, "Optimization of NULL Convention Self-Timed Circuits," Elsevier's Integration, the VLSI Journal, Vol. 37/3, pp. 135 165, August 2004.
[9]. David Roclin, "Optimum Transistor Sizing of MTNCL Threshold Gates for Various Design Constraints", M.S thesis, Université du Maine, 2008.
[10]. Andrew Bailey, Ahmad Al Zahrani, Guoyuan Fu, Jia Di, and Scott Smith, "Multi-Threshold Asynchronous Circuit Design for Ultra-Low Power", Journal of Low Power Electronics Vol.4, 1–12, 2008.
[11]. A. Alzahrani, A. Bailey, G. Fu, and J. Di, "Glitch-Free Design for Multi-Threshold CMOS NCL Circuits", Great Lake Symposium on VLSI, 2009.
[12]. A. D. Bailey, J. Di, S. C. Smith, and H. A. Mantooth, "Ultra-Low Power Delay-Insensitive Circuit Design," IEEE Midwest Symposium on Circuits and Systems, pp. 503-506, August 2008.
[13]. S.C. Smith and J. Di, "Ultra-low power multi-threshold asynchronous circuit design", US patent 7977972 B2, July 12, 2011.
[14]. Liang Zhou and Scott C. Smith, Jia Di, "Bit-Wise MTNCL: An Ultra-Low Power Bit-Wise Pipelined Asynchronous Circuit Design Methodology", Circuits and Systems (MWSCAS), 2010 53rd IEEE International Midwest Symposium on, Aug, 2010.
[15]. Harish Gopalakrishnan, "Energy Reduction for Asynchronous Circuits in Soc Applications", Ph.D. dissertation, Wright State University, 2005
[16]. F.A. Parsan, J. Zhao, S.C. Smith, "SCL Design of a Pipelined 8051 ALU", Circuits and Syatems (MWSCAS), 2014 IEEE 57th International Mdweat Symposium on, Aug, 2014.
[17]. Liang Zhou and Scott C. Smith, "Standby Power Reduction Techniques for Asynchronous Circuits with Indeterminate Standby States", International Conf. Computer Design, CDES 2011.