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180nm Technology Based Low Power Hybrid CMOS Full Adder

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ABSTRACT

We have designed the hybrid full Adder using CMOS logic style by dividing it in three modules so that it can be optimized at various levels. 1st module is an XOR-XNOR circuit, which generates the full swing XOR and XNOR outputs simultaneously and have a good driving capability. It also consumes the minimum power and provides better delay performance. 2nd module is a sum circuit which is also a XOR circuit and uses carry input and the output of the 1st module as input to generate sum output. 3rd module is a carry circuit which uses the output of the first stage and other inputs to generate the carry output. In this paper we have proposed new full adder circuit which reduce the power consumption, delay between carry out to carry in. Simulations are carried out on CADENCE Virtuoso Version.6.1.5 using GPDK 180nm technology CMOS processes.

Key words : Adder, Low Power Design, Hybrid-CMOS logic, High Speed.

1. INTRODUCTION

It has several demerits such as charge sharing, high clock load, higher switching activities and lower noise immunity and it requires high power for driving the clock lines. Another logic styles are transmission-gate full adder (TGA)[5] and transmission-function full adder (TFA)[6] based upon transmission gates and transmission function theory.
These full adders consume low power, but have very low driving capabilities. Hybrid-CMOS logic design style uses more than one module for designing of full adder. Examples of this style are NEW 14-T adder [7], hybrid pass logic with static CMOS output drive full adder [8],In this design style full adder structure is designed by breaking the full adder into three modules. Module I is an XOR-XNOR circuit which drives the other modules, So it must have good driving capability and provide full swing outputs simultaneously. Module II and Module III are the sum and carry circuits which use the output of first module and third input signal as input to produce the sum and carry outputs respectively. General structure of hybrid CMOS design style is shown in Fig.1. This logic design style provides the freedom to take the optimum circuits for every module for getting the optimum performance of adder cell. These adders generally lack the driving for the capabilities. Their performance as a single bit is good, but as the size of chain increases, the performance degraded drastically. But in this paper we tried to present an adder cell with this logic style for which the performance is not degraded in adder chain. We tried to get better delay performance from Cin to Cout and evaluate the performance of adder cell in 4 bit adder chain and 8 bit adder chain.

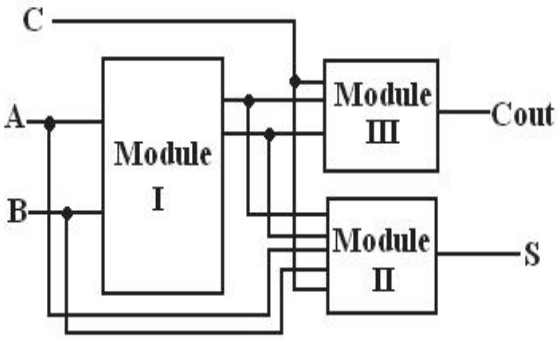

Fig1: General form of Hybrid-CMOS Logic Design.

In the recent year, many other new circuits are proposed using less number of transistors with less delay and very low power requirement. An adder with 10 transistors[12],[15] an adder with 8 transistors[16] do not give full swing outputs for all input combinations and there is difference in output level for different combinations and these circuits have very low driving capabilities. Some other logic circuits are also proposed in [13] but they do not give full swing output for all input combinations and power requirement is more. We do not take these adders in our discussion due to they do not provide full swing output. The rest of the paper is organized as follows. Section II gives brief introduction of Hybrid CMOS Logic Design style and some XOR-XNOR circuits. Section III consists of explanation of proposed module II and module III circuits and proposed full adder cell. Section IV explains the simulation results and analytical comparisons and Section V gives a conclusion.

2.HYBRID-CMOS LOGIC DESIGN

The sum (S) and carry (C_{out}) expression for a 1-bit full adder with three binary inputs A, B and C_{in} are given by

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$S = A \oplus B \oplus C$ (1)

$C_{out} = A.B + C_{in} . (A \oplus B)$ (2) In hybrid-CMOS architecture, we get XOR and XNOR of A and B inputs as the intermediate signal at the output of module I. These input signals and C_{in} are available for the input of module II and module III. So we get new expression for sum and carry using XOR output H and XNOR output H'

$S = H \oplus C_{in} = H.C_{in}' + H' C_{in}$ (3)

$C_{out} = H'.A + H.C_{in}$ (4)

Where (.)' is used for the complement of the signal. Module I circuit is an XOR-XNOR circuit.

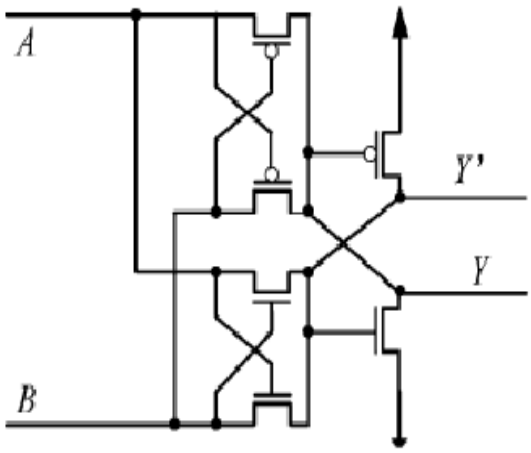

Fig 2.1: XOR-XNOR 6 T gate

Many XORXNOR circuits are proposed by many authors. Circuit shown in fig. 2.1 use only 6 transistors and provide full output swing. This circuit is widely used in hybrid CMOS logic style. This circuit requires low power and provides low delay and due to the feedback transistors at the output connected with supply voltage and ground provide good driving capability. But some combination of inputs such as "00" and "11" it provides little bit higher delay. The circuit shown in fig 2.2. is an improved version of this circuit in this circuit pull up and pull down transistors are used to improve the delay performance of the circuit for these combinations. But the drawback of this circuit is that the overall delay is increased. The circuit shown in fig.2.3 , provides full output swing for XOR and XNOR simultaneously and provide good driving capability but due to use of inverter circuit at one of the input the power requirement is higher. There are many other XOR – XNOR circuits but most of them do not meet our requirements of simultaneously full XOR- XNOR output swing and good driving capability.

3. PROPOSED FULL ADDER

A. Module II Circuit

The expression of the sum (3) shows that module II circuit is only an XOR circuit. For an XOR gate when input H will be at logic '0' then output will follow the other input, it can be implemented by using one NMOS to pass logic '0' by connecting the gate terminal with H', source terminal with Cin and drain terminal at the output, and one PMOS to pass the logic '1' by connecting the source terminal with Cin, gate terminal with H and drain with the output. When H will be at logic 0 and H' will be at logic 1, both transistors will be on and output will be connected to Cin, So when Cin will be at logic '1' output will be connected to logic '1' and when it will be at logic '0' output will also be connected to logic '0'. Both the transistors will be in off state for H to be at logic '1'. When the inputs H and Cin will be at logic '1', then the output is low, it is implemented by connecting two NMOS in series with their gate terminals connected to H and Cin, source terminal of one of the NMOS is connected to the grounded and the source terminal of other is connected to the output . Similarly, when H is at logic '1' and Cin is at logic '0', the output is at logic 1 so we use two PMOS in series with source terminal of one of the PMOS at logic high, drain terminal of other PMOS at output and the gate terminals are connected with H and Cin espectively. When both inputs will be at logic '1' then output will be connected to ground and the output will be at logic '0', when H will be at logic '1' and Cin will be at logic '0' both inputs H' and Cin will be at logic '0' and both transistor will be on and output will be connected to power supply and we get logic '1' at the output.

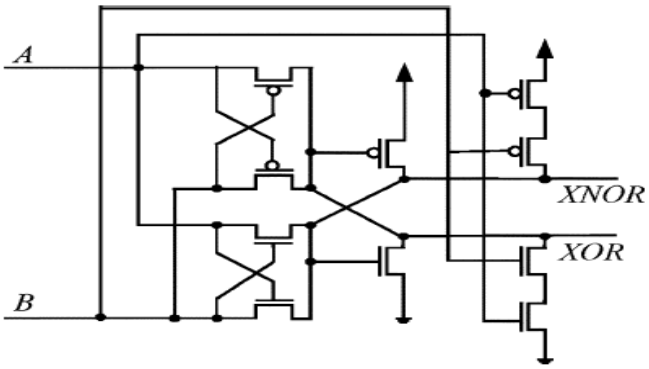

Fig 2.2: Modified 1 XOR-XNOR circuit

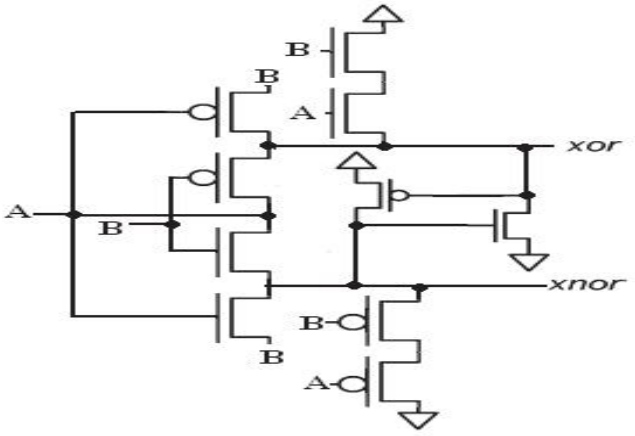

Fig 2.3: Modified 1 XOR-XNOR circuit 1

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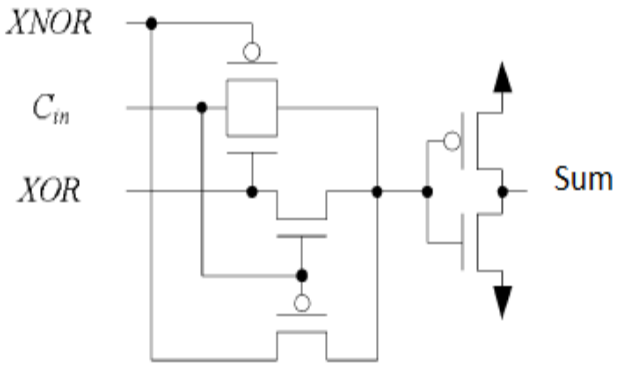

Fig 3: Module II Sum circuit

In the designing of circuit we try to avoid the use of inverters to reduce the power consumption and the logic high passes by PMOS while Logic low passes by NMOS to get the minimum delay as shown in fig 3.

B. Module III Circuit

Module III circuit is a multiplexer which select Cin if H is at logic '1' else selects A or B as the output Cout as shown in (5). In the proposed circuit we use transmission gate with H and H' at the gate terminals of NMOS and PMOS respectively to pass the Cin to Cout for H at logic high or when other inputs A and B are at different logic level. When the H is at logic '0' or both inputs A and B are at same logic level we have to pass any of these inputs to the output. So we use one PMOS and one NMOS to pass input A by one transistor and other input B by another transistor. By the use of these two inputs from two sides it improves the performance of the circuit. The proposed circuit is shown in fig. 4.

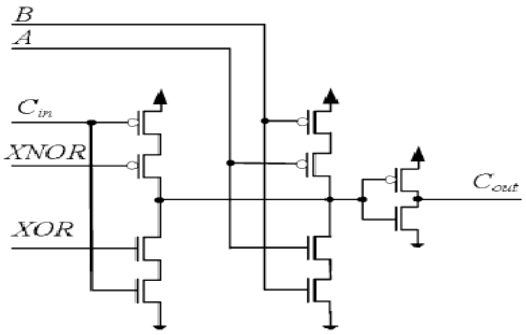

Fig 4: Module III Carry Circuit

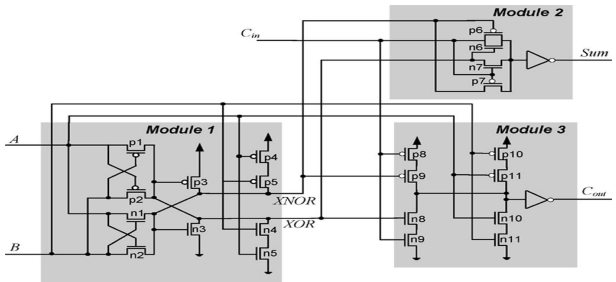

Fig 5: Proposed Full Adder

4.SIMULATION RESULTS

The transient analyses of the circuits were performed on CADENCE Virtuoso Ver.6.1.5 GPDK 180nm CMOS process. For providing the real environment to the simulation we use input buffers for all the inputs and a constant output for power and delay measurements. The simulation test bench is used as shown in Fig. 7.

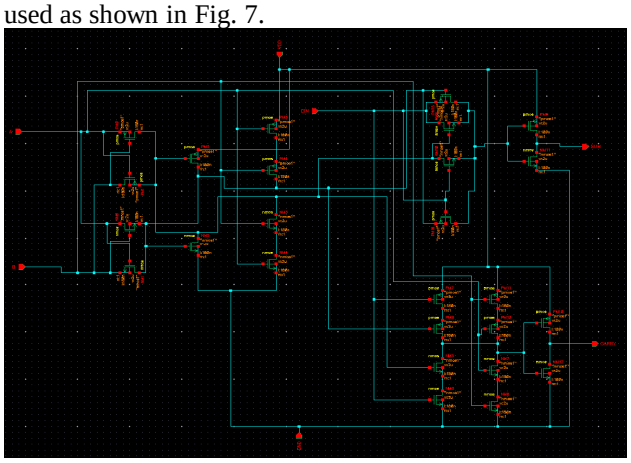

Fig 6: Schematic of Proposed Full Adder

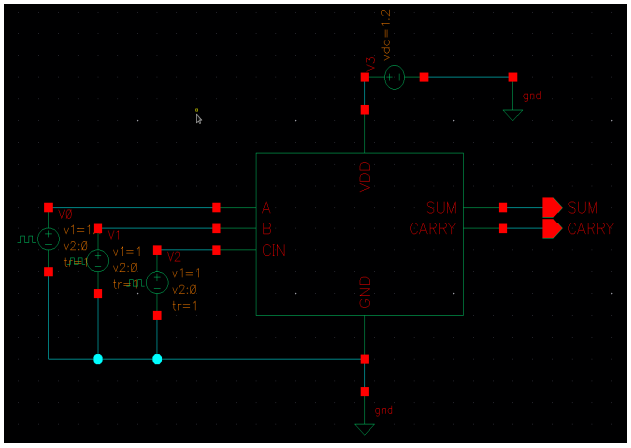

Fig 7: Test Circuit for Full Adder

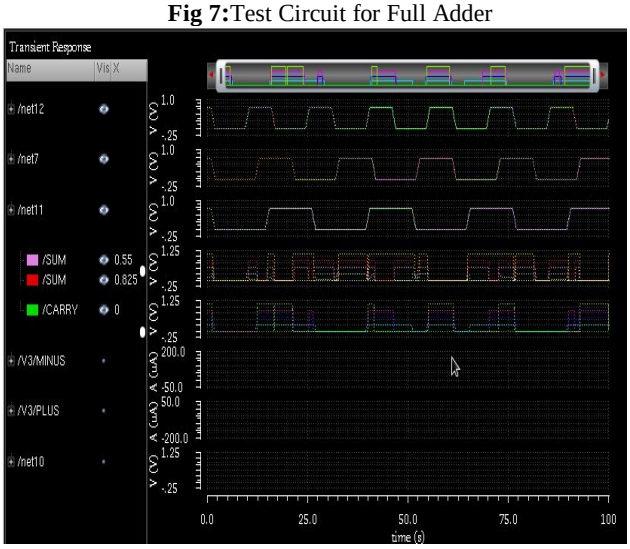

Fig 8: Output waveform for Full Adder

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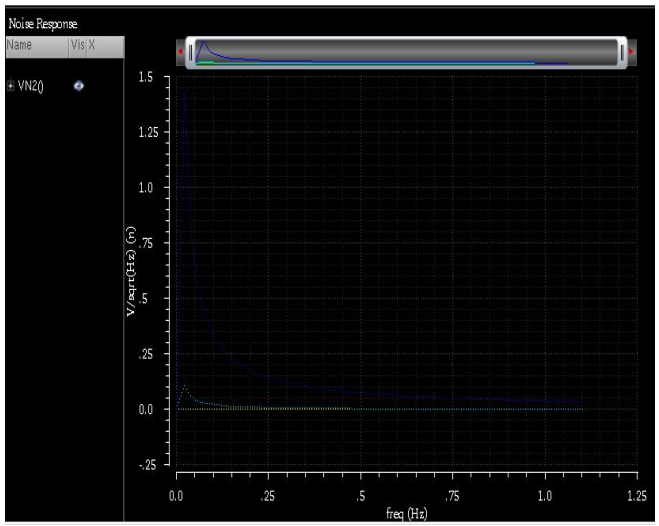

Fig 9: Noise Analysis for Full Adder

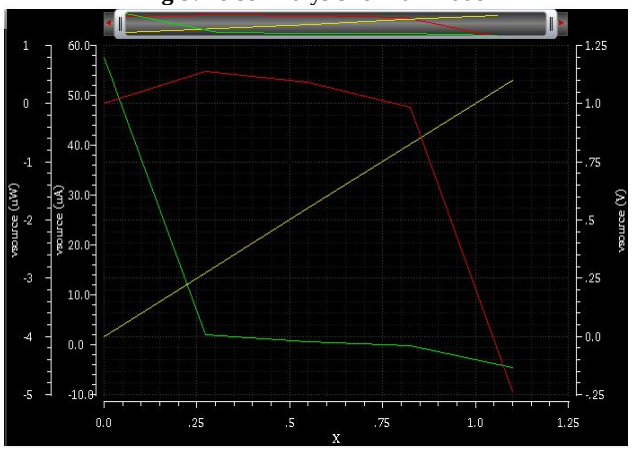

Fig 10: Power Analysis for Full Adder

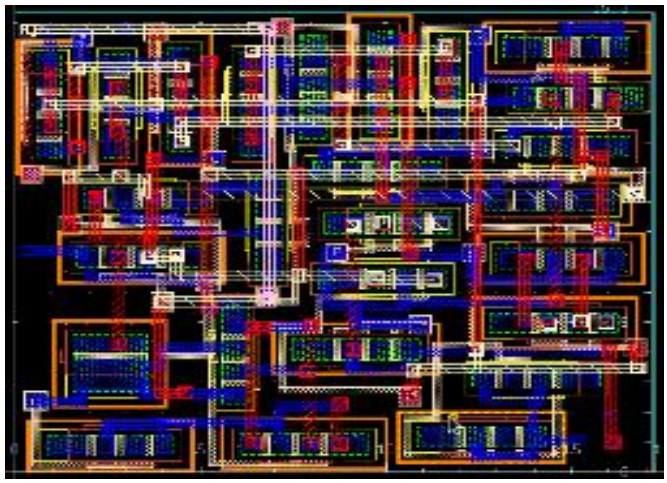

Fig 11: Layout for Full Adder

POWER,DELAY COMPARISION OF FULL ADDERS

VCC(V)	0.7	0.8	0.9	1.0	1.2	1.4	1.6	1.8

Power (μW)

HYBRID	0.318	0.824	0.916	0.978	1.507	2.154	3.368	3.798
C-CMOS	0.84	1.45	2.12	3.63	4.91	6.23	8.77	12.4
CPL	1.03	1.70	2.64	4.8	5.64	7.72	11.2	14.0
TFA	1.50	2.28	3.60	4.56	6.25	8.25	10.6	14.9
TGA	1.49	2.20	3.30	4.29	6.12	8.47	10.0	12.3
14T		3.66	7.62	8.14	9.82	12.7	18.8	26.0
10T						44.4	56.5	70.7

DELAY for sum and carry values

delay(?wf1 VT("/net9"), ?value1 0....

x	delay(?...le nil)	delay(?...le nil)	delay(?...le nil)
0.000	10.76	10.76	4.764
300.0E-3	10.76	10.76	4.762
600.0E-3	10.79	14.20	8.200
900.0E-3	10.89	14.20	8.200
1.200	10.95	14.20	8.200

C-CMOS	1.42	0.756	0.531	0.397	0.333	0.292	0.269	0.252
CPL	0.908	0.468	0.321	0.236	0.197	0.184	0.179	0.172
TFA	1.53	0.777	0.511	0.385	0.322	0.288	0.270	0.172
TGA	1.42	0.721	0.497	0.383	0.321	0.294	0.274	0.255
14T		8.30	2.06	0.902	0.531	0.382	0.303	0.257
10T						3.61	1.85	0.986

Comparison of the worst case Cin to Cout delay, power consumption, for carry outputs at the supply voltage range of 0.8V-1.8V of reported and proposed circuit is shown in Fig. 5.The delay comparison of Cin to Cout for circuits described in section I using the same logic style design and proposed the Circuit given in fig. 2 for the supply voltage range from 0.8V-1.8V is shown in fig. 6. The proposed circuit gives comparable performance with the circuit describes in [7] and 55% to 57% faster than other reported circuits at 1.8V voltage supply in terms of worst case Cin to Cout delay. The average power consumption is measured with the same input settings and same input range as for the propagation delay measurement. The comparison of simulation results for proposed circuit and other reported circuits for the average power consumption is shown in Fig. 10. Subsequently the average dynamic power of proposed circuit is 13.8% to 30.8% lowers than the reported circuits for the input voltage 1.8V when compared with the other circuits of the same logic style.

5.CONCLUSION

For full adder cell design, pass-logic circuit is thought to be dissipating minimal power and have smaller area because it uses less number of transistors. Thus,the CPL adder is considered to be able to perform better than C-CMOS adder in [12]. However, in our opinion, pass-logic circuit usually has irregular structure, which increases the wiring complexity and its performance is highly susceptible to transistor sizing.

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On the other hand, the complementary CMOS logic circuit has the advantages of layout regularity and stability at low voltage. Therefore, it is the different design constraints imposed by the applications that each logic design style has its place in the cell library development.

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