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Study of Plasma Induced Damage (PID) through Surface Volt-age Measurement for Helical Resonator Plasma (HRP) Ashers

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ABSTRACT

This paper presents an important observation on the total surface charge collection, which correlates with plasma induced damage (PID) during plasma ashing process using the quantox wafers in the measurement of the surface voltage (Vs) on the wafer surface using a contact-less Kelvin Probe for changes in parameters during plasma ashing. It is known that plasma ashing process do contribute for PID, along with other plasma processes. In this report, it is covered on the study on how processing condition change can impact the PID, in terms of total surface charge collection and also the uniformity of the charges on the wafer surface. In this study, we covered the helical resonator plasma (HRP) asher and tested 5 parameters with various conditions, which where the process time, pressure, gas flow, power and temperature. It suggested that changes in the condition of these parameters do impact on the total surface charge collection and also the uniformity of the charges on the wafer surface.

Key words : Helical Resonator Plasma (HRP) Asher; Plasma Ashing; Plasma Induced Damage; Surface Voltage Measurement.

1. INTRODUCTION

In the last 50 years, development in the semiconductor industry is rapid and newer technology has been introduced to the vast market for faster and efficient usage. Ranging from the technology of 10um to the currently developed 14nm, Plasma Induced Damage (PID) is something that cannot be measured in-line on production wafer and can only be tested during the electrical test and/or functional test. Various kinds of plasma processes in the industry such as deposition, implantation, oxidation and dry etching, are known for their risk of causing PID, which can be defined as the damage caused by the charges in the plasma that get trapped in the thin gate oxide and change the transistor characteristics, which eventually impacts the electrical and functional characteristics, as well as the reliability of the device [1 – 4, 12].Plasma ashing; also known as Plasma Resist Strip (PRS) process is known to have a high risk of causing PID. PRS is a process of removing the photoresist (PR) used and residues/polymer formed at the post-etching or post-implant step [5, 11]. The PID caused by the plasma ashing process is generally random. The common causes for PID are due to the electron charges present in the plasma and the continuous ion bombardment on the surface of the wafer during processing [1 – 2, 11]. Many types of PRS tools and conditions are present in the industry, which exhibit different impact during the process. Generally, there are single wafer processing PRS and batch processing PRS. Different conditions are utilized for different process post-steps, as it may impact on the defect density as well as the performance of the device [6, 8].The most commonly used method for measuring PID is through the measurement of the surface voltage (Vs) on the wafer surface using a contactless Kelvin Probe. A surface voltage is usually the result of surface or insulator charge or work function difference and it is most commonly detected with a non-contacting probe, Kelvin Probe [9].

2. EXPERIMENTAL DETAILS

2.1 Quantox Wafers

Quantox wafers are a high quality 1000Å thermally grown wet oxide on a p-type substrate wafer using a furnace. Individual quantox wafers were used for each condition and at each tool group for this analysis. The full map surface voltage (V_s) measurement was done using the Quantox tool, which applies 1793 measurement locations per wafer. The Quantox measurement map is as illustrated in Figure 1 below.

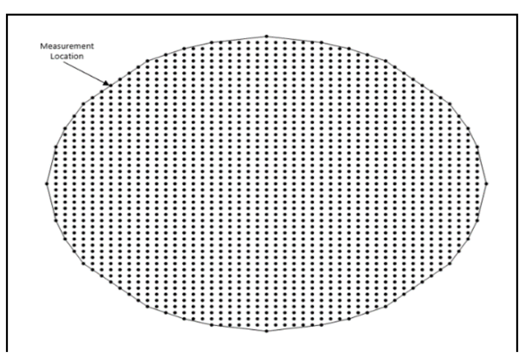


Figure 1: Quantox Measurement Map

Figure 2 below shows the thermally grown oxide on the p-type substrate used for this study. P-type substrate is preferred since minimal treatment is required as compared to n-type substrate that requires chemical treatment for stable depletion of the surface potential barriers [9].

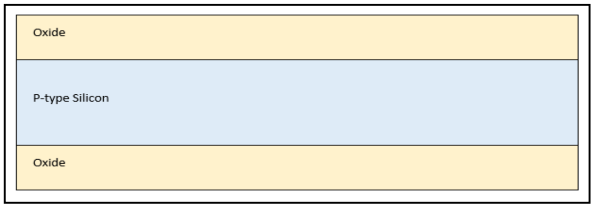


Figure 2: P-type Substrate Wafer

2.2 Quantox Measurement Tool

Surface voltage (V_s) measurement is done using the vibrating Kelvin Probe. It is done to detect the localized surface static charge gradients via the V_s mapping that may differ with different conditions due to non-uniform plasma in the chamber [9]. Magnitude of plasma damage is higher if the non-uniformity and/or the total surface charge is high. Figure 3 depicts the V_s measurement executed in this study.

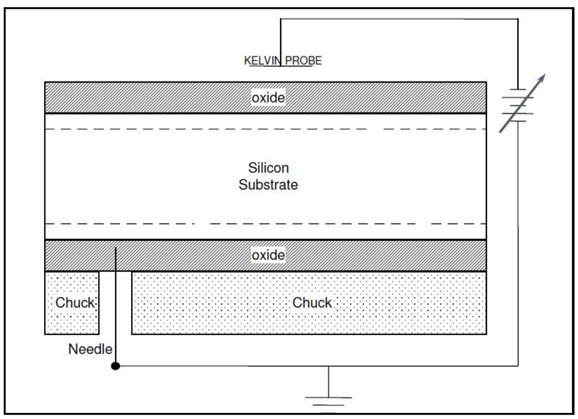


Figure 3: Surface Voltage (V_s) Measurement with Quantox Backside Contact

2.3 Asher Model

In the industry, many models of plasma ashers are used for mass production. Generally used models are the Inductively Coupled Plasma (ICP), Helical Resonator Plasma (HRP) and the Barrel Plasma ashers [7, 10]. In this study, the ICP plasma asher model is studied by varying the processing parameters, in order to understand the impact on the plasma and production wafers.

The HRP asher model used in this study, is as illustrated in Figure 4. This is a one chamber configuration, wherein the wafer is placed on the suspector and based on the processing condition, the ashing process occurs.

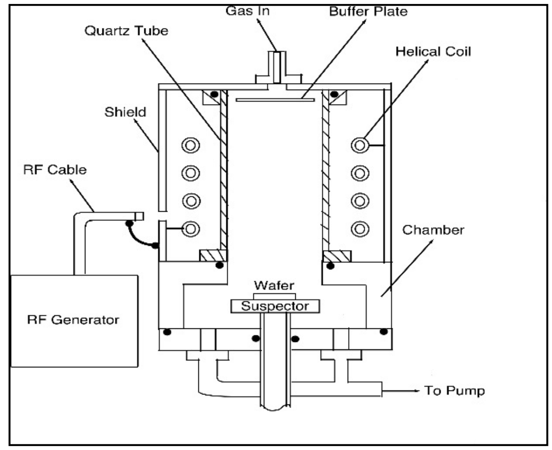


Figure 4: HRP Asher Model

3. RESULTS AND DISCUSSION

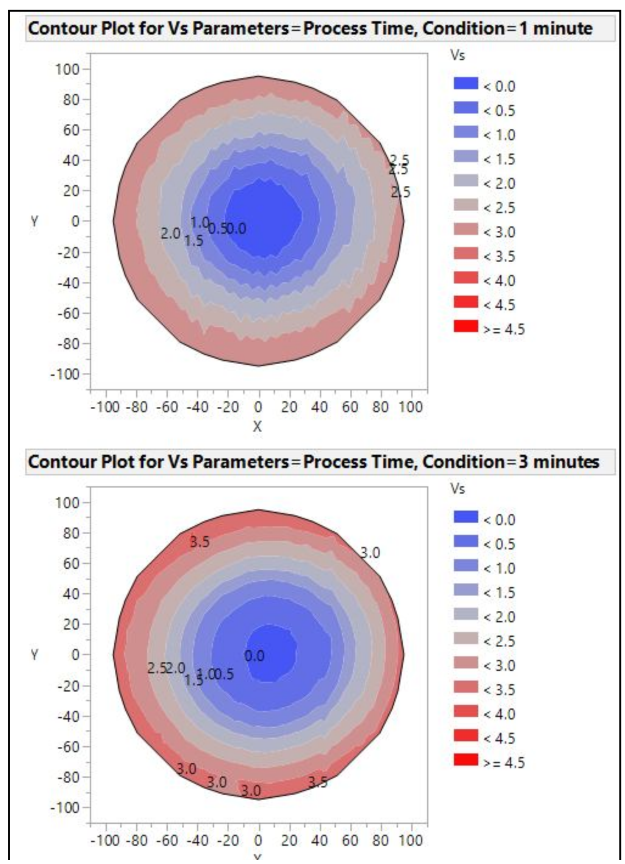
3.1 HRP Asher Model

Data collection is done by varying one parameter and maintaining the remaining parameters, as shown in Table 1.

Table 1: Conditions of Parameters

Parameters	Condition 1	Condition 2	Condition 3
Time (min)	1	3	5
Pressure (Torr)	1.0	1.5	2.0
Gas Flow (sccm)	2500	3500	4500
Power (W)	2100	2500	2900
Temperature (°C)	220	250	280

3.2 Time



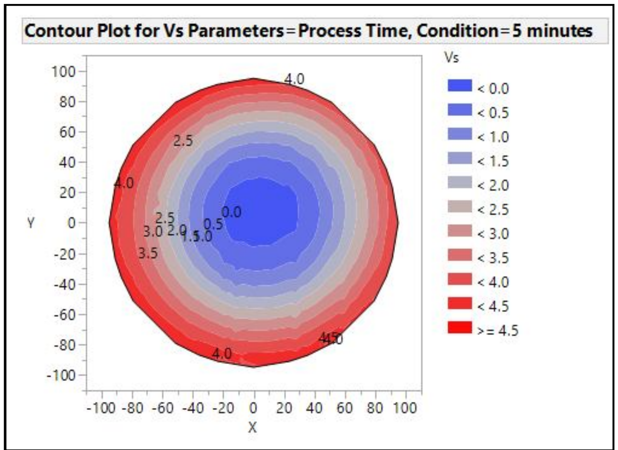


Figure 5: HRP - Process Time Vs (V) Contour Plot

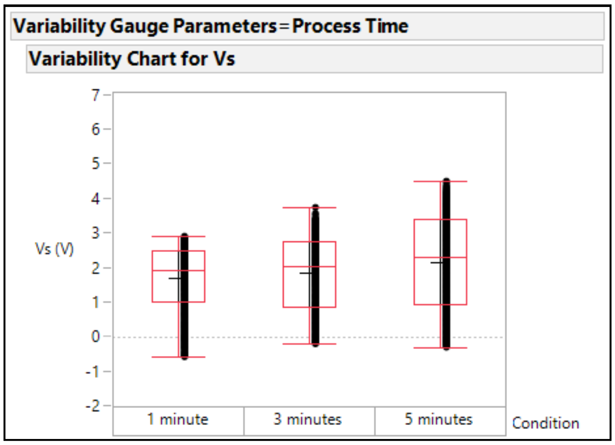


Figure 6: HRP - Process Time Vs (V) Variability Chart

Table 2: HRP - Process Time Condition Vs (V) Parameter Units

Processing Condition	Mean (V)	Std Dev (V)	Min (V)	Max (V)
Time – 1 minute	1.713	0.953	-0.563	2.924
Time – 3 minutes	1.851	1.058	-0.189	3.760
Time – 5 minutes	2.190	1.374	-0.285	4.517

The data collected for the above stated conditions suggest that with increase in time, we do observe an increase in the surface charges on the wafer surface, based on the Vs mean value. At the 5 minutes condition, we observed surface charges to be non-uniform. With the Vs standard deviation at about 1.374 and difference between the minimum and maximum at about 4.7V, this potential difference on the wafer surface can cause current to travel, thus shorting the device at a specific location. For this parameter, we see that longer processing time impacted on the total surface charge collection and non-uniformity of the surface charges on the wafer surface because the wafer is subjected to the plasma environment for a longer period of time. In the industry, longer processing time is applicable for higher photoresist thickness.

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3.3 Pressure

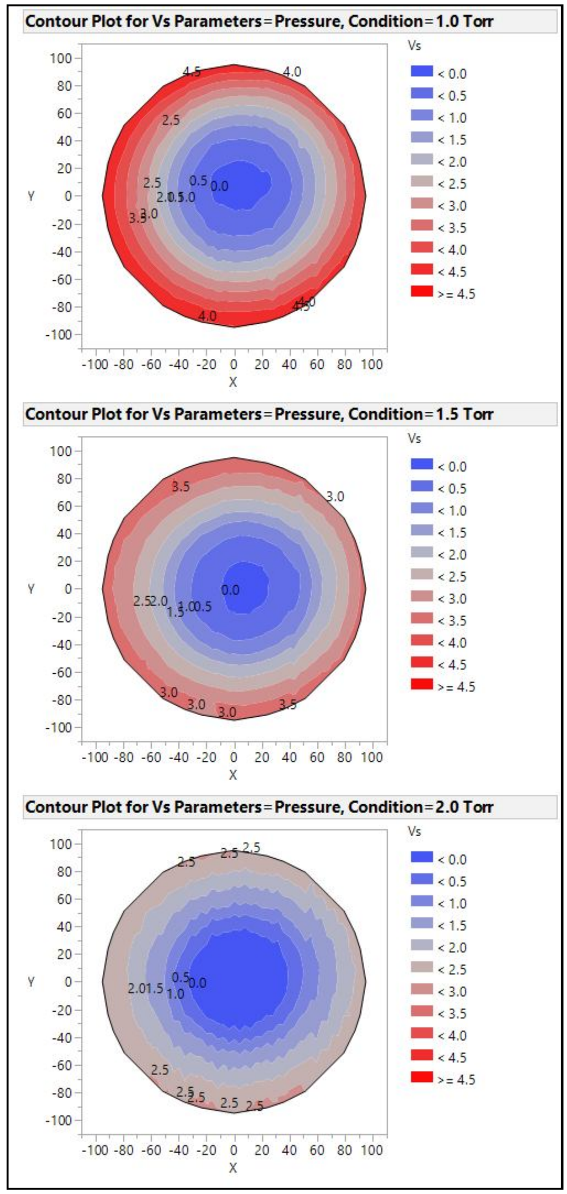


Figure 7: HRP - Pressure Vs (V) Contour Plot

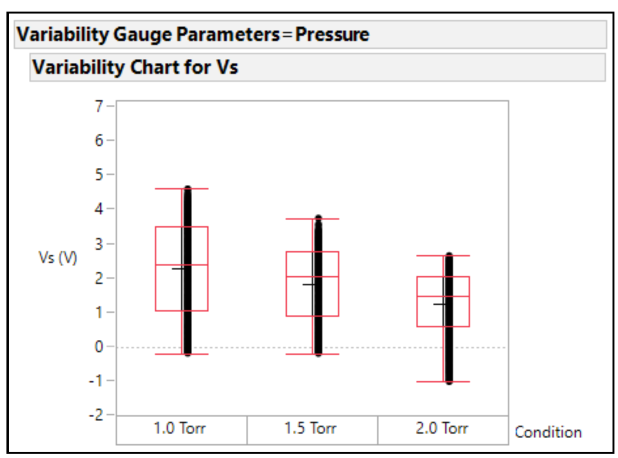


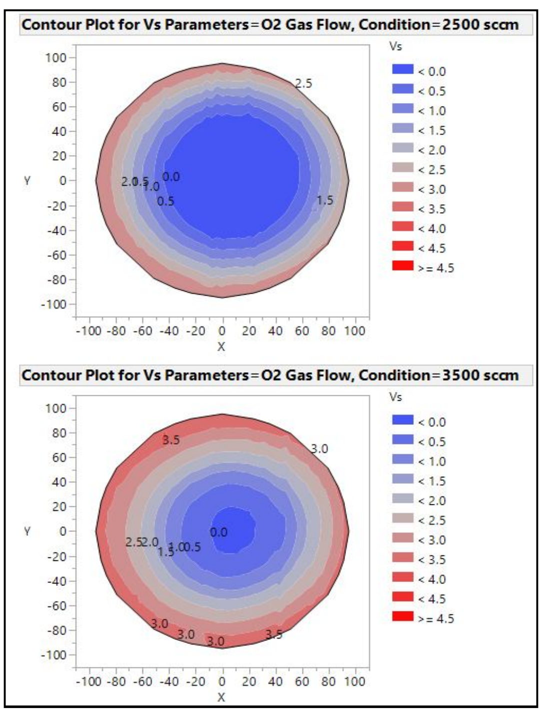
Figure 8: HRP - Pressure Vs (V) Variability Chart

Table 3: HRP - Pressure Condition Vs (V) Parameter Units

Processing Condition	Mean (V)	Std Dev (V)	Min (V)	Max (V)
Pressure – 1.0 Torr	2.290	1.374	-0.185	4.617
Pressure – 1.5 Torr	1.851	1.058	-0.189	3.760
Pressure – 2.0 Torr	1.266	0.957	-1.013	2.668

The data collected for these conditions suggest that with increase in pressure, we do observe a decrease in surface charges on the wafer surface, based on the Vs mean value. This is due to the scattering of the ions for ashing process at higher pressure. This can be viewed on the contour map for the pressure condition at 2.0 Torr, as depicted in Figure 7. It illustrates the scattering of the ion bombardment on the wafer surface, causing a non-smooth contour for various regions. For this parameter, we see that lower pressure impacted the total surface charge collection because of higher ashing rate condition at a lower pressure environment, as observed for a pressure condition of 1.0 Torr. The Vs standard deviation for a pressure of 1.0 Torr is about 1.374, suggesting lower pressure causes more interactions of ions on the surface but in a non-uniform manner, which increases the risk of PID. The usage of the higher pressure condition can reduce the PID concern but it will impact the overall processing time due to its lower ashing rate, thus increasing the concern of PID for longer time process with a non-uniform ion bombardment on the wafer surface.

3.4 Gas Flow



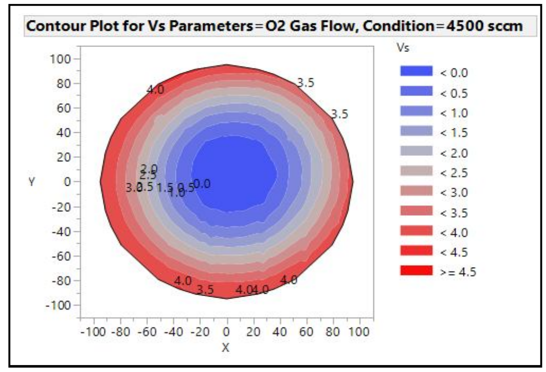


Figure 9: HRP - O_2 Gas Flow Vs (V) Contour Plot

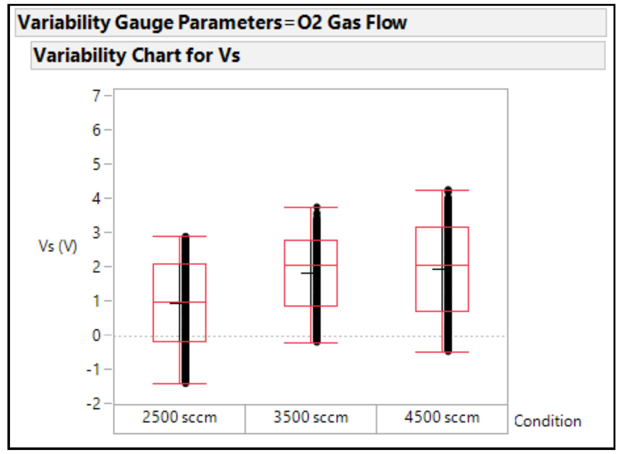


Figure 10: HRP - O_2 Gas Flow Vs (V) Variability Chart

Table 4: HRP - O2 Gas Flow Vs (V) Parameter Units

Processing Condition	Mean (V)	Std Dev (V)	Min (V)	Max (V)
O2 Gas Flow – 2500 sccm	0.941	1.277	-1.395	2.907
O2 Gas Flow – 3500 sccm	1.851	1.058	-0.189	3.760
O2 Gas Flow – 4500 sccm	1.941	1.374	-0.459	4.267

Based on the data in the tabular column above, the surface charges on the wafer surface, based on the Vs mean value is lower for the 2500 sccm O2 gas flow condition. This is due to the lack of ions to interact with the surface, thus impacting the standard deviation value. Meanwhile for the 4500 sccm O2 gas flow condition, higher surface charge is seen due to abundant ions present in the plasma and its interaction with the wafer surface. This also impacts the standard deviation value as more ions present in the plasma (in a controlled volume) will collide with each other, thus more unpredicted bombardment will occur on the wafer surface at many regions of the wafer, causing more potential difference at different locations on the wafer. Based on this, we observe that the 3500 sccm O2 gas flow has better uniformity compared to the remaining two conditions. Although the 2500 sccm O2 gas flow surface charges is lower than the other conditions, the actual processing condition will be impacted since lower ions result in a lower ashing rate and there will be a need to increase the process timing, which will have adverse effects on charge collection on the wafer surface.

3.5 Power

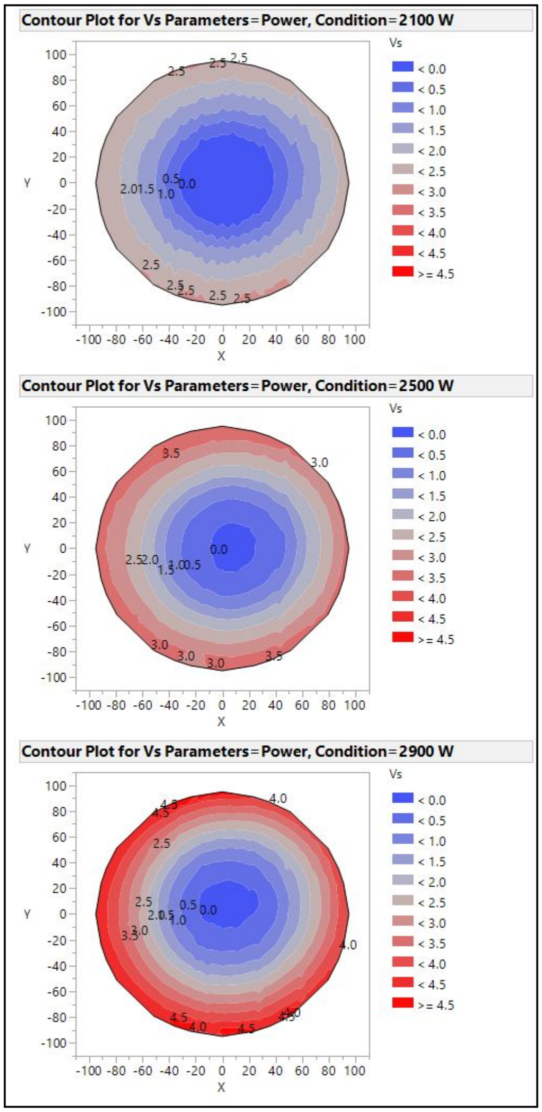


Figure 11: HRP - Power Vs (V) Contour Plot

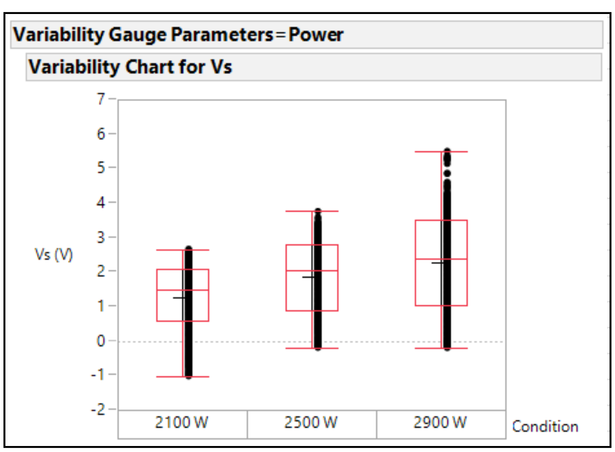


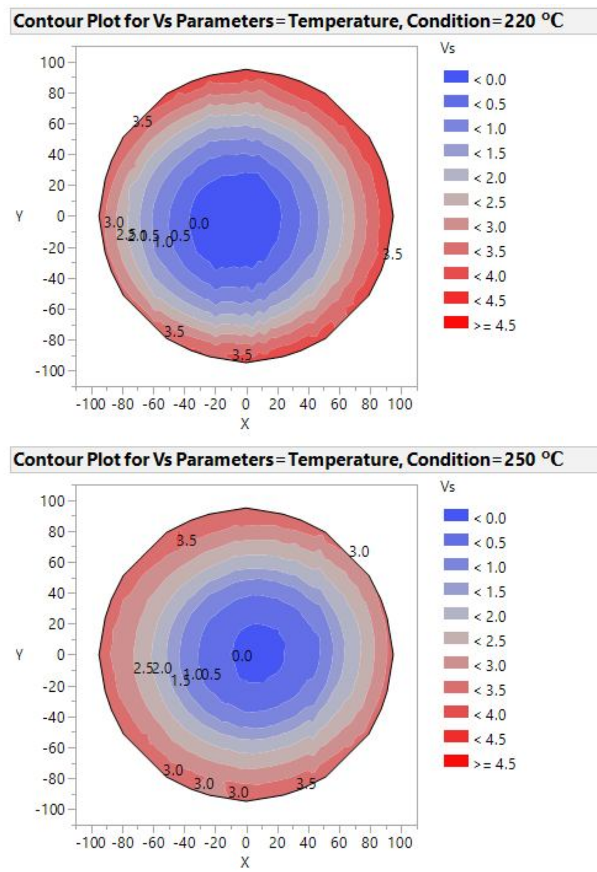
Figure 12: HRP - Power Vs (V) Variability Chart

Table 5: HRP - Power Vs (V) Parameter Units

Processing Condition	Mean (V)	Std Dev (V)	Min (V)	Max (V)
Power – 2100 W	1.266	0.957	-1.013	2.668
Power – 2500 W	1.851	1.058	-0.189	3.760
Power – 2900 W	2.292	1.396	-0.195	5.502

Based on the data tabulated above, the surface charges on the wafer surface, based on the Vs mean value and the standard deviation increases with an increase in the power delivered to the processing condition. This is due to the energy carried by the ions and its bombardment on the wafer surface, which increases with the increase in power supplied. Based on this observation, lower power delivered will result in lower PID concern with lower charge collection and also with better uniformity.

3.6 Temperature



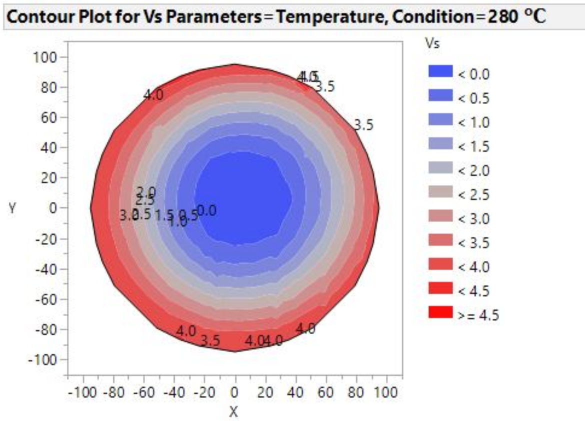


Figure 13: HRP - Temperature Vs (V) Contour Plot

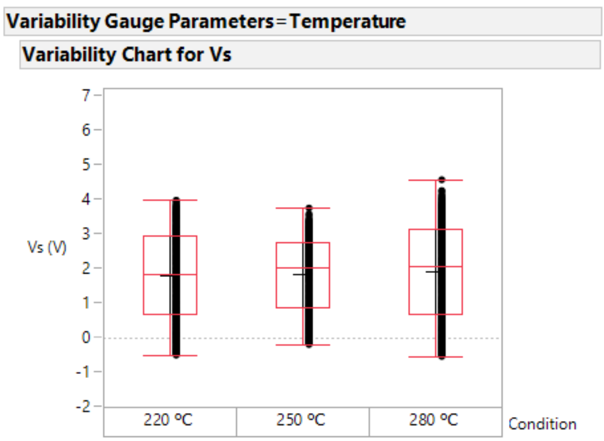


Figure 14: HRP - Temperature Vs (V) Variability Chart

Table 6: HRP - Temperature Vs (V) Parameter Units

Processing Condition	Mean (V)	Std Dev (V)	Min (V)	Max (V)
Temperature – 220 °C	1.793	1.281	-0.499	3.988
Temperature – 250 °C	1.851	1.058	-0.189	3.760
Temperature – 280 °C	1.941	1.376	-0.535	4.584

The surface charges on the wafer surface, based on the Vs mean value is increasing with an increase in the processing temperature. Based on the mechanism of the heater in the suspector, the increase in temperature increases the wafer temperature and chamber region near to it. This in turn increases the bombardment energy of the ion, but not to a very high extent, since the chamber temperature is fixed. The standard deviation of both the 220 °C and 280 °C temperature condition is higher, suggesting that the ion bombardment on the wafer surface is lowered for 220°C temperature and increased for 280°C temperature in a more scattered manner. As explained earlier, the increase in the temperature does increase the surface charges collection and is not a main contributor since the heater element is on the suspector and only heats the wafer, not the overall chamber. In the industry, this high temperature ashing is not preferred for post implant PRS due to resist popping concern [8].

3.7 Summary

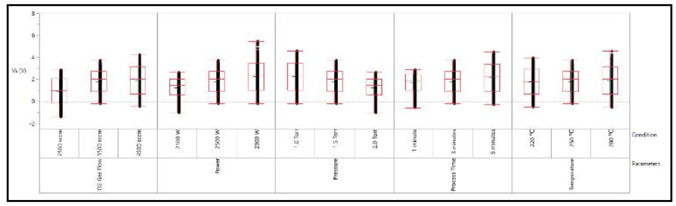


Figure 15: HRP - All Parameters Vs (V) Variability Chart

Table 7: HRP - All Processing Conditions Vs (V) Parameter Units

Processing Condition	Mean (V)	Std Dev (V)	Min (V)	Max (V)
Time – 1 minute	1.713	0.953	-0.563	2.924
Time – 3 minutes	1.851	1.058	-0.189	3.760
Time – 5 minutes	2.190	1.374	-0.285	4.517
Pressure – 1.0 Torr	2.290	1.374	-0.185	4.617
Pressure – 1.5 Torr	1.851	1.058	-0.189	3.760
Pressure – 2.0 Torr	1.266	0.957	-1.013	2.668
O2 Gas Flow – 2500 sccm	0.941	1.277	-1.395	2.907
O2 Gas Flow – 3500 sccm	1.851	1.058	-0.189	3.760
O2 Gas Flow – 4500 sccm	1.941	1.374	-0.459	4.267
Power – 2100 W	1.266	0.957	-1.013	2.668
Power – 2500 W	1.851	1.058	-0.189	3.760
Power – 2900 W	2.292	1.396	-0.195	5.502
Temperature – 220 °C	1.793	1.281	-0.499	3.988
Temperature – 250 °C	1.851	1.058	-0.189	3.760
Temperature – 280 °C	1.941	1.376	-0.535	4.584

In summary, the surface charges on the wafer surface, based on the Vs mean value emphasizes significant change in the overall mean value and also standard deviation values when the condition of the parameter is increased or decreased. The increase of the Vs and also the standard deviation indicates an increase in the PID concern since the total surface charges and non-uniformity is high.

4. CONCLUSION

In this study, the quantox wafers were used in order to collect the surface charges and it was measured using the Quantox tool, which utilizes the Kelvin probe method, to measure the surface charges which is depicted using the Vs mapping. Process time condition changes show that an increase in time increases the surface charges on the wafer surface, based on the Vs mean value. Its non-uniformity also increases due to prolonged wafer exposure in the plasma environment. For the pressure condition changes, we observed that with increase in pressure, we do observe a decrease in the surface charge collection on the wafer surface, due to the scattering of ions during the ashing process at higher pressure. Meanwhile for the lower pressure condition, it impacted on the total surface charge collection on the wafer surface because of higher ashing rate condition with lower pressure environment. This contributed to an increase of the standard deviation since more interaction of ions occur on the wafer surface. For the O_2 gas flow condition changes, it was observed that an increase in the gas flow impacted the charge collection since more ions were available for reaction. But, lower O_2 gas flow at 2500 sccm and higher O_2 gas flow at 4500 sccm affected the uniformity due to lack of ions and abundance of ions during the process respectively. Meanwhile for the power condition changes, we observed an increase in the charge collection and non-uniformity with an increase in power. This occurred as the energy driving the ions was elevated which in turn increased the frequency of the ion bombardment on the wafer surface, thereby increasing the surface charge collection on the wafer surface. As for the temperature, condition changes, based on the mechanism of the heater in the suspector, the increase in temperature increases the wafer temperature and chamber region near to it and this increased the bombardment energy of the ion but not to a very high extent, since the chamber temperature is fixed. Based on the data collected, we do observe that the surface charge collection increased with an increased processing temperature condition. Since the HRP asher model is a high power and high temperature asher model, the PID concern is higher compared to other asher model types.

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