ISSN 2278-3091
Volume 9 No.2, March -April 2020
International Journal of Advanced Trends in Computer Science and Engineering
Available Online at http://www.warse.org/IJATCSE/static/pdf/file/ijatcse52922020.pdf
https://doi.org/10.30534/ijatcse/2020/52922020

Performance of Gate Engineered Symmetric Double Gate MOS Devices and circuits for ultra-low power Analog and RF applications

N. Mohankumar[1]*, Girish Shankar Mishra[1], M. Arun Kumar[1], R. Poornachandran[2]
[1] Department of Electrical, Electronics & Communication Engineering, School of Technology, Gandhi Institute of Technology and Management (GITAM) – Bengaluru Campus, Bengaluru-561203, India
mohankumar.nagarajan@gitam.edu
[2] Research scholars, Anna University, Chennai-25

ABSTRACT

Double-Gate MOSFETs have become a potential candidate for future microelectronics industry due to its better control of the channel thus providing better immunity to short channel effects. A systematic investigation, with the help of extensive device simulations, considering the effects of Dual Material Gate (DMG) technology on the sub-threshold and superthreshold analog performance and Radio Frequency applications of symmetric double gate silicon-on-insulator (SOI) MOSFETs with gate lengths of 0.1 m is reported. The extensive device simulations reveal that the dual metal gate technology results in reduced drain induced barrier lowering and increased output resistance, thus illustrating the benefits of high-performance DMG SOI MOS devices over their single material gate (SMG) counterpart. Various RF figure of merits of the DMG devices such as the cut-off frequency, maximum frequency of oscillation and the gain bandwidth product are extracted and compared with the SMG devices to compare the relative performances. The circuit performance of a simple inverting amplifier with both DMG and SMG double gate devices is also studied by variation of the load resistance. It is concluded that the DMG devices exhibit better subthreshold analog performance and improved RF figure of merits compared to the SMG counterpart.

Key words: Carrier transport efficiency, Dual-material gate (DMG), Radio frequency (RF) applications, Silicon-on-insulator (SOI), Short Channel Effects (SCEs)

1. INTRODUCTION

As the end of the Semiconductor Industry Association (SIA) roadmap is being approached, the double gate devices are considered to be one of the most promising technologies for the future microelectronics industry due to its excellent immunity to short channel effects and higher drive on the current. Bulk CMOS devices were scaled beyond 100nm regime gives rise to short-channel effects, a major concern [1, 2]. The double gate or multi gate devices provide a better scalability option due to its excellent immunity to short-channel effects. Among the other advantages of DG MOSFETs are the near 60mV/dec subthreshold slope, low Drain-Induced-Barrier-Lowering (DIBL) and the possibility of using lightly doped or undoped body. Use of the undoped body also results in an enhanced mobility of the charge carriers and the elimination of statistical fluctuation of dopant concentration. Undoped DG MOSFETs provide the flexibility of using metal gates with near mid-gap work function to control the threshold voltage Vth [3-8]. Volume inversion is another important phenomenon that is observed in case of multi gate MOS devices where the inversion charges instead of being confined near the Si-SiO2 interface spread near the center of the channel and this is more evident in the subthreshold regime [8]. The charge carriers thus experience less interfaces scattering than that of a regular bulk MOSFET. This results in increased mobility and transconductance in double-gate devices than bulk CMOS transistors. Among the various types of DG MOSFETs, the FINFET structures are easier to fabricate compared to the planar structure.

The FINFET structure is most effective in the sense that the channel is wrapped by the gate from all the three sides, thus increases the effective gate control compared to the bulk CMOS devices [9-11]. The non-overlapped or underlapped FINFET devices have created lots of interest in this field due to the advantages of better control of SCEs via gate bias-dependent channel length and reduced gate-induced drain leakage (GIDL) and gate-source/drain tunneling [12, 13]. Most of the researches on the double gate devices carried out in the last few years mainly focused on the digital applications rather than the analog/RF applications. But the recent advancement of the IC industry evinced a lot of interest on the System on Chip (SOC) applications where the analog and the digital circuits are realized on the same chip. This results in an increased functionality and the reduction of the size and the cost. Along with the applications in logic designs, CMOS technology has also started dominating the RF market also which was previously dominated by BICMOS, BJT and the MESFET technologies [14-18]. Due to rigorous scaling advantages, CMOS has become a viable option for analog & RF applications and RF system-on-chip.

To improve the analog performance of DG MOSFETs and also to provide better immunity to SCEs, various approaches such as the channel engineering using halo implantation [19-22] and the gate work-function engineering [23-28] have been proposed. The dual-material gate (DMG) devices show great promise in this regard. Dual-material gate technology was proposed by Long et. al. way back in 1999 [23]. In this architecture, for an n-channel MOSFET, two different metals M1 and M2 with different work functions W1 and W2 respectively are selected as gate material such that W1>W2. These two metals are then aligned side by side to form the desired gate. This introduces a potential step along the channel. This step in the channel potential profile is responsible for the simultaneous suppression of SCEs and the transconductance improvement. The electric field and the electron velocity curve show an extra peak at the interface of the two metals in addition to that normally exist at the drain end. Thus, the dual metal gate technology results in increased carrier transport efficiency along the channel. This so-called gate work function engineering allows the use of lightly doped or nearly undoped body resulting in reduced mobility degradation effects in the channel and improved performance.

Very few reports of DMG devices such as subthreshold analog performance of bulk CMOS with DMG technology had been reported by Chakraborty et al [24]. With SOI technology rapidly emerging as technology for next generation VLSI, the effects of DMG technology on the submicron SOI devices has to be investigated. In the recent past, the market demand for energy constrained battery-operated devices has increased tremendously. Therefore, the design of devices and circuits for such ultra-low power applications is a challenging task. Analog circuits based on the subthreshold operations of the devices gained interest in this regard of having the higher gain in the subthreshold regime due to the exponential behavior of in this paper, a systematic investigation of the subthreshold analog performance and RF FOMs of a gate engineered (DMG) symmetric double gate devices is explored. Different analog parameters like the transconductance (g_m) and the transconductance generation factor for the DMG and the SMG n-channel devices are compared. Moreover to suit RF applications, various RF figure-of-merits such as the maximum oscillation frequency ($f_{\max}$), the cut-off frequency (f_t) and the gain bandwidth product (GBW) are studied for both the devices using extensive simulations. The circuit performance of a simple inverting amplifier for these devices is also explored as an application purpose.

2. DEVICE STRUCTURE AND SIMULATION PARAMETERS

The schematic cross-sectional view of an n-channel double gate MOSFET with dual material gate technology is shown in figure 1. Here the gate-source underlap structure is used to minimize the parasitic capacitance as well as to suppress the short channel effects [12, 13]. The technology parameters and the supply voltages used for device simulations are according to International Technology Roadmap for Semiconductors (ITRS) for 100nm gate length devices [32]. In both the DMG and the SMG n-channel devices, the threshold voltage (V_T) are maintained at a constant voltage of +0.355V with a drain to source voltage of 0.1V. The threshold voltage of the DMG device is adjusted by varying the work-function of metal gate M1 and metal gate M2 to achieve the desired values. Since for n-channel devices work-functions (W1>W2), we use 4.55 eV and 4.1 eV which roughly equals the work function of Copper and Alumunium. Several metal gate electrodes such as W/ TiN, Mo, Ta and TiN have been studied by researchers for better thermal and chemical stabilities [24]. The proportion of length of the two gate metals (L1 and L2) is kept equal for better performance [25]. The channel thickness is kept at 20nm while the front and the back-gate oxide thickness are fixed at 3nm. The body doping of both the DMG and the SMG devices is kept practically undoped (10^{15} /cc) to reduce the effect of mobility degradation by impurity scattering. The gate work function of the SMG device is fixed at 4.55 eV to maintain the same threshold voltage as that of the DMG FET.

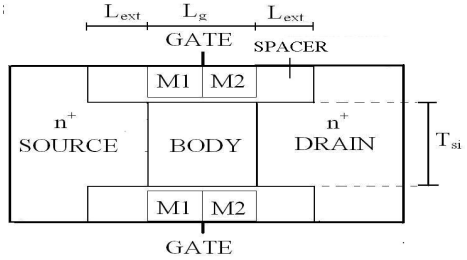

Figure 1: Cross sectional view of a DMG double gate n-channel MOSFET with gate source/drain underlap

Various process steps have been suggested to realize the dual metal gate technology. A novel Split-Gate MOSFET was reported in [27] with mono-nickel-silicide (NiSi) as a promising gate metal. Antimony implantation in the polysilicon gate prior to silicidation results in reduction of NiSi work function. By using proper masking technology, Antimony can be implanted to the NiSi gate close to the drain side thus forming high-low work function architecture. Another process step was reported in [28] where five additional steps are required prior to LDD formation. The metal with high work function can be deposited using the self-aligned asymmetric spacer process with a high degree of thickness control.

Nickel Silicidation for metal gate has become a motivating technology for FinFET devices as was reported by Kedzierski et. al. [11]. Metal gates provides the advantages of reduced poly-depletion effects, reduction of transverse

field as well as reduction of the gate leakage. In this technology, poly-Silicon gates are converted to NiSi by proper silicidation technique. Nickel provides the advantages of excellent compatibility with conventional fabrication steps along with near midgap work function and low stress of formation. Thus, it is proposed that integration of the process steps of [27] and [28] can successfully results in fabrication of a FinFET with Dual Metal Gate technology.

Sentaurus of ISE TCAD [32, 33] are used for 2-D device simulation. In our simulation, we have used the density gradient model which solves the quantum potential equations self-consistently with the Poisson and carrier continuity equations. The quantum potential is introduced to include quantization effects in a classical device simulation. In the density-gradient transport approximation, the quantum potential is a function of the carrier densities and their gradients. The analog /RF performance of both the devices is studied with the mixed-mode simulation with a highly précised RF extraction tool for calculating the RF figure-of merits. Benchmarking of the simulation results has been done with measurement data.

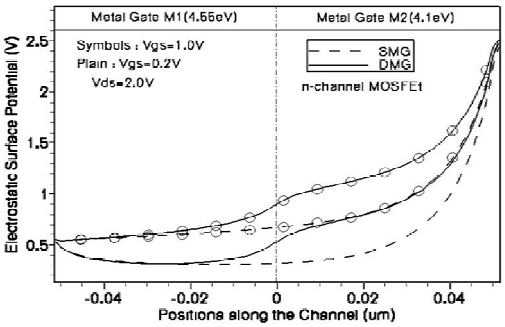

Figure 2: Comparison of electrostatic surface potential for gate to source voltage of V_{gs} = 0.2V and 1.0V and drain to source voltage of V_{ds} = 2.0 V in DMG and SMG double gate n-channel devices.

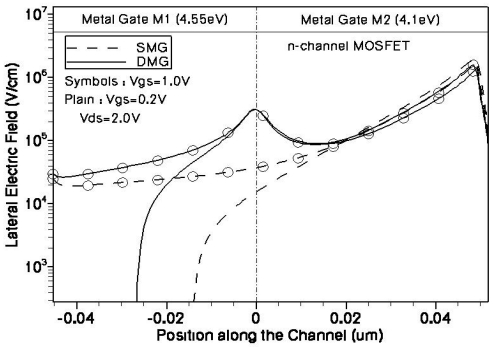

Figure 3: Comparison of lateral electric field for DMG and SMG double gate n-channel MOSFETs along the channel for gate to source voltage of V_{gs} = 0.2V and 1.0V and drain to source voltage of V_{ds} = 2.0V.

3. SIMULATION RESULTS AND DISCUSSION

The surface electrostatic potential of the n-channel DMG device is shown in figure 2 for the drain-to-source voltage of V_{ds} = 2.0 V and the gate-to-source voltage (V_{gs}) 0.2V and 1.0V. In this figure 2, the position along the channel is plotted in the X-axis direction where "0" indicates the center of the channel. At the interface of the two metals, a step rise of the potential occurs.

This is due to the fact that the region under metal M1 has a higher threshold voltage due to higher work-function of metal M1. So, the effective surface potential under metal gate M2 increases considerably due to its lower work-function [23]. The advantage of such a step rise in potential lies in the fact that the drain voltage variations or the drain fields are mostly screened by the higher potential under metal M2. This so-called screening of the region

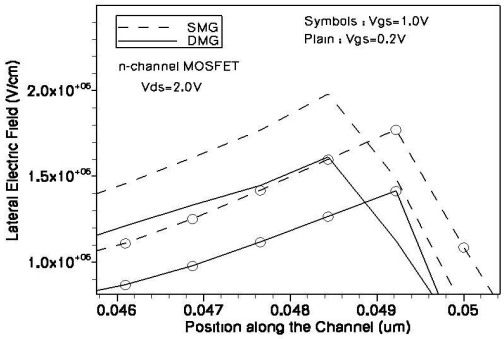

Figure 4: Comparison of lateral electric field for DMG and SMG double gate n-channel MOSFETs at the drain end for gate to source voltage of V_{gs} = 0.2V and 1.0V and drain to source voltage of V_{ds} = 2.0V.

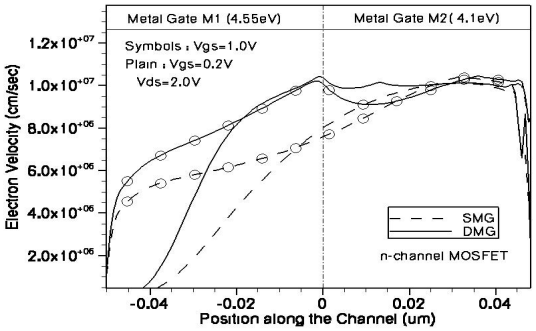

Figure 5: Comparison of electron velocity for DMG and SMG double gate n-channel MOSFETs along the channel for gate to source voltage of V_{gs} = 0.2V and 1.0V and drain to source voltage of V_{ds} = 2.0V.

under metal M1 by metal M2 is responsible for greater immunity to drain induced barrier lowering. The lateral electric field is shown in figure 3 and a detailed view of the pattern at the drain end of the channel is shown in figure 4

where it reveals that the peak electric field at the drain side in the n-channel DMG device is reduced considerably compared to that of the SMG device and there exists an additional small electric field peak at the interface of the two metals which causes the electron velocity to increase rapidly at the source side compared to that of the SMG n-channel MOSFET. Reduction of the drain electric field is obviously attributed to another cause of reduced DIBL and the hot carrier effects [24]. A closer look at the electric field distribution at the channel-drain junction is shown in figure 4 where the peak field is reduced nearly by 25% in case of the DMG device compared to the SMG DG MOSFET at V_{gs}=1.0V. The electron velocity is shown in figure 5 which exposes the fact that the carrier transport efficiency is greatly improved in the case of the DMG MOSFET. Due to the sudden increase of the electron velocity at the source side, the DMG MOSFETs are expected to show higher carrier transport efficiency than the SMG devices. As a result of this, the electron concentration in the channel

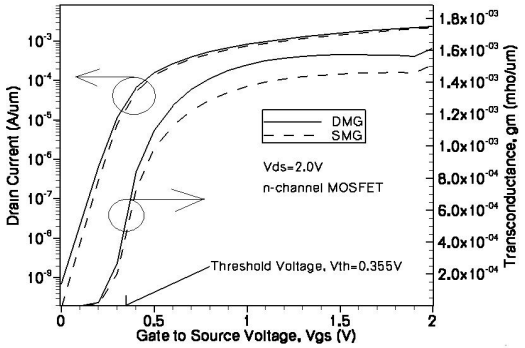

Figure 6: Comparison of drain current and transconductance in the DMG and the SMG double gate n-channel MOSFETs as a function of gate to source voltage V_{gs} for drain to source voltage of V_{ds} = 2.0V.

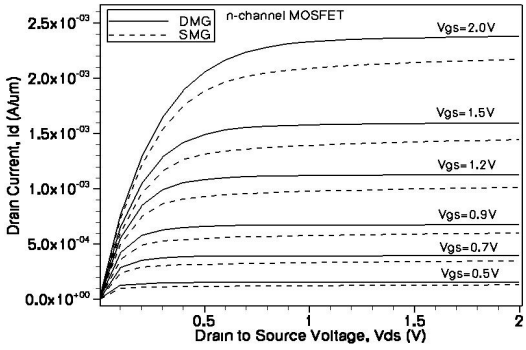

Figure 7: Comparison of drain current in the DMG and the SMG n-channel MOSFETs as a function of drain to source voltage V_{ds} for gate to source voltage of V_{gs} = 2.0V.

region is increased along with reduced DIBL and the hot carrier effects. Owing to lower effective threshold voltage under metal M2, the electron density increases in that region simultaneously increasing the drain current and the transconductance as explained in the next section. Thus, a DMG FET provides the advantages of reduced DIBL as well as increased transport efficiency.

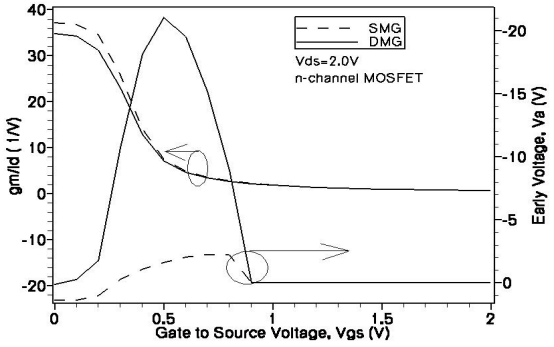

Figure 8: Comparison of transconductance generation factor and Early voltage for the SMG and the DMG n-channel MOSFETs as a function of gate to source voltage V_{gs} for drain to source voltage V_{ds} = 2.0V.

4. ANALOG AND RF PERFORMANCE

In this section, the different analog performance parameters for both the DMG and the SMG n-channel devices are studied. Figure 6 shows the variation of drain current I_d and the transconductance g_m with the gate to source voltage V_{gs} for a drain to source voltage V_{ds} = 2.0 V. It is evident from figure 6 that both I_d and g_m are higher in the DMG devices compared to the SMG devices.

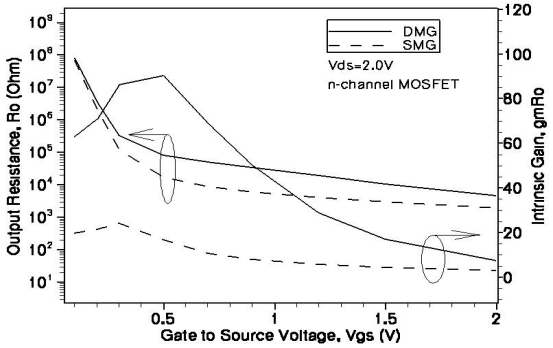

Figure 9: Comparison of output resistance Ro and intrinsic gain (gm Ro) for the SMG and the DMG n-channel MOSFETs as a function of gate to source voltage V_{gs} for drain to source voltage V_{ds} =2.0V.

The improvement is more visible in the subthreshold region compared to the strong inversion operation. The sudden increase of the electron velocity at the source side as explained earlier hold responsible for improvement in both I_d and g_m for such devices.

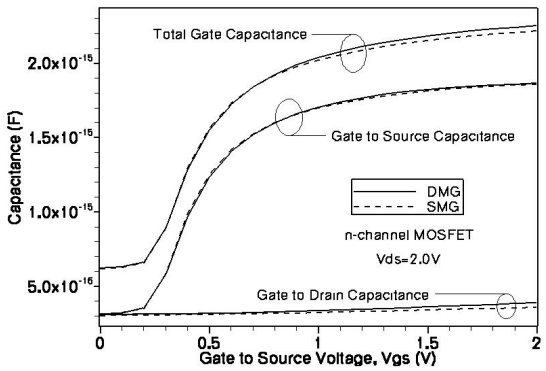

Figure 10: Comparison of different capacitance in the SMG and the DMG n-channel MOSFETs as a function of gate to source voltage V_{gs} at drain to source voltage of V_{ds} = 2.0V.

The drain current variation with the drain to source voltage V_{ds} for different gate to source voltages is shown in figure 7 where it is visible that the DMG devices exhibit higher current than the SMG device for the same gate to source voltage. The interesting feature about the I_d-V_{ds} curve lies in the fact that the drain current show more flatness at saturation for the DMG device compared to the SMG transistors. This reduced influence of the drain to source voltage on the drain current results in reduced depletion width in the drain-body junction thus increasing the output resistance.

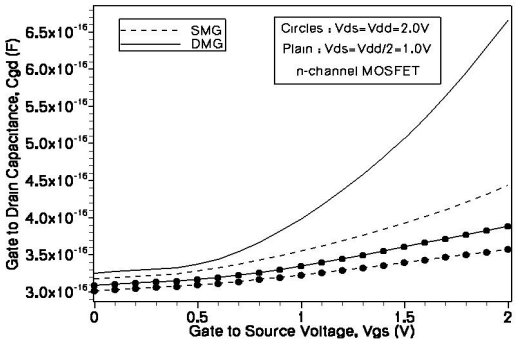

Figure 11: Comparison of gate to drain capacitance in the SMG and the DMG n-channel MOSFETs as a function of gate to source voltage V_{gs} at drain to source voltage of V_{ds} = 2.0V.

Another important parameter for judging analog performance is the transconductance generation factor (TGF) (g_m / I_d). This parameter is viewed as the available gain per unit power dissipation. As shown in figure 8, the TGF for the DMG devices is lower than the SMG devices in the subthreshold regime. This should not affect the performance much in the subthreshold regime, since the power dissipation is much less in that regime.

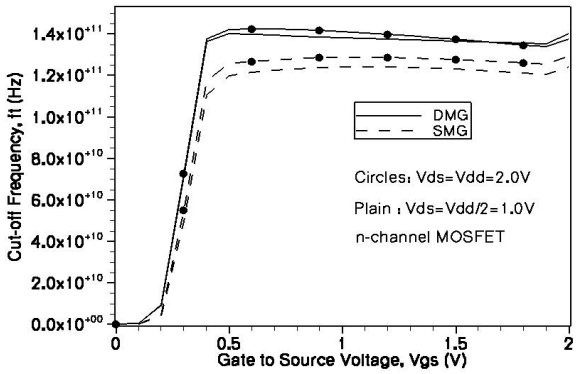

Figure 12: Comparison of cut-off frequency computed as a function of gate to source voltage V_{gs} for the SMG and the DMG n-channel MOSFETs at drain to source voltage of V_{ds} = 2.0V.

Above the threshold voltage, the difference between the two reduces distinctly. The early voltage variation is also shown in figure 8 where the DMG device exhibits comparatively higher early voltage than the SMG counterpart in the low gate voltage regime. The output resistance of a MOS transistor at any Vgs is evaluated as

$$R_o = V_a / I_d \qquad (1)$$

where V_a and I_d are early voltage and drain current at that particular V_{gs}. The Output resistance variation with the gate to source voltage is shown in figure 9 where the DMG devices demonstrate a considerable increase of R_o from the equation (1). The intrinsic gain which is product of transconductance and output impedance is also shown in the same figure. The DMG devices exhibit substantial increase of the gain in the low gate voltage regime. The DMG devices are thus expected to perform better in case of subthreshold analog applications

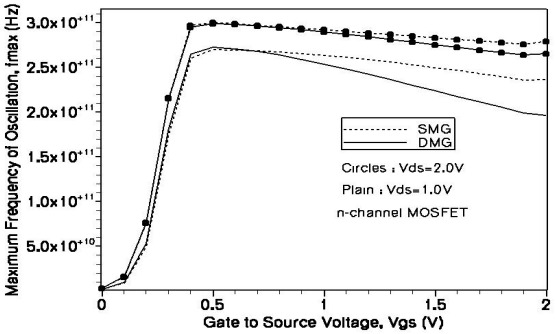

Figure 13: Comparison of maximum frequency of oscillation computed as a function of gate to source voltage V_{gs} for the SMG and the DMG devices at drain to source voltage of V_{ds} = 2.0V.

compared to the SMG devices. The circuit performance of n-channel DMG devices is studied and compared with its SMG counterpart. A simple inverting amplifier with different load resistance is simulated using both the DMG and the SMG device. The gain is calculated by taking the slope of the

input-output curve for an output voltage of $V_{DD}/2$. The gain of the inverting amplifier with the DMG devices increases by about 16% compared to that of the circuit with the SMG devices.

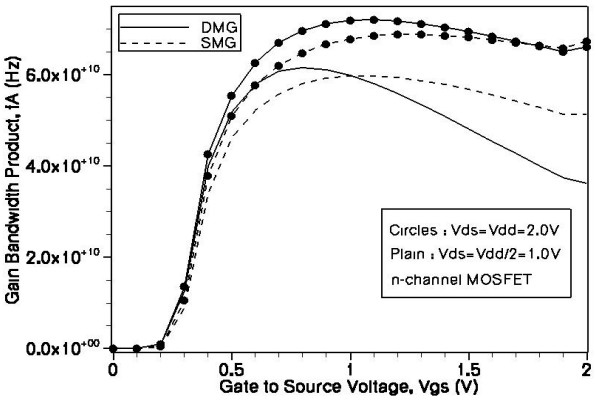

Figure 14: Comparison of the Gain Bandwidth Product for a dc gain of 10 computed for the SMG and the DMG n-channel MOSFETs at drain to source voltage of V_{ds} = 2.0V.

The RF performance trends of DMG devices will be studied in this section. The different RF figure-of-merits (FOM) such as the cutoff frequency (f_t) and the maximum oscillation frequency (f_{max}) are explored. Cut-off frequency is the frequency when the current gain is unity. Maximum oscillation frequency is the frequency when the power gain is unity and can be extracted by the Mason's gain formula. The approximate values of f_t and f_{max} are shown in equation (2) and (3)

$$f_t \cong \frac{g_m}{2\pi C_{gg}} \tag{2}$$

$$f_{max} \cong \frac{g_m}{2\pi C_{gs}\sqrt{4(R_s+R_i+R_g)(g_{ds}+g_m\frac{C_{gd}}{C_{gs}})}} \tag{3}$$

where C_{gs} and C_{gd} are the gate-to-source and the gate-to-drain capacitance respectively, and are the transconductance and the output conductance, C_{gg} is the total gate capacitance, R_g, R_s and R_i are the gate, source and channel resistance respectively. So, it is obvious that both the figure-of merits are greatly influenced by geometrical parameters. In the 2-D device simulator, ac analysis is performed over a frequency range and the Y parameters are computed. Then an advanced two port network RF extraction tool is used to generate the different RF-FOMs using the equations (2) and (3).

$$f_t = f_0 . |H_{21}| \tag{4}$$

$$f_{max} = f_0 \cdot \sqrt{\frac{|Y_{21}-Y_{12}|^2}{4[\mathrm{Re}(Y_{11})\mathrm{Re}(Y_{22})-\mathrm{Re}(Y_{12})\mathrm{Re}(Y_{21})]}} \tag{5}$$

The different capacitance variations are shown in figure 10 and 11. Due to the lower work function of the metal M2, the electron density is increased near the drain end in case of the DMG device. The gate to drain capacitance (C_{gd}) is slightly increased for DMG transistor compared to the SMG counterpart as shown in figure 11. The enhancement becomes prominent for low drain to source voltage of 1.0V. Due to the similarity of metal M1 of the DMG device and the gate metal of the SMG transistor, the gate to source capacitance (C_{gs}) is more or less same for both the devices under consideration. The total gate capacitance being the sum of C_{gs} and C_{gd} shows more or less equality with a slight increase in the strong inversion regime due to the effect of increased C_{gd}. So, the DMG devices with more or less gate equal capacitance and the increased transconductance provide an increased cut-off frequency. Figure 12 shows the cut-off frequency versus gate to source voltage V_{gs} that reveals the increased cut-off frequency of the DMG devices compared to the SMG devices. The maximum frequency of oscillation for the DMG and the SMG devices for different drain to source voltage is shown in figure 13. As seen from equation (5), the gate to drain capacitance plays a major role in determining f_{max}. Another important parameter is the gate resistance R_g. The use of metal gates results in reduced gate resistance. Owing to higher gate to drain capacitance at strong inversion, the maximum frequency of oscillation of the DMG devices is more or less equal to that of SMG devices with slight degradation at high gate voltages. Another important parameter for evaluating RF performance is the gain bandwidth product (GBW) for a certain dc gain (f_A). For a dc gain of ten, it is given by (6)

$$f_A \approx \frac{g_m}{2.\pi.10.C_{gd}} \tag{6}$$

The GBW for a dc gain of 10 is shown in figure 10(c). Due to slightly higher electron density at the drain side of the DMG devices, the gate to drain capacitance should be slightly higher. But the higher transconductance of the DMG devices results in an increased GBW as seen in figure 14. Finally, an inverting amplifier is simulated using varying load resistance with both the DMG and the SMG n-channel MOSFETs and the voltage gain is measured by calculating the slope of the input-output characteristics as shown in figure 15. An increase of around of 13% is observed in case of the DMG n-channel MOSFETs compared to the SMG counterpart.

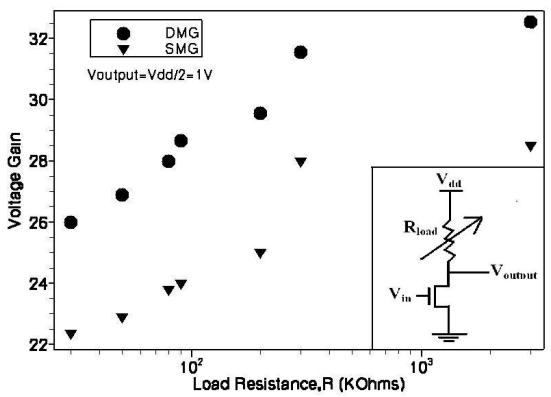

Figure 14: Comparison of voltage gain of a simple inverting amplifier with SMG and DMG n-channel MOSFETs as a function of the load resistance R_{Load} for an output voltage of V_{output}=VDD/2=1.0V

5. CONCLUSION

In this paper, we have explored the analog and RF performances of a symmetric Double Gate MOSFETs implemented with Dual Metal Gate technology both in the subthreshold and super-threshold regime of operation. The surface potential and the lateral electric field clearly reveal the fact that DMG devices are better immune to short channel effects specially to drain induced barrier lowering. Electron velocity curve explains the higher carrier transport efficiency of the DMG transistors. Various analog parameters like the drain current, the transconductance, the transconductance generation factor, early voltage and the output resistance of the DMG devices are studied and compared with the SMG counterpart. The circuit performance of a simple inverting amplifier with varying load resistance also proves that the DMG devices are superior to the SMG devices. The different RF FOMs also seems to improve for the DMG devices both in the super threshold as well as in the subthreshold regime. So, it is concluded that the Double Gate MOSFETs with the Dual Metal Gate technology will be very much favorable for future analog and RF applications as well as low power subthreshold analog circuits.

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