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High Speed High Capacity Memories for Secured Internet of Things based systems

K. Mariya Priyadarshini, R. S. Ernest Ravindran , B Manideep, B Deepak, K PavanSai
Koneru Lakshmaiah Education Foundation, Vaddeswaram Andhra Pradesh, India

Abstract: The Internet of Things (IoT) is a network connecting objects ranging from remote sensors to smart devices and tablets. To support high speed and high caacity networking speed the database management system (DBMS). To meet the requirements of DBMS of IoT smart micro devices are in high demand to store and access the data. Dual Edge Triggering (DET) flip-flops stand out to be a unique solution overcoming the trade-offs between speed and power. This paper presents a 64-bit register to control the flow of data to enhance the communication between devices connected over IoT. Though the concept of DET is subsisting, the design of area power and delay flip-flops efficient is still under design process. In this paper two new D-type flip-flops with Dual Edge Triggering are proposed. One among the two consists of 14 Transistors (14T) and the other consists of 12 Transistors (12T). The two designs are compared with existing 16 Transistor (16T) DET Flip-Flop. 14T DETFF (Dual Edge Triggered Flip-Flop) is found to be efficient in terms of area power and delay parameters. 12T DETFF shows really amazing and efficient results than 14T. Results are derived by simulating the circuits at 45nm technology at 1.2V supply voltage. It is observed that propagation delay of 14T is reduced by 45.39% when compared with 16T, for 12T it is reduced by 60.52% with respect to 16T. For 14T decrease in area is observed to be 18.42%, and 12T 36.16% of area is reduced when compared with 16T. Examinations of Dynamic Power scattering is finished with various capacitive loads, at various frequencies for multi bit registers extended up to 64-bits.

Key Words: IoT, DBMS, DET, Clock efficiency, Dynamic Power Dissipation, Leakage current.

1. INTRODUCTION

In the past years IoT technology is a standard methodology to device and run business applications. Massive data that gets generated by sensor nodes need to be picked up, incorporated and stored. Huge amount of DBMS is in demand to integrate this distributed data from multi sources [1-5]. AI (Artificial intelligence) and ML (Machine Learning) have their unique way in interacting with the things surrounding us. Our voice is the Speech processed and given as input voice command for few devices [6-9].Few electronic gadgets takes humans face as input to interact in a more intuitive manner [9-13]. As more and more devices with extending machine intelligence are connected over “Internet-of-Things” (IoT), “edge-computing” i.e. the computational weight of calculating on these edge devices vs. the “cloud” becomes progressively significant.

The Digital Signal Processors used for image and speech processing need to be precise and adequately fast to encode and decode the data. The processor efficiency strongly depends on two things 1) Adders and Multipliers 2) Memory Utilization [14-16]. In today’s DSP controlled processors utilized by AI, ML and IoT connected devices, demand for memory size is equally increasing along with computational complexity[17-19]. The current memory estimate is in products of Tera Bytes[20], so as to design such memories with less chip area two difficulties need to be confronted 1) To design memory cell with less number of transistors low leakage power dissipation as size of the transistors are scaling down. 2) Faster access to read and write the data into the memory [20-23]. In order to satisfy these two constraints many flip-flop circuits with implicit and explicit edge triggering flip-flops were proposed [6] .Implicit Data close to output Hybrid Latch Flip-Flop and Modified Hybrid Latch Flip-Flop are some of the techniques for implicit pulse triggered flip-flops. Explicit data close to output, Conditional Discharge Flip-flops, Explicit Modified Hybrid Latch flip-flops are few designs of Explicit Single Edge Triggered Flip-Flips [22-24]. All the previously mentioned flip-flops utilize either rising edge or falling edge of the clock leaving the other edge unused that decreases the proficiency of the clock consequently lessening the frequency [23, 24].

To increase the clock efficiency or to be clear to distribute the load on clock both at the rising and falling edges Dual Edge Triggering came into existence. This greatly increased the processor speed and lead to high frequency processor designs [24, 25]. The idea of DET is to give two ways from D to Q with the goal that read and write activities can be performed parallel. To be more clear at rising edge of the clock event one way writes the information to Q the other way reads the bit value and at falling edge the other way around occurs. Implementation of dual edge sensitivity using numerous modules including complementary latch pair and pulse-triggered latch, have been reviewed in [24].

Many techniques were proposed which make use of transmission gates and also n-mos pass transistors .Voltage scaling is one of the simple and common techniques that is in usage to maximize energy efficiency [25-29]. Quadratic decline in energy consumption can be attained by scaling down supply voltage. Therefore, voltage scaling is widely adopted between IoT applications where power consumption is major constraint [30]. and battery-operated miniature sensor. If one path latches the data the other path outputs the data to Q. the following figure:1 clearly shows two paths from D to Q. Q1 and Q2 are the two present states of the flip-flop and Q is the next state. At positive edge of Clk Q1=D and at negative edge of the Clk Q_2=D. This paper obviously clarifies the effectiveness of 14T, 12T and 16T flip-flops at higher order bits (5, 10, 15, 20, 32, 64-bits) in terms of area delay and power dissipation.

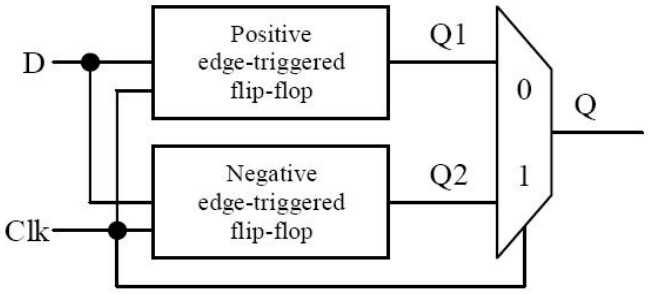

Figure1: Dual Edge Triggering for D-Flip-Flop [7]

2. EXISTING TECHNIQUES

In the first existing DET flip-flop (DETFF1) acts as a master slave flip-flop . This flip-flop consist of two data paths from D to Q, 4 transmission gates are used to give clock signal, 2 transmission gates in the upper data path closes the D to Q path when clock is high(read operation is performed) and the lower data path latch stores the bit value(write operation) and vice-versa. It consist of 20 transistors out of which 10 transistors form 2 latches remaining 10 transistors used for clocking. The only disadvantage in this technique is its transistor count when used for ultra large scale IC designs[29-31]. Because of increasingly number of switching transistors DETFF1 demonstrates progressively unique power scattering at higher frequencies despite the fact that it replaces ordinary master slave flip-flops [31]. To reduce the count of the transistors another DETFF2 is proposed. Among the two back to back connected inverters in DETFF1 one inverter is replaced by one P-mos transistor [32]. When bit '0' need to be stored p-mos is off and when bit '1' is stored p-mos is on. Source of p-mos is always connected to V_{dd}. Due to this transistor count reduces to 18. This further reduces area, dynamic power dissipation when compared to DETFF1. As the number of static devices reduces that optimizes the static power and leakage power dissipation.

the static output-controlled discharge flip-flop (SCDFF), the dual-edge triggered static pulsed flip-flop (DSPFF) [33], and the adaptive clocking dual-edge triggered sense amplifier flip-flop (ACSAFF) are few Dual Edge triggered flip-flops which act on the principle of Differential amplifier. In [34] a reversible Dual, Dual edge triggered (DET) flip flop is designed, here two D latches, namely positive edge triggered latch and negative edge triggered latch and a multiplexer are used. For designing the proposed reversible DET flip flop, reversible gates such as Fredkin gate and Feynman gate are used.

Transmission Gate based DETFF is proposed in [35] which uses 18 transistors. The concept of dual path is introduced in this paper to reduce the number of transistors which reduces switching activity. From the analysis with previous techniques like Conventional Dual Edge Triggered Flip-Flop (CDE-FF) [34-36] Asynchronous Set Reset D Flip- Flop (ASRD-FF)[36], 18T DETFF it is observed to have 27.22% decrease in power consumption for 50% switching activity factor (α) but delay increases up to 46.47%.

One more existing DETFF is 16T D-Flip-Flop [37-39], in these circuit two p-mos transistors forming the latch are removed and replaced with CMOS inverters. But the transmission gates used for clock signals are replaced by n-mos pass transistors as shown in the figure below. At positive edge of the clock data read operation will be performed by the bottom latch and the data path is open to input D, and the D value can be written at the upper latch and open to output Qn. When compared to DETFF1 AND DETFF2 16T DETFF shows optimized results. Number of transistor count is 16 which reduce the area of flip-flop and interconnections displayed in figure: 2.Dynamic power dissipation is also reduced as the number of switching transistors reduces by 2. D to Qn delay is also reduced as transmission gates are replaced by n-mos transistors. As more number of static inverters are used this may lead to leakage power dissipation. The proposed 12T DETFF reduces leakage power dissipation along with dynamic power dissipation.

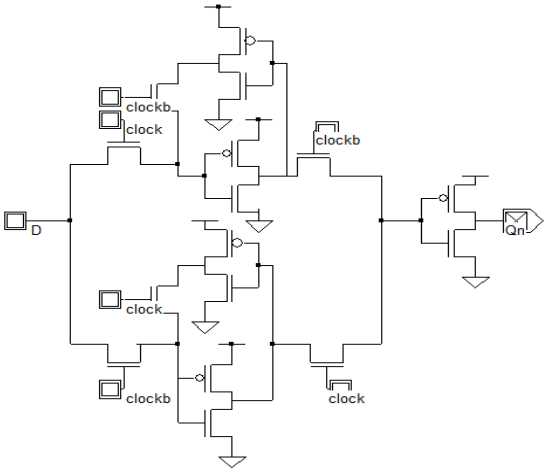

Figure 2: 16T Dual Edge Triggered Flip-Flop

3 Proposed DETFF's using 14 Transistors and 12 Transistors

3.1: 14T Dual Edge Triggered Flip-Flop: In this paper two different DETFF are proposed by modifying the 16T flip-flop, the two n-mos transistors connecting back to back inverters are removed. From the circuit it observed that, in the upper D to Qn path n-mos transistors switching for clkb used for the same read operation during positive edge, and bottom path clk signal switches n-mos connecting inverters for read operation. Since in a single way two transistors switch for similar edges of the clock for same activity n-mos transistors associating consecutive inverters are evacuated. This reduces the transistor count to 14T from 16T and the circuit diagram is shown in figure: 3.

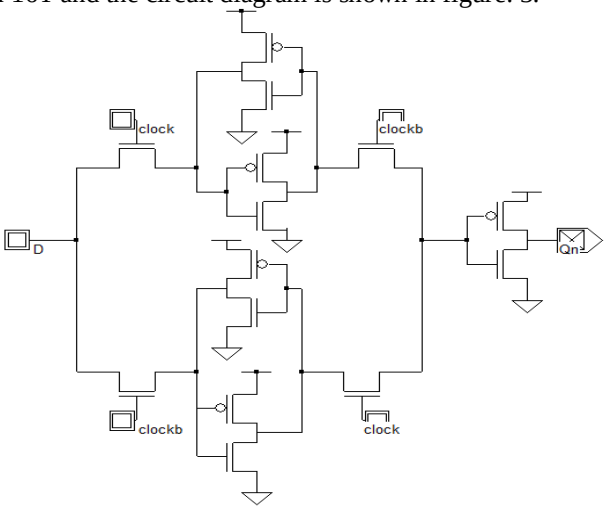

Figure 3: 14T Dual Edge Triggered Flip-Flop

3.2 12T Dual Edge Triggered Flip-Flop: This is a modified circuit of 14T DETFF. In this circuit the two latches (back to back connected inverters) are replaced by one p-mos transistor and CMOS inverter, the output of inverter is connected to gate of p-mos and input is connected to drain. The source terminal of p-mos is connected to VDD. By modifying the latch of flip-flop, transistor count has greatly diminished from 16T to just 12T and the circuit appears as below in figure: 4.

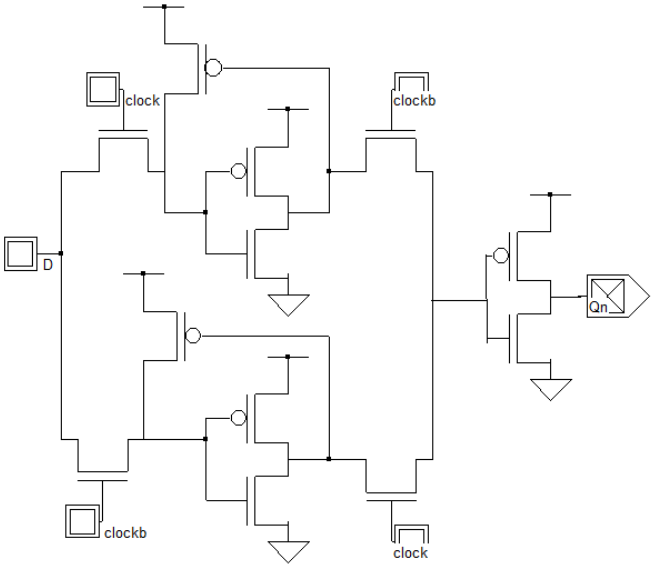

Figure 4: 12T Dual Edge Triggered Flip-Flop

The following figure: 5 and 6 shows the switch level model of 12T DETFF for reading and write operation of logic-1 at falling edge of clock. From the figure we can understand that in the upper data path data bit'1' is written into the latch and previously stored bit'1' in the bottom latch is read onto output Qn. Thus we can say that at one edge both read and write operation can be performed on a flip-flop.

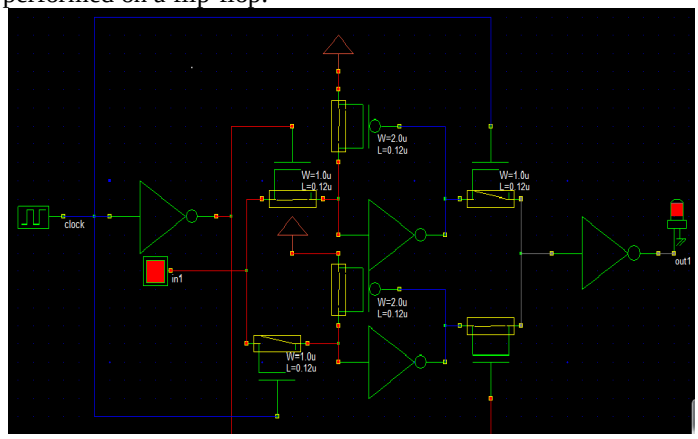

Figure 5: switch level model of 12T DETFF showing Read and write operation at falling edge of clock

Similarly at the rising edge of the clock read and write operation can be performed. At this edge the latch present in upper data path used for read operation and bottom data path latches the bit value.

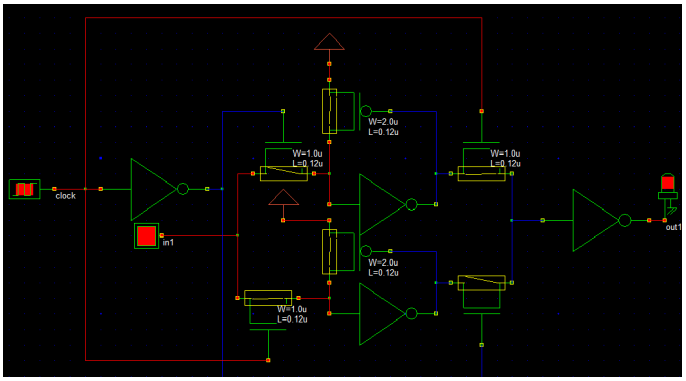

Figure 6: switch level model of 12T DETFF showing Read and write operation at rising edge of clock

4 RESULTS and DISCUSSIONS

The proposed 14T, 12T DETFF's are simulated and analyzed using 45nm Predictive Technology Model (PTM). The results are estimated with that of current 16T DETFF in terms of area power and delay. Comparisons are made for set-up and hold time values for proposed and existing FF's. The numerical values are calculated based the relational equations shown below.

$$T_{ckq} + T_c + T_s \leq T_{ck} + T_{sk} \qquad (1)$$

Where T_{ckq} is clock to q delay of flip-flop, T_c is propagation delay of data input to be received, T_s is the set-up time of output q, T_{ck} is the clock period and T_{sk} is the clock skew. The hold time (T_{hold}) mathematical relation between clock and output Q is given by.

$$T_{ckq} + T_c \geq T_{hold} + T_s \qquad (2)$$

The following table: 1 shows set-up time and hold-time comparison of 16T,14T and 12T DETFF, from the table: 1 it is observed that when compared to 16T, 14T DETFF shows less propagation delay, but the 12T DETFF demonstrates a more noteworthy decrease in rise time and fall time. It is seen that hold time is more prominent than set-up time since flip-flops utilize increasingly number of n-mos transistors which add to fall time delay.

Table 1: Setup time and Hold time delay comparison of existing and proposed techniques

Types of DETFF	Setup Time (ps)	Hold Time (ps)
16T (existing technique)	87	65
14T (Proposed Technique)	25	58
12T (Proposed Technique)	19	39

The following waveforms in Fig: 7, 8, 9 show the output waveforms of 16T, 14T and 12T Flip-Flops.

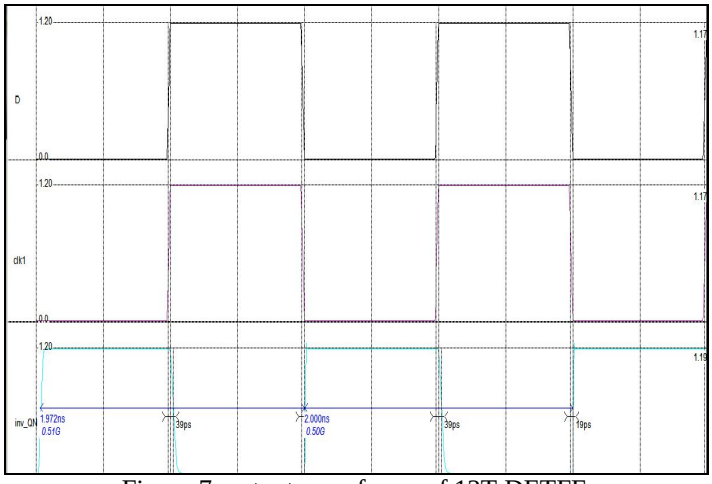

Figure 7: output waveforms of 12T DETFF

From the above waveform we observe that Qn the output changes at both rising and falling edge of the clock. Output fall time is 39ps and rise time is 19ps.

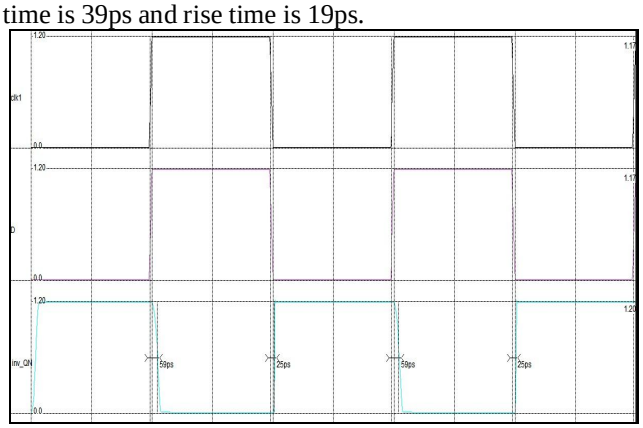

Figure 8: output waveforms of 14T DETFF

Figure 8 shows both at rising edge and falling edge of the clock output inv_QN follows input but with one pulse delay.

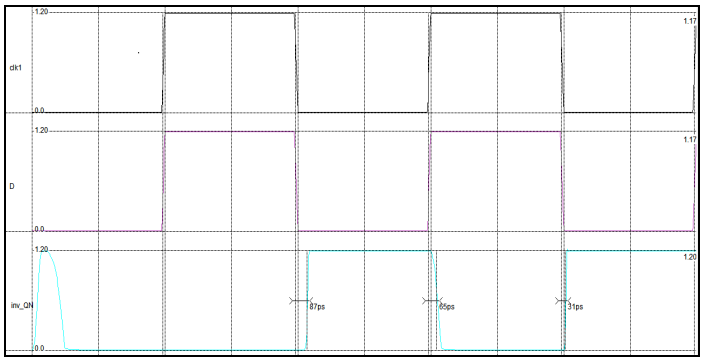

Figure 9: output waveforms of 16T DETFF

In Figure 9 even though data read and write operation is done at both rising and falling edge a spike is observed at the output. The rise time and fall time delays are tabulated in table:1. Table: 2 shows layout width and height comparison of existing and proposed DETFF's. The following values are calculated by generating layouts using 120nm technology, from the following table we observe that dimensions of the 14T and 12T DETFF are less compared with existing 16T DETFF. Layouts for 5-bit, 10-bit, 15-bit, 20-bit, 32-bit and 64-bit DETFF utilizing three flip-flops are created and width and length esteems are determined for area examination. The values shown below conclude that area occupied by 12T DETFF is much less than 16T and 14T.

Table 2: Post Layout Area comparison of multi bit Registers of existing and proposed techniques

Types of registers	16T DETFF		14T DETFF		12T DETFF	
	Width (µm)	Height (µm)	Width (µm)	Height (µm)	Width (µm)	Height (µm)
1-bit	16	14	13	14	11	13
5-bits	71	14	64	14	51	13
10-bits	145	9	116	9	107	8
15-bits	217	9	174	9	141	9
20-bits	290	9	231	9	163	8
32-bits	583	14	463	14	371	13
64-bits	923	14	739	14	923	8

For the same multi bit registers dynamic power dissipation is calculated and the graph is shown below.

Area comparison is done at the post layout simulation level of proposed D Flip-flops with existing 16T. For 14T 64-bit register layout area is reduced by 19.93% when compared with 16T, where as for 12T layout area is reduced by 42.85%. On an average the layout area among all multi bit register is reduced to 19% by 14T and by 12T area is reduced to 37.5%. It is completely clear that 12T is progressively proficient when compared with that of 14T and 16T flip-flops in terms of area.

Power delay product versus frequency examination is done at various frequencies so as to dissect the execution of flip-flops. Frequency values are varied from 500MHz to 4GHz for the sake of analysis.

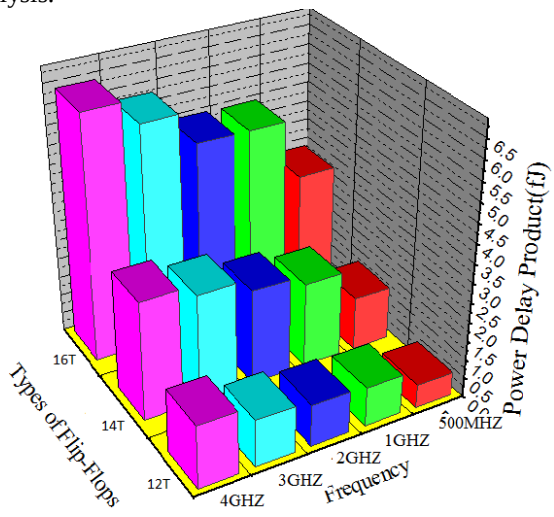

Figure 10: Power Delay Product (PDP) Comparison at Different Frequencies

In figure:10 3-Dimensional Analysis of Power Delay Product(PDP) is done at 45nm technology at post layout simulation. It is observed that PDP for 14T DETFF is less when compared with 16T DETFF, and is much less in 12T DETFF. For 16T DETFF the difference between maximum (at 500MHZ) PDP and minimum (4GHZ) PDP is 3.02fJ, for 14T it is 1.697fJ and for 10T it is 1.02fJ. The delta variation in PDP is much better than 14T and 10T. Among 14T and 10T DETFF's show less variation of 0.6fJ. We conclude that in terms of energy efficiency of Flip-Flops 14T and 10T show good results.

The following Table:3 shows the evaluation of dynamic power dissipation for three kinds of flip-flops extended up to 32-bit and 64-bit data paths.

Table:3 Load Capacitance v/s Dynamic Power Dissipation(µWatts)

Load Capacitance v/s Dynamic Power Dissipation(µWatts)						
Load Capacitance	16T TFETFF		14T TFETFF		12T TFETFF	
	32-bits	64-bits	32-bits	64-bits	32-bits	64-bits
0fF	265.01	421.3	217.06	384.2	159.8	276.2
20fF	272.38	435.6	219.3	414.25	167.2	282.4
40fF	281.41	441.4	226.10	419.16	171.5	297.5
60fF	296.74	462.8	240.65	425.02	186.9	315.1
80fF	305.52	531.3	251.30	471.02	193.6	326.3
100fF	315.6	537.12	268.17	498.79	196.3	331.7

At no load i.e. at 0fF capacitance dynamic power dissipation for 14T 32-bit data path is reduced by 18.09% with full load (100fF) it is reduced by 15.02% when compared with that of 16T. In case of 12T 32-bit data path dynamic power is reduced by 39.70% and with full load (100fF) it is reduced to 37.8% when compared with that of 16T. Similarly for 14T 64-bit data path register for 14T dynamic power dissipation it is reduced by 8.8% at zero load and 8.9% at full load. For 12T 64-bit data path register dynamic power dissipation is reduced by 34.36% at zero load and 38.24%. From this it is perfectly clear that for multi-bit registers both 14T and 12T DETFF are productive than 16T yet 12T shows much better outcomes.

The following Table:4 shows leakage power dissipation after generating the Layout of each DFF, at various temperatures differing from -40 °C to 120 °C.

Table: 4 Temperature v/s Leakage Power Dissipation(nwatts)

Temperature(0C)	16T DETFF	14T DETFF	12T DETFF
-40	15.9	24.6	39.7
-20	17.1	25.9	40.6
0	19.3	26.1	41.6
20	22.4	26.9	42.3
40	24.6	27.4	43.1
60	25.1	27.6	45.9
80	27.3	28.5	47.8
100	30.8	29.4	52.4
120	33.6	31.9	55.2

The delta difference in leakage power dissipation from -40^0C for 16T is 17.7nW, for 14T it is 7.3 nW and 15.5 nW for 12T DETFF. It is seen that 14T and 12T shows less delta variation in leakage power when compared with 16T which is an advantage. But when compared with 12T individual values leakage power is greater than 16T. Coming to 12T the delta variation in leakage power is under 16T and above 14T.

IV CONCLUSION

This Paper explains a new dynamic 14T DETFF and 12T DETFF which are well suited for high performance microprocessors. With dual edge triggering the processor speed can be doubled for doing power inversion. The 64-bit 12T registers can be used by the DSP processors to increase the speed of pulse width modulation. Analysis in terms of propagation delay, layout area, dynamic power dissipation with respect to frequency and leakage power dissipation with respect to temperature are done. From all the above discussed results it can be concluded that 14T DETFF shows better performance in terms of delay area and dynamic power, but the leakage power variation is wider i.e. 16.52µW when compared to 16T. But 12T shows proficiency in all aspects of comparisons. Dynamic power dissipation and area wise comparison results are analyzed even at 5-bit, 10-bit, 15-bit, 20-bit, 32-bit and 64-bits data paths. The percentage reduction in area for 14T 64-bit is 19.93% and 49% for 12T with that of 16T. Thus we conclude that 12T DETFF is more reliable which increases memory yield of IC designs.

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