ISSN 2278-3091

International Journal of Advanced Trends in Computer Science and Engineering, Vol. 3 , No.1, Pages : 486– 489 (2014)

Special Issue of ICETETS 2014 - Held on 24-25 February, 2014 in Malla Reddy Institute of Engineering and Technology, Secunderabad– 14, AP, India

SIMULATION OF A LAG-LEAD COMPENSATOR WITH A FIRST ORDER PLUS AN INTEGRATOR PROCESS USING PSPICE

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Abstract—A compensator having the characteristics of lag-lead network is called lag-lead compensator. In lag-lead compensator is component in a control system that improves an undesirable frequency response in a feedback control system. It is a fundamental building block in classical theory. The frequency response of the control system or the root locus plot are traditionally used to tune the compensator in a lengthy procedure. A first order with an integrator process in a unity feedback loop of maximum overshoot and large settling time is controlled using a lag-lead compensator (through simulation). The lag-lead compensator is tuned by minimizing the sum of absolute error of the control system using PSPICE. The result was reducing the process oscillation and an settling time. The comparison showed that the present tuning technique is superior.

Keywords—Lead-lag compensator; PSPICE; First-order;

I. INTRODUCTION

Lag-lead compensator influence disciplines as varied as robotics, satellite control, automobile diagnostics, laser frequency stabilization and many more. Given the control plant ,desired specification can be achieved using compensator I,D,PI,PD and PID are optimizing controllers which are used to improve system parameter(such as reducing steady state error, reducing resonant peak , improving system response by reducing rise time).

Lag-lead compensators can improve the performance of linear control systems through the proper tuning of the compensator parameters. There are two schools in designing lag-lead compensators. One of them uses the frequency response specifications of the compensated control system. The other uses its time response specifications.

PSPICE was initially developed by MicroSim and is used in electronic design automation. It was the first version of UC Berkeley SPICE available on a PC, having been released in January 1984 to run on the original IBM PC.

It includes features such as analysis of a circuit with automatic optimization, encryption, a model editor, support for parameterized models, auto – convergence and checkpoint restart, several internal solvers, a magnetic part editor, and support for tabrizi core model for nonlinear cores.

II. DESIGN PROCEDURE

A. Compensator Structure

The basic lag-lead compensator consists of a gain, two poles, and two zeros, and from a transfer function standpoint is just the series combination of a lag compensator and a lead compensator. Based on the usual electronic implementation of those compensators [3], the specific structure of the lag-lead compensator is:

$G_{c\_lag\_lead(s)=}$

$$Kc.[1/\alpha_{d.}(s+z_{cd})/(s+p_{cd})].[1/\alpha_{g.}(S+Z_{cg})/(S+P_{cg})]$$

$$=K_c[(s/z_{cd}+1)/(s/p_{cd}+1)].[(S/Z_{cg}+1)/(S/P_{cg}+1)]$$

$$=K_c[(\Gamma_{ds}+1)/(\alpha_d\Gamma_{ds}S+1)].[(\Gamma_g S+1)/(\alpha_d\Gamma_{ds}S+1)]$$

With

$$Z_{cd}>0,\ P_{cd}>0,\ \alpha_{d} = Z_{cg}/P_{cg}<1,\ \Gamma_{d}=1/z_{cd}=1/\alpha_d p_{cd}$$

$$Z_{cg}>0,\ P_{cg}>0,\ \alpha_{g} = Z_{cg}/P_{cg}>1,\ \Gamma_{d}=1/z_{cg}=1/\alpha_g p_{cg}$$

The subscript d on the various variables indicates the lead compensator, and the subscript g indicates the lag compensator.

Figure 1 shows the Bode plots of magnitude and phase for a typical lag-lead compensator. The values in this example are $K_c = 1$, $p_{cg} = 0.032$, $z_{cg} = 0.2$, $z_{cd} = 0.8$, and $p_{cd} = 5$, so $\alpha_g = 0.2/0.032 = 6.25$ and $\alpha_d = 0.8/5 = 0.16$. Changing the gain merely moves the magnitude curve by $20*\log_{10}|K_c|$.The choice of $\alpha_d = 1/\alpha_g$ for these plots was made for convenience; it is not a requirement for the design procedure. Some textbooks present design procedures that require $\alpha_d = 1/\alpha_g$, but that will not be done in theses notes.

The major characteristics of the lag-lead compensator are the magnitude attenuation in the intermediate frequencies and the positive phase shift at slightly higher frequencies. The maximum positive phase shift occurs at the frequency $\omega = \omega_{max}$, which is the geometric mean of z_{cd} and p_{cd}. The minimum value in the magnitude curve occurs (at least approximately) at the frequency that is the geometric mean of z_{cg} and z_{cd}. The large negative phase shift that is seen at intermediate frequencies is undesired but unavoidable. Proper design of the compensator requires placing the compensator poles and zeros appropriately so that the benefits of the positive phase shift and the magnitude attenuation are obtained at the correct frequency, without the negative phase

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shift causing problems. The following paragraphs show how this can be accomplished.

B.OUTLINE PROCEDURE

The following steps outline the procedure that will be used to design the lag-lead compensator to satisfy steady-state error, phase margin, and gain crossover frequency specifications. If the specification is given in terms of the closed-loop bandwidth ω_B instead of the gain crossover frequency ω_x, the following rule of thumb can be used to produce a preliminary design:

$$\omega_B \approx 1.5\omega_x.$$

1) Determine if the System Type N needs to be increased in order to satisfy the steady-state error specification, and if necessary, augment the plant with the required number of poles at s = 0. Calculate K_c to satisfy the steady-state error.
2) Make the Bode plots of $G(s) = K_cG_p(s)/s^{(N_{req}-N_{sys})}$.
3) Design the lead portion of the lag-lead compensator:
a) Determine the amount of phase shift in G(jω) at the specified gain crossover frequency and calculate the uncompensated phase margin $PM_{uncompensated}$ (assuming that the specified gain crossover frequency defines the uncompensated phase margin);
b) calculate the values of φ_{max} and α_d that are required to raise the phase curve to the value needed to satisfy the phase margin specification;
c) using the value of α_d and the specified gain crossover frequency, compute the lead compensator's zero z_{cd} and pole p_{cd}.
4) Design the lag portion of the lag-lead compensator:

a) determine the magnitude of G(jω) at the specified gain crossover frequency;

b) determine the amount of shift to the magnitude curve at the specified gain crossover frequency that is caused by the lead compensator;

c) determine the amount of magnitude attenuation that is required to drop the combined (plant + lead compensator) magnitude down to 0 db, and compute the corresponding α_g.
d) using the value of α_g and the specified gain crossover frequency, compute the lag compensator's zero z_{cg} and pole p_{cg} .5) If necessary, choose appropriate resistor and capacitor values to implement the compensator design.

III. SIMULATION MODELS

<u>OPEN-LOOP ANALYSIS</u>

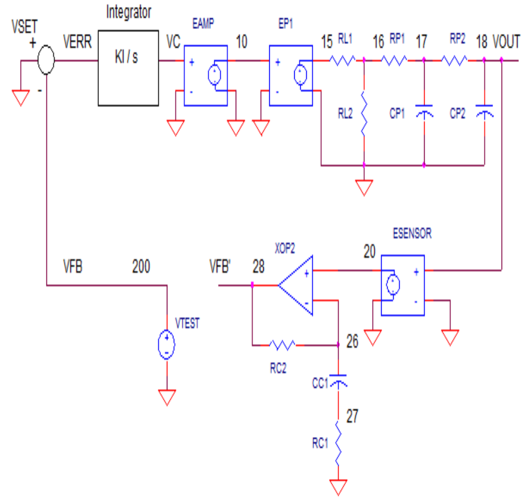

Fig:1 open loop analysis

Choose fz = fu = 10Hz

Choose RC2 = 100k

Calc CC1 = 1/(2·pi·CC1·fz) = 0.159 uF (round down to 0.1 uF, a realistic value.)

Calc fp = 10 · fz = 10Hz · 10 = 100Hz

Calc RC1 = RC2 / 10 which places fp about 10 times higher than fz.

<u>CLOSED-LOOP SPICE FILE</u>

```
OP_CTRL_LEAD.CIR

* SET POINT
VS       1        0        AC 1     PWL(0US 0V
0.01US -10V)
*
* CLASSIC CONTROL AMPLIFIER
R1       1        2        100K
R2       28       2        100K
CI       2        3        0.1UF
XOP1     0 2       3        op_001
*
* POWER AMP WITH LIMIT
EAMP     10       0        VALUE = {  LIMIT( 1
* V(3), +15, -15 )  }
*
* PROCESS (MOTOR, HEATER, ETC)
EP1      15       0        VALUE = { 100 *
V(10)  }
* LOSSES (FRICTION, HEAT LOSS, ETC.)
RL1      15       16       0.1
RL2      16       0        100
* DELAY (INERTIA, THERMAL MASS, ETC.)
RP1      16       17       100K
CP1      17       0        0.1UF
RP2      17       18       100K
```

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```
CP2     18      0       0.1UF
*
* SENSOR (TACHOMETER, THERMISTOR, ETC.)
ESENSE  20      0       VALUE = { 1/100 *
V(18)  }
*
* LEAD COMPENSATION
CC1     26      27      0.1PF
RC1     27      0       10K
RC2     26      28      100K
XOP2    20  26  28   op_001

*
 * BASIC OP AMP MODEL
* Device Pins      In+ In- Vout
.SUBCKT op_001    1    2    82
RIN   1   2   1e9
*   Aol=1000000, fu=1000000 Hz
G1   0    10  VALUE = { 1.0 * V(1,2)  }
R1   10   0   1e6
C1   10   0   1.59e-7
* OUTPUT STAGE
EOUT 80 0   10  0    1
ROUT 80     82    10
.ENDS
*
* ANALYSIS
*************************************
.TRAN   0.1MS  400MS
*.AC    DEC     20 0.1 1000MEG
.PROBE
.END
```

OPEN-LOOP SPICE FILE

```
OP_CTRL_LEAD_OL.CIR

*
* SET POINT
VS      100     0       AC 0
*
* INVERTER
EINV 1 0        100 0   -1
*
* OPEN-LOOP TEST VOLTAGE
VTEST   200     0       AC 1
*
* CLASSIC CONTROL AMPLIFIER
R1      1       2       100K
R2      200     2       100K
CI      2       3       0.1UF
XOP1    0 2      3       op_001
*
* POWER AMP WITH LIMIT
EAMP    10      0       VALUE = {  LIMIT( 1
* V(3), +15, -15 )  }
*
* PROCESS (MOTOR, HEATER, ETC)
EP1     15      0       VALUE = { 100 *
V(10)  }
* LOSSES (FRICTION, HEAT LOSS, ETC.)
RL1     15      16      0.1
RL2     16      0       100
* DELAY (INERTIA, THERMAL MASS, ETC.)
RP1     16      17      100K
CP1     17      0       0.1UF
RP2     17      18      100K
CP2     18      0       0.1UF
*
* SENSOR (TACHOMETER, THERMISTOR, ETC.)
ESENSE  20      0       VALUE = { 1/100 *
V(18)  }
*
* LEAD COMPENSATION
CCI     26      27      0.1PF
RC1     27      0       10K
RC2     26      28      100K
XOP2    20  26  28   op_001
*
*
*
 * BASIC OP AMP MODEL
* Device Pins      In+ In- Vout
.SUBCKT op_001    1    2    82
RIN   1   2   1e9
*   Aol=1000000, fu=1000000 Hz
G1   0    10  VALUE = { 1.0 * V(1,2)  }
R1   10   0   1e6
C1   10   0   1.59e-7
* OUTPUT STAGE
EOUT 80 0   10  0    1
ROUT 80     82    10
.ENDS
*
* ANALYSIS
*************************************
*.TRAN  0.1MS  1000MS
.AC DEC 20 0.01 1e5
.PROBE
.END
```

Iv.CONCLUSION

The lag-lead compensator in (32) is able to satisfy all three of the specifications imposed on the system given in (20). In addition to satisfying the phase margin, crossover frequency, and steady-state error specifications, the lag-lead compensator also produced a step response with a shorter settling time and less overshoot. In summary, lag-lead compensation can provide steady-state accuracy and necessary phase margin at a specified frequency when the Bode phase plot can be moved up the necessary amount at that frequency. The philosophy of the lag-lead compensator is to add positive phase shift at the specified gain crossover frequency to satisfy the phase margin

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specification and then to provide sufficient magnitude attenuation to satisfy the crossover frequency specification.

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