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DESIGN OF LOW POWER DIGITAL I/O CELL WITH ESD CIRCUIT PROTECTION

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Abstract— A novel low-power I/O cell is proposed in this work. The new input/output (I/O) cell is found to reduce the I/O power consumption, which has been considered as the major power dissipation of the whole chip. The maximum operating clock is 500 MHz given a 10-pF off chip load. Physical measurements of the proposed I/O cells show that the delays of the transmitter and the receiver are 2.7ns and 1.6 ns, respectively. The largest power/bandwidth of the proposed design is 38.9 W/MHz when transmitting. This work also facilitates ESD circuit that prevents the circuit from high voltage spikes.
Keywords- ESD protection, i/o cells,trnsmitter, receiver.

I. INTRODUCTION

In the digital transmission of chips through longs wires on the printed circuit board (PCB) is the input/output (I/O) cells which are responsible for voltage level shifting and electrostatic discharge (ESD) protection. Besides, long wires mean huge and loads to the I/O cells. The I/O cells, namely I/O pads, are asked to supply sufficient current to drive these large loads. Hence, not only is the pad area large, but also the power consumption occupied a great portion of the overall power. Most of prior CMOS I/O cells utilized very large area to accommodate large driving transistors as well as large passive elements. As the supply voltage of the chip is dropped, the switching speed of the I/O pads is reduced proportionally which in turn neutralize the high-speed performance of any CMOS digital core design. The output voltage swing in the transmitter of our new cell is reduced to about half of the supply voltage. In the mean time, the high-speed and high-throughput digital core design is not affected by using a feedback loop containing transistors with different threshold voltages. The power dissipation is also drastically reduced. The receiver of the proposed I/O cell, on the other way around, restores the signal level such that it can be faithfully decoded to be the original data. Neither reference bias nor passive element is required in the proposed design.

The I/O cell is typically called a “Standard I/O Cell” because of its common interface implementation and regular structure. The I/O cell provides the functional building blocks used for synthesis and a layout representation of the cells for place-and-route. This guarantees that a physical or layout representation of the cells exists when the design is implemented using place-and route tools. Standard Cell- Based Design refers to a design approach that uses a library of basic building blocks called standard cells. This flow requires an I/O cell of predefined logic circuits implementing a selected range of logic functions, characterized for power, area and timing.

[1] presents low-power and small-area digital I/O cell. The new input/output (I/O) cell drastically reduces the I/O power consumption, which has been considered as the major power dissipation of the whole chip. In [2] the authors have employed three circuit techniques to reduce the power and area of I/O circuits. Input multiplexed transmitter architecture with reduced voltage swing allows a small transmitter to be used while still providing most of the speed advantage of an output-multiplexed architecture. [4] Presents new CAD tools for CMOS I/O circuit design. To our knowledge, this is the first layout extractor developed for CMOS I/O circuit reliability. Unlike normal extractors, the circuit schematic is extracted based on the specified ESD conditions. In addition, parasitic BJTs are extracted for circuit simulation. J. G. Hansen [6] presents the design of cell library for minimal leakage currents. The advantages of having library are faster time-to-market and reuse of often complex logic functions. The design methodology and requirement has been described. It is obvious that a very careful procedure and format has to be followed in order to produce a good cell library for ASIC design. Asral [5], explains the standard cell design requirements, standard cell design and the characterization process. The characterization process in this paper is much easier then the complexed one or the industrial flow that was given in the above TSMC data book.

The paper is organized as follows. Section II deals with the back ground knowledge about input/output cell design.

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Section III presents the proposed methodology to reduce power dissipations at transmitter and receiver end of a digital I/O cell. Section IV is devoted to results and discussion and paper is concluded in section V.

II INPUT/OUTPUT CELL

A typical IO cell design in digital data transmission is shown in Figure1

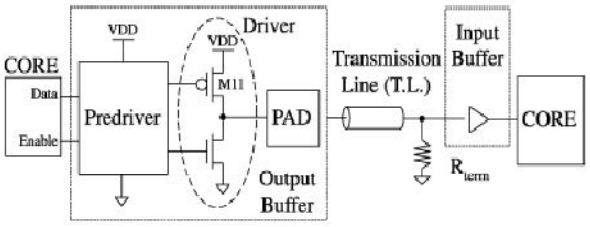

Fig.1.Basic I/O cell design.

The pre-driver, when enabled, supplies the gate drive to the driver composed of a pair of huge pMOS and nMOS transistors to steer a large current to or from the long wire. This traditional design cannot directly be voltage scaled so as to achieve the power saving by $P=f.C.V^2$, where f is the switching frequency, C is the load, and V is the supplied voltage. The reason is obvious: if the supplied voltage of the driver is shifted from VDD (supply voltage) to 1/2 VDD, the drain current of M11 becomes

$$I_D = \frac{\beta}{2}\left(V_{SG} + V_{thp}\right)^2\left[1+\lambda\left(V_{SF} - V_{SD,sat}\right)\right]$$

Where, V_{SG} is the voltage drop between the source and the gate of is M11; V_{SF} is that between the source and the drain of M11.The decrease of V_{SF} caused by the shrinkage of the supplied voltage results in the decrease of I_D. Thus, the driving capability as well as the speed is deteriorated. Adding a reference 1/2 VDD bias to the driver pair might be considered as a good idea. Regardless of using a band gap bias or a second voltage supply, the area penalty is highly unacceptable since the load is large. On top of this drawback, the reference 1/2 VDD bias usually has a poor driving capability which severely affects the supplied voltage of the driver pair. The consequence could be malfunction and large power dissipation [6]-[7].

III PROPOSED METHODOLOGY

a) ESD PROTECTION CIRCUIT:

ESD failure is one of the major IC reliability issue in the field. Most of the customer complaints in the field due to chip failures are due to ESD issues. This occurs when huge static charges gets induced into the chip through human body/machine/second IC, which results in failure of chip.ESD results in

- Dielectric Failure resulting in gate oxide breakdown when the gate of the input buffer is connected to the input pad [9].
- Thermal failure results in melting of the device [9].
- Latent failure which is a typical failure which increases leakage current/reduces gate oxide integrity without any change in functionality. This problem cannot be identified immediately.

These problems can be overcome by proper handling of IC's or by using packaged IC's or by introducing a ESD protection circuit to the IC pins which diverts huge voltages/high current from the internal circuitry thus protecting the IC.

This figure shows the Low voltage trigger ggNMOS circuit designed to clamp the high rise time ESD signal. Here the resistor and capacitor pair acts as high pass filter [2] to filter the signal of rise time more than 400pS. As we know the TR =2.2RC [8] Assume R=1K therefore C=18.18pF.

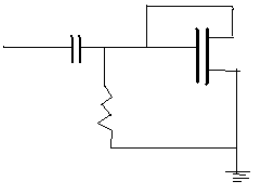

Fig.2.ESD circuit.

During the normal operation NMOS is in cut-off as the gate is connected to ground through 1K resistor. But the occurrence of ESD event will trigger the gate and make the transistor to conduct hence clamp the over voltage stress due to ESD event. The ESD current can go up to 1A the size NMOS is designed to sink this current. By using linear current equation of NMOS [Appendix] it was found that WN=180nm LN=180nm.

B) DESIGN OF TRANSMITTER AND RECEIVER:

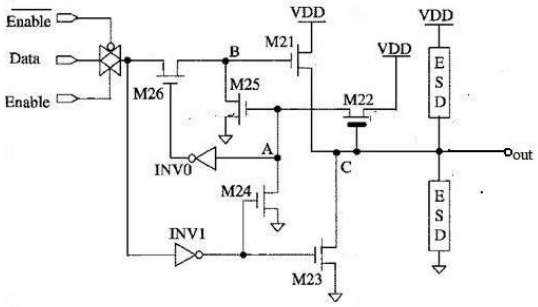

Fig.3. proposed methodology of transmitter design.

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Referring to Fig.3, which is the proposed transmitter, Data and Enable are signals generated by the digital core. ESD is the electrostatic discharging circuitry for the purpose of protection [11]–[13]. The model of the pad as well as the bonding wire and package is shown in Fig.3. The operation of the transmitter is described as follows.

T1) When Data is low and Enable is high, inverter INV1 turns on M23 and M24 which in turn pull down node C and A, respectively, to ground. Then, the low voltage at node A turns on M26 via INV0.

T2) As soon as Data turns high, a wide M26 turns on M21 right away. Node C, thus, will be charged to around 0.1V very shortly which turns on the zero- nMOS, M22. The voltage at node A then is boosted to VDD. Thus, M26 is off and M25 is turned on to ground node B which in turn shuts down M21. The charging operation to node C is then terminated. The final voltage level of node C after the mentioned procedure will be kept around. Since neither reference bias nor passive element is used in the design, the transmitter size is extremely small. Notably, in order to avoid the racing problem which might occur in the procedure of shutting down M21.We have to ensure that M26 is turned off before M25 is on. Otherwise, a large dc current will be induced. The design of inverter INV0 is different from the rest of the inverters. The pull down transistor in INV0 is a zero- nMOS, as shown in Fig. 4. The threshold voltage of the zero- nMOS, which provides a high sensitivity to the variation of the voltage at node A, is 0.2 V [14]. Hence, the gate drive at M26 will be discharged very quickly. The final voltage level at node C does not have to be very precisely a, which is the “high” of the output of the transmitter. It will drift due to the temperature, process variation, or loading. As long as the a logic “1” sent by the proposed transmitter is above 0.8 V for all process corners, it can be recovered correctly by the sophisticated receiver design which will be illustrated in the following section.

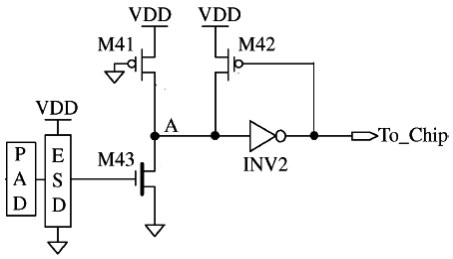

Fig.4. proposed methodology of receiver design.

The signal delivered by the transmitter will be contaminated seriously by the noise and crosstalk of the transmission lines. The quality of the signal present at the receiver is expected to be poor. Referring to Fig. 5, the received signal appears at the gate of M43 via pad and ESD circuitry. The threshold voltage of M43 is chosen to be a medium V. (Note: The medium- transistors are available in TSMC 0.25-m 1P5M process and better processes.) The function of the receiver is described as follows.

R1) When the gate drive of M43 is low to turn off M43, node A is charged to VDD. Hence, the To_Chip signal is low. The weak feedback latch composed of INV2 and M42 stabilizes the signal to the digital core.

R2) If the gate drive of M43 turns high, M43 will be turned on to discharge node A. To_Chip signal, thus, is pulled high. As long as the voltage of the gate drive of M43, which is the received signal via the pad and ESD, is higher than the pre-determined 0.4 V, the voltage level of the signal sent to the internal digital core can be restored to VDD.

IV RESULTS AND DISCUSSION

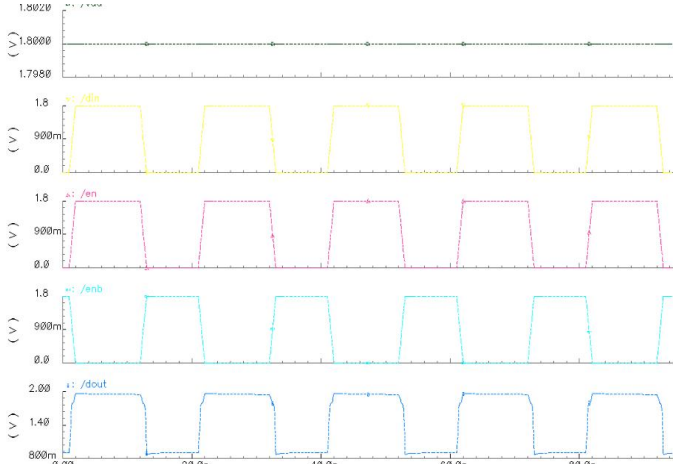

Fig.5. waveforms of transmitter design.

The proposed methodology implemented on 180nm technology with a Vdd of 1.8v and with enable(en), enable(enb), input(din) taken as 1.8v .Fig. shows the simulation results of transmitter it can be observed when enable is set to 1, enb is set to 0, input(din) set to 1 the output becomes high with voltage of 1.8v.

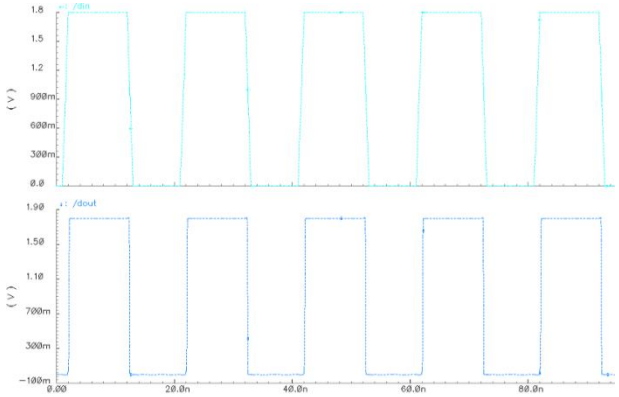

Fig.6. waveforms of receiver design.

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The proposed methodology implemented on 180nm technology with a Vdd of 1.8v and with input(dout) as 1.8v. Fig. shows the simulation results of receiver it can be observed when input (dout) set to 1 the output becomes high with voltage of 1.8v.

TABLE I

Features	Previous work	Transmitter	Receiver
Technology	CMOS 180nm	CMOS 180nm	CMOS 180nm
Power supply	1.8v	1.8v	1.8v
delay	10.8nsec	2.7nsec	1.6nsec
Power dissipation	60mw	282µW	120 µW

V CONCULSION

In this paper presented a novel design of digital input/output cell with ESD protection cell. The design presented satisfactory results regarding circuit safety without affecting the logic naturality. The present work reduces the power dissipation and propagation delay compared to the work with basic I/O cells.

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