ISSN 2278-3091

International Journal of Advanced Trends in Computer Science and Engineering, Vol. 3 , No.1, Pages : 90 – 94 (2014)
Special Issue of ICETETS 2014 - Held on 24-25 February, 2014 in Malla Reddy Institute of Engineering and Technology, Secunderabad– 14, AP, India

Reduction of Static Power Dissipation in Adiabatic Combinational Circuits Using Power Gating MTCMOS

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Abstract- **This paper proposes a method to reduce static power consumption in Adiabatic logic circuits based on Complementary Pass transistor Adiabatic Logic (CPAL) operated by two phase power clocks. We are applying power gating MTCMOS technique to reduce static power consumption in CPAL circuits. We tested MTCMOS power gating technique on 4-bit ripple carry adder to observe effect of static power reduction on two phase CPAL combinational circuits. On an average we are saving 48% of static power by using power gating MTCMOS technique to CPAL circuits and the static power is constant with frequency in power gating MTCMOS CPAL circuits. All the circuits are verified using Cadence 180nm technology with Spectre simulator.**

Keywords -Static power; low power; power-gating; combinational circuits; adiabatic circuits.

I. INTRODUCTION

Low power VLSI design is very popular because increase of portable devices use, to increase the system reliability and to decrease the cost of cooling. Dynamic power dissipation is more dominant in CMOS ICS. As technology improves, dynamic power dissipation is decreased because supply voltages are decreased. To maintain the speed of system, threshold voltages of transistors should be decreased. This intern increases the leakage power dissipation in CMOS ICS as subthreshold leakage current is exponentially related to threshold voltage. For deep sub-micron technology, leakage power dissipation may be more than the dynamic power dissipation. Subthreshold leakage power is dissipated by OFF state MOS transistors, which is more prominent in steady state [1-7].

There are several sources of leakage currents: sub-threshold leakage current due to very low threshold voltage(V_t), gate leakage current due to very thin gate oxide (T_{ox}), and band-to-band tunnelling leakage current due to heavily doped halo [4, 5]. Several leakage reduction techniques, such as dual threshold CMOS, power-gating technique with Multi Threshold Voltage CMOS (MTCMOS), stacking transistor techniques, variable threshold CMOS, and input vector control have been proposed in recent years and achieved considerable energy savings [5-7].

In level restoring CMOS logic circuits, energy drawn from power supply is dissipated as heat through ON resistance of MOS transistors. Adiabatic logic is energy efficient (or low power) technique which dissipates less amount of dynamic power by transferring some of energy back to power supply [2]. Several adiabatic logic families using multi-phase power clocks have been reported [8, 9]. The problems of multi-phase clocking adiabatic circuits include complicated power-clock tree, and multiple power-clock generators, which result in extra area overhead and increase the complexity of the layout place and route [10, 11]. Recently, a CPAL using two-phase power clock scheme has been reported in [12], which can operate in a single-phase power clock by introducing a two-phase power-clock generator [1].

In CPAL circuits power is dissipated even in steady state i.e. for constant input signals, since output nodes always charges and discharges by power clocks. We are applying power gating MTCMOS technique to CPAL circuits to shutdown idle Adiabatic circuits to disconnect their power clocks [13, 14].

This paper focuses on the static power reduction of the two phase CPAL combinational logic circuits using MTCMOS power gating technique. Taken as an example, the static power losses of a 4-bit ripple carry adder using two-phase CPAL circuits with MTCMOS power-gating scheme are investigated at different frequencies.

II. REVIEW OF CPAL CIRCUITS

CPAL Buffer using two-phase power clock scheme have been reported in [12], as shown in Figure. 1. It is composed of two main parts: the logic function circuit and the load driven circuit. The logic circuit consists of four NMOS transistors (N_5-N_8) with Complementary Pass transistor Logic (CPL) function block. The load driven circuit consists of a pair of transmission gates (N_1, P_1 and N_2, P_2). The clamp transistors (N_3 and N_4) ensure stable operation by preventing from floating of output nodes. The detailed description on two-phase CPAL circuits can be found in [12]. Figure 2(a) and 2(b) shows logic symbol of Adiabatic buffer and its simulated waveforms.

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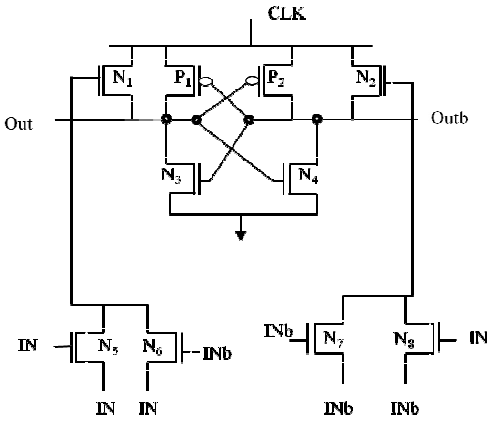

Figure 1. CPAL Buffer [12].

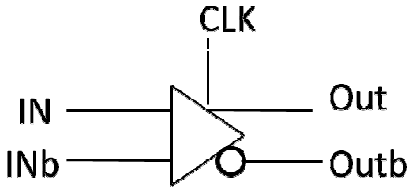

Figure 2(a) Adiabatic buffer symbol [12].

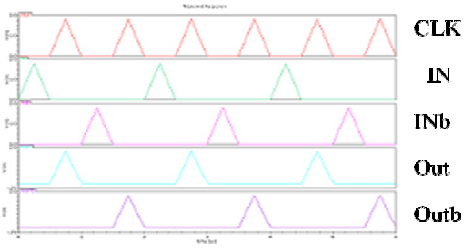

Figure 2(b) Simulated waveforms for buffer.
Figure 2. Adiabatic Buffer symbol and its simulated waveforms.

The CPAL gates (AND/NAND gate, OR/NOR gate, XOR/XNOR gate, and multiplexer) based on the two-phase CPAL can be found in [15].

III. Proposed circuits

i. CPAL Full adder

CPAL Full adder consists of sum generator and carry generator. We modified Architectures of CPL Full adder [15] such that logic function part itself gives required logic to drive load driven circuit. Figure 3(a), 3(b) and 3(c) shows two-phase CPAL sum generator, carry generator and block diagram of Full adder respectively. Figures 3(a) and 3(b) shows only logic function part of sum generator and carry generator of CPAL Full adder.

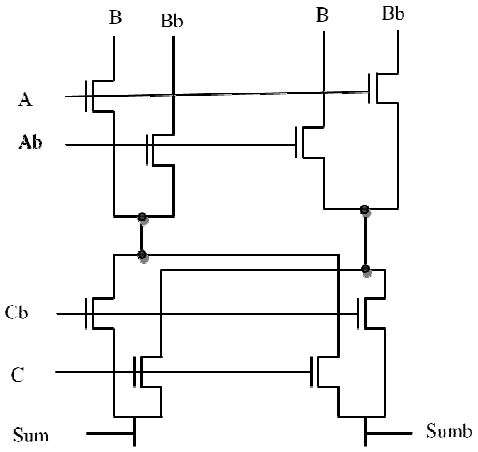

Figure 3(a) Sum generator.

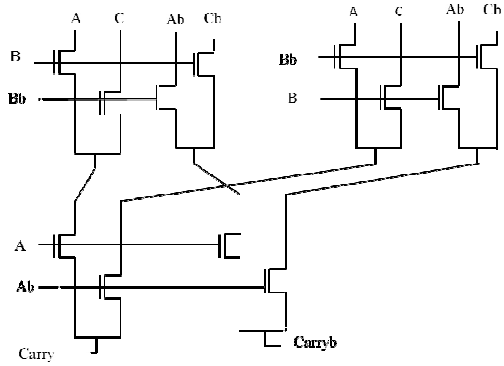

Figure 3(b) Carry generator.

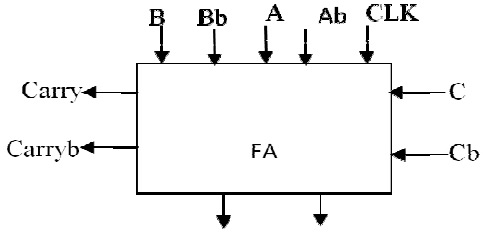

Figure3(c) Full adder symbol.
Figure 3.CPAL Full adder

ii. Power gating scheme

J.P.Hu and Jinghong Fu have proposed very good power gating scheme [1]. We have tested their power gating scheme on combinational circuits but we didn't get attractive results. So we have taken idea of power gating scheme of [1]. The idea is applying power clocks to Adiabatic circuits in active mode and disabling the power clocks in standby mode. This can be easily done using CPAL buffer [12] shown in figure 1. To decrease the leakage power present in Adiabatic buffer we have used the idea [1] in [12]. The idea is to construct

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transmission gate formed by N_1 and P_1 (Figure. 1) with high V_t transistors as described in [1].

The power-gating scheme for CPAL circuits using two-phase power clocks and its simulated waveforms are shown in Figure. 4(a) and 4(b) respectively. CPAL buffer chain used as power gating switches and inserted between power clocks (CLK_1 and CLK_2) and CPAL circuits. Power gating switches are used to disconnect the adiabatic logic block from the power clocks in standby mode to reduce power losses [1].

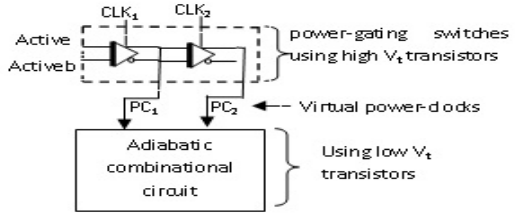

Figure 4(a) Power gating scheme

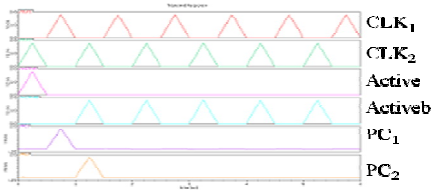

Figure 4(b) Power gating scheme simulated waveforms

Figure 4. Two-phase CPAL power-gating scheme with MTCMOS technique and its simulated results

The power gating adiabatic circuits work in two modes under the control of Active (active enable signal). In active mode, Active is high, thus virtual power clocks (PC_1, PC_2) follow power clocks (CLK_1, CLK_2), and adiabatic logic block works normally. In standby mode, Active is low, thus PC_1 and PC_2 will be set as low level, so Adiabatic logic block is disconnected from power clocks to reduce its power dissipations [1].

We can easily generate two-phase non overlap power clocks using power clock generator which is operating with single power clock [1].

IV. .SIMULATION RESULTS

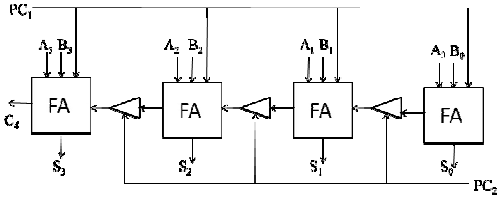

Figure 5. A test bench circuit of 4-bit CPAL ripple carry adder.

We have chosen 4-bit ripple carry adder as a test bench circuit to observe the effect of Power gating MTCMOS technique on static power reduction in two phase CPAL Combinational circuits. A 4-bit CPAL ripple carry adder using two- phase power clock is shown in figure 5. We have used the buffers in between full adders in ripple carry adder to synchronise inputs of adder with power clock. The following table's shows simulation results of 4-bit ripple carry adder in CMOS, CPAL and power gating CPAL configurations. All the simulations carried out at 1MHz frequency.

Table 1. Power comparison of 4-bit ripple carry adder for case1

Circuits	runtime power(µW)	static power(µW)
CMOS	6.4192	1.0582
CPAL	0.8335	1.3538
Power gating CPAL	0.8310	0.63191

In case 1 runtime power is calculated when A [3:0] and B [3:0] make transitions 0001→1110 and 0000→1111 resp. and static power is calculated when A [3:0] and B [3:0] is at 1110 and 1111 resp. In this case we got 87% of run time power saving in CPAL circuits compared to CMOS. We got 53% of static power saving by using power gating Adiabatic circuits.

Table 2. Power comparison of 4-bit ripple carry adder for case2

Circuits	runtime power(µW)	static power(µW)
CMOS	7.8729	1.4537
CPAL	0.8312	1.4372
Power gating CPAL	0.8298	0.8986

In case 2 runtime power is calculated when A [3:0] and B [3:0] make transition 1110→0001 and 1111→0000 resp. and static power is calculated when A [3:0] and B [3:0] is at 0001 and 0000 resp. In case we got 89.44% of runtime power saving in CPAL circuits compared to CMOS. We got 37% of static power saving by applying power gating MTCMOS technique to CPAL circuits.

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Table 3. Power comparison of 4-bit ripple carry adder for case3

Circuits	runtime power(µW)	static power(µW)
CMOS	2.9486	1.3133
CPAL	1.1231	1.4095
Power gating CPAL	1.1252	0.632

In case 3 runtime power is calculated when A [3:0] and B [3:0] makes transition 0000→1000 and 0000→0111 resp. and static power is calculated when A [3:0] and B [3:0] is at 1000 and 0111 resp. In this case we got 62% of runtime power saving and 55% of improvement in static power.

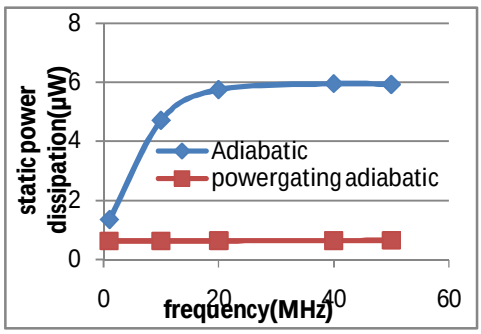
Table 4: Variation of static power of power gating Adiabatic ripple carry adder with frequency

Static power dissipation in (µW)		
freq(MHz)	CPAL	power gating CPAL
1	1.3538	0.6319
10	4.7186	0.6326
20	5.75411	0.6342
40	5.9574	0.6396
50	5.9316	0.6433

Table 4 shows the variation of Static power of power gating CPAL 4-bit ripple carry adder with frequency for case1.

Figure 6 shows the variation of static power of power gating MTCMOS CPAL 4-bit ripple carry adder with frequency.

Figure 6. Static power variation with frequency



From the figure 6 we will notice that static power of Adiabatic ripple carry adder increases with frequency but for power gating Adiabatic ripple carry adder static power is almost constant with frequency.

V. CONCLUSION

This paper presents the static power reduction of two phase CPAL combinational circuits using MTCMOS power gating scheme. The results show that on an average 80% of dynamic power is reduced compared to CMOS and 48% of static power loss is reduced compared to CPAL by using power gating MTCMOS technique to CPAL circuits and the static power of power gating MTCMOS CPAL circuits almost constant with frequency whereas for the reported CPAL circuit's static power is varying with frequency.

ACKNOWLDGEMENT

This project is supported by Department of Electronic Engineering, Indian Institute of technology (BHU), Varanasi, India.

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