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INVESTIGATION ON TOTAL HARMONIC DISTORTION IN FIVE LEVEL CASCADED H-BRIDGE INVERTER

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***Abstract*-It becomes complex to connect the power semiconductor switches directly to medium and high level voltages. Hence to overcome complexities multilevel inverters came into picture and it has gained more attention in market for various applications like renewable energy systems, industrial motor drives, etc. Multilevel Inverters produce output voltages with good quality and contains less harmonic distortion. In this paper, the single phase five level cascaded H-bridge inverter is modeled in MATLAB/SIMULINK. Here, sinusoidal pulse width modulation (SPWM) techniques are used to trigger the switching device used in CHMLI. The Total Harmonic Distortion (THD) is observed and reduced by varying the modulation index and frequency modulation of SPWM.**

Keywords: *cascaded H-bridge multilevel inverter, five level cascaded H-bridge inverter (FCI), sinusoidal pulse width modulation, total harmonic distortion.*

1. INTRODUCTION

The tremendous increase in energy demand led to call of high power converter technology to transmit the power with high accuracy. When dealing with high voltages, conventional inverters produce output voltages of low quality and high harmonic content which affects the equipment performance. So new power converter topologies were invented known as multilevel inverters and gained importance in industry applications because of high power ratings and better harmonic performance suitable for medium and high power applications. The output voltage of multilevel inverters is in form of stepped waveforms and obtained easily without use of transformers which decreases the cost of inverter. Improved quality of waveforms can be obtained by increasing number of steps in the output waveforms and the harmonic content also comes down. Multilevel Inverters are classified into three topologies namely diode clamped, flying capacitor and cascaded type inverters. PWM is a technique in which width of gate pulses are controlled and used for various applications. Different types of PWM techniques are proposed for multilevel inverters like sinusoidal pulse width modulation, selective harmonic elimination and space vector modulation. SPWM is considered as the best technique among other PWM methods because of various reasons like high power handling capacity, no temperature variation, easy to implement and control. Here SPWM is used for modeling of five level cascaded H-bridge inverter (FCI). The design and modeling of FCI is done in MATLAB/SIMULINK.

2. CASCADED H-BRIDGE MULTILEVEL INVERTER (CHMLI)

CHMLI is a series connection of single phase H-bridge inverters units. The CHMLI is well suited for high power applications among other topologies because of high modularity degree. It gives continuous supply to load even if there is fault in any module and thus it is very reliable. Each module requires one dc source which may be acquired from solar cells, batteries. Cascaded Inverters are ideal for connecting renewable energy sources with an ac grid, because of the need for separate dc sources, which is the case in applications such as photovoltaic or fuel cells.

For N number of output levels, the total number of H-Bridge units (M) required is shown as [1]

$$M= (N-1)/2$$

In this paper, CHMLI topology is used for modeling of MLI. To get five levels in output voltage, two H-bridge modules are required. The design of five level cascaded H-bridge inverter is shown in figure 1. Each module consists of four switches and by different combinations of switches (S11-S24) five different voltage outputs, +2Vdc, +Vdc, 0 and –Vdc, –2Vdc[2]. The switching pattern of eight switches in the module of five level cascaded H-bridge inverter is shown in Table 1[1].

2.1 Importance of CHMLI:

- It reaches high output voltages and high power levels.
- Higher reliability due to greater modularity degree.
- Requires least number of components for building circuit.
- The voltage stress on switching devices is reduced.

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- Easier to increase the number of levels by adding the modules.
- Elimination of big transformers which leads to decrease in cost.

TABLE 1: Switching pattern of five level cascaded H-bridge inverter

Switches	**Inverter Voltage**				
	+2Vdc	*+Vdc*	*0*	*-Vdc*	*-2Vdc*
S_{11}	1	1	1	0	0
S_{12}	0	0	1	1	1
S_{13}	0	0	1	1	1
S_{14}	1	1	0	0	0
S_{21}	1	1	1	0	0
S_{22}	0	1	1	0	1
S_{23}	0	0	0	1	1
S_{24}	1	0	0	1	0

3. MULTILEVEL SINUSOIDAL PULSE WIDTH MODULATION (MSPWM)

In cascaded H-bridge multilevel inverters, the switching action of semiconductor devices is done by following SPWM technique. SPWM technique consists of a Sinusoidal reference signal and a high frequency carrier signal. In case of multilevel inverters MSPWM technique is employed where for N numbers of output levels, N-1 carrier signals are used. The reference signal is a sinusoidal waveform of frequency (F_r) and amplitude (A_r).The carrier signal is triangular in nature and all carrier waves have same frequency (F_c) and amplitude (Ac). The reference signal and carrier waves are compared at every instant of time and the output obtained is given as input to active devices. The output of MSPWM varies between +1 and zero[3]-[7]. The various types of multilevel sinusoidal pulse width modulation are shown in figure 1.

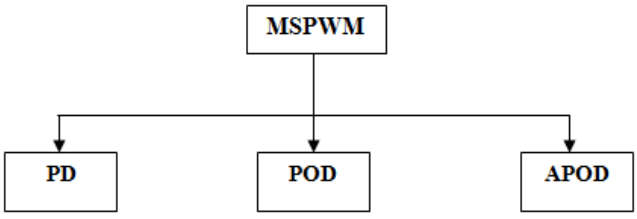

Figure 1: Types of MSPWM

Modulation index (M_a) = $A_r/2A_c$

Frequency modulation = Fc/Fr

3.1 Phase Disposition (PD) PWM

In this method, all carriers above and below zero axes are in phase with each other as shown in figure 2.

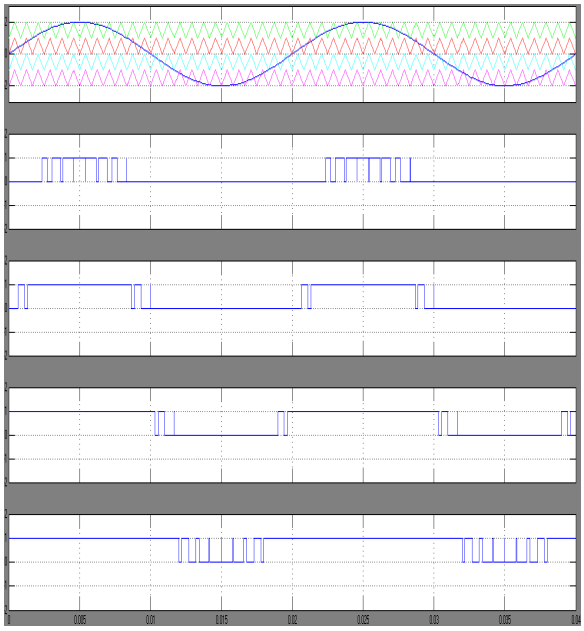

Figure 2: PDPWM

3.2 Phase Opposition Disposition (POD) PWM

In this method, there is phase difference of 180^0 between all carriers lying above and below the zero axes. PODPWM is shown in figure 3.

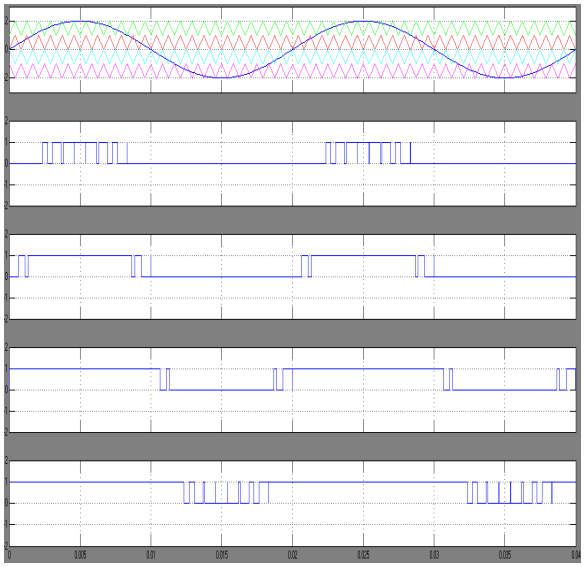

Figure 3: POD PWM

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3.3 Alternative Phase Opposition Disposition (APOD) PWM

In this method, there is phase difference of 180^0 between two alternate carrier signals as shown in figure 4.

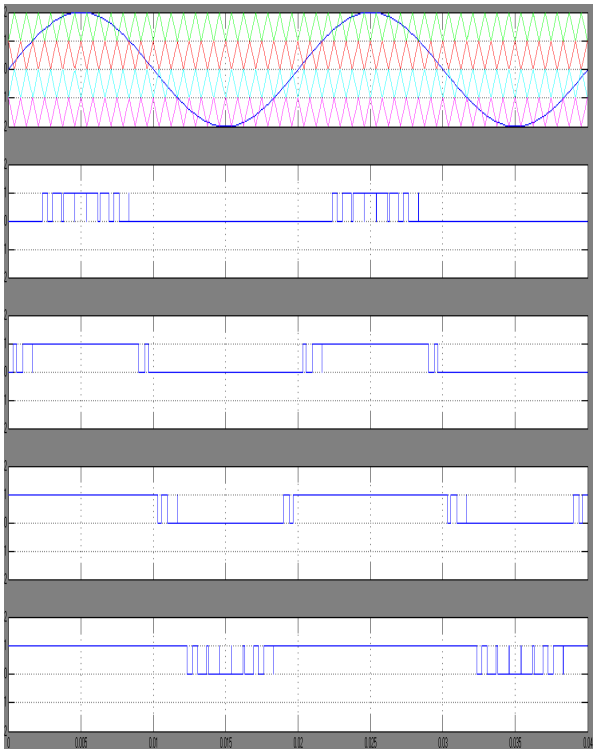

Figure 4: APOD PWM

4. SIMULATION CIRCUIT

4.1 IGBT Triggering Circuit

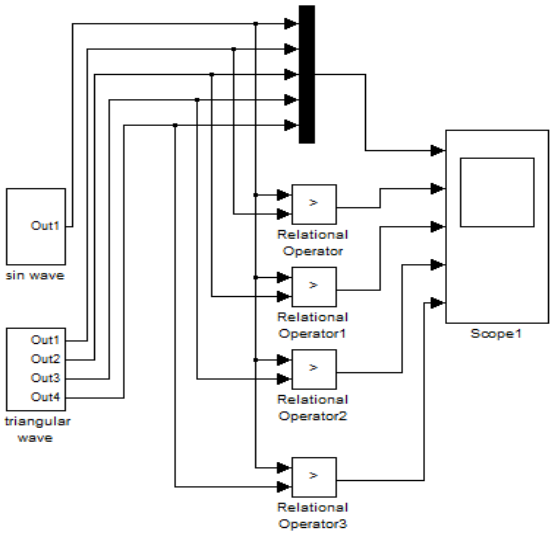

Figure 5: IGBT triggering circuit

4.2 Five Level Cascaded H-Bridge Inverter (FCI) With Triggering Subsystem

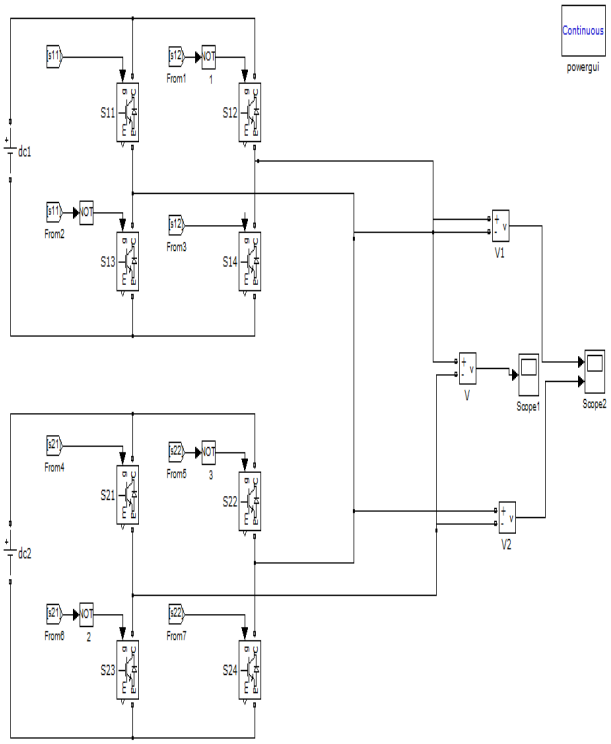

Figure 6: Five Level Cascaded H-Bridge Inverter

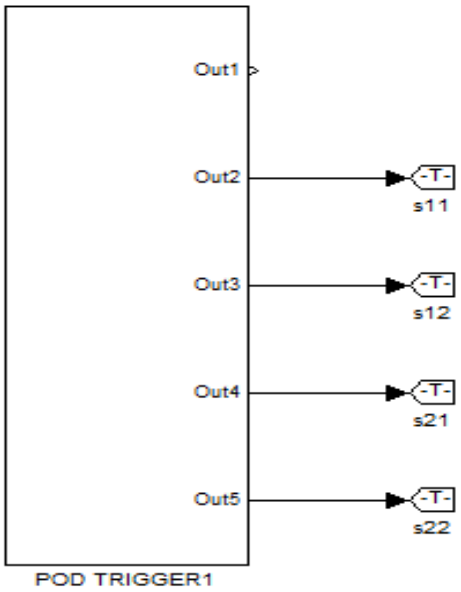

Figure 7: Triggering Circuit Subsystem

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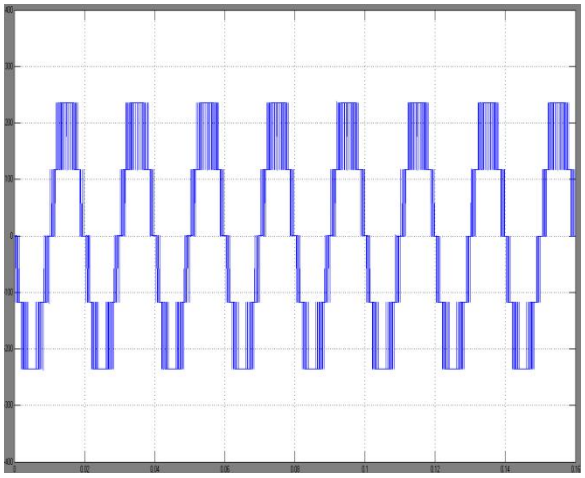

Figure 8: Output voltage of PDPWM FCI

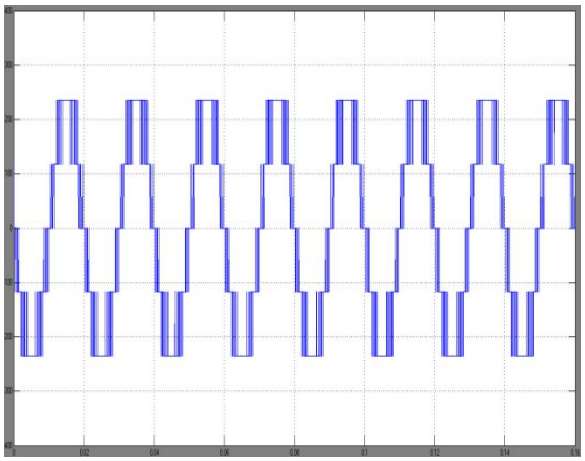

Figure 9: Output voltage of PODPWM FCI

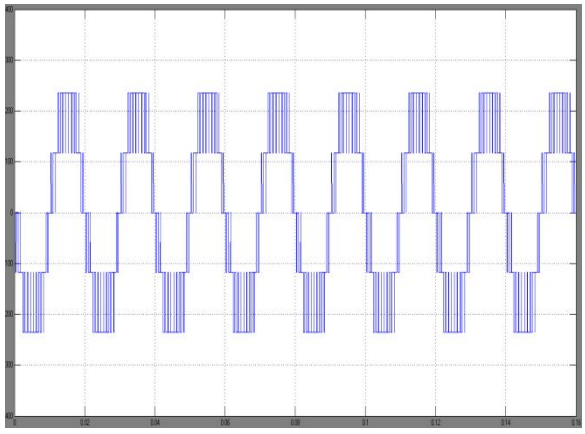

Figure 10: Output voltage of APODPWM FCI

5. SIMULATION RESULT

TABLE 2: F_c =1200 Hz, F_r =50 Hz

M_a	Total Harmonic Distortion(THD)		
	PD	POD	APOD
0.6	44.15	43.94	44.91
0.7	41.49	36.43	41.56
0.8	38.23	37.47	39.12
0.9	33.44	32.71	33.89
1.0	26.76	26.05	26.22

TABLE 3: F_c=1800 Hz, F_r=50 Hz

M_a	Total Harmonic Distortion(THD)		
	PD	POD	APOD
0.6	42.97	42.72	44.46
0.7	40.82	35.02	41.73
0.8	37.49	36.77	37.54
0.9	32.58	31.63	32.30
1.0	25.09	24.57	24.99

TABLE 4: F_c =2400 Hz, F_r =50 Hz

M_a	Total Harmonic Distortion(THD)		
	PD	POD	APOD
0.6	42.12	41.84	44.31
0.7	40.26	34.24	41.14
0.8	37.29	36.32	37.32
0.9	37.12	30.93	31.41
1.0	25.16	24.23	24.41

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CONCLUSION

This present work proposes the Simulation model of Five Level Cascaded H-Bridge inverter. Here different multilevel sinusoidal pulse width modulation techniques are employed to trigger the switching components and total harmonic distortion for every scheme is observed. After investigating different techniques, it is found that Phase Opposition Disposition (POD) technique yields less THD in the output voltage waveform of CHMLI. The THD level is further reduced by increasing the carrier frequency of MSPWM.

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